Mask Set Errata for Mask 1M09S

Introduction

This report applies to mask 1M09S for these products:

- PXN20

Errata ID	Errata Title
1282	CRP: Spurious Pin Wakeup in Run Mode
2340	FEC: slot time is designed for 516 bit times; deviation from the 802.3
2382	FLASH: Flash Array Integrity Check
3659	FLASH: Resuming after a suspend during an Erase may prevent the erase from completing.
3853	Flash array reads may be incorrect after wake up from sleep mode
2501	LPM: High VDD Sleep Mode Current

e1282: CRP: Spurious Pin Wakeup in Run Mode

Errata type: Errata

Description: During RUN mode, a CRP_PSCR[PWKSRCF] flag may be unintentionally set instead of the intention of only setting the wakeup flags during Sleep mode. The pin wakeup flags work fine during Sleep mode. There is not an issue when the pin wakeup flags are disabled. The flag may be set during flag configuration of CRP_WKSE[WKCLKSEL], CRP_WKPINSEL[WKPSELn], and CRP_WKSE[WKPDETn]. The flag may also be set if there is a change in the wakeup pin at the same time as the internal system clock or the internal pin wakeup clock. Note that if the pin toggles then the flag may be set regardless of whether the pin is selected as posedge or negedge.

Workaround: Workaround for unintentional flag setting during configuration, would be to first complete the pin wakeup configuration (i.e. select pin wakeup clock, select pin muxing, and configure pin enable/edge detect via the CRP registers CRP_WKSE[WKCLKSEL], CRP_WKPINSEL[WKPSELn], and CRP_WKSE[WKPDETn]). Then poll the CRP_PSCR[PWKSCRF] pin wakeup flag and if set write one to clear and then recheck. May take one pin wakeup clock cycle to clear.

Workaround for unintentional flag setting during pin change is to have the SLEEPF and STOPF flags in CRP_PSCR checked in the CRP interrupt service routine and if neither of them is set then clear all flags in CRP_PSCR[PWKSRCF].

e2340: FEC: slot time is designed for 516 bit times; deviation from the 802.3

Errata type: Information

Description: The Fast Ethernet Controller (FEC) slot time is 516 bit times which is longer than the 512 bit times specified by the IEEE 802.3 standard.

If a collision occurs after the standard 512 bit times (but prior to 516 bit times), the FEC may generate a retry that a remote ethernet device may identify as late. In addition, the slot time is used as an input to the backoff timer, therefore the FEC retry timing could be longer than expected.

Workaround: No software workaround is needed or available.

e2382: FLASH: Flash Array Integrity Check

Errata type: Errata

Description: The Flash Array Integrity Check (AIC) which may be enabled during the flash user test (UTest) mode does not return the expected UMn[MISR] values for some flash PFCRPn[RWSC] read wait state configurations. For PFCRPn[RWSC] values of 3-6, the UMn[MISR] signature computation during AIC does not include the data read from the very last address in the selected address sequence and thus the UMn[MISR] value is not as expected. For PFCRPn[RWSC] values of 7, the UMn[MISR] signature computation during AIC will not be correct as well.

Workaround: The Flash Array Integrity Check is correct for PFCRPn[RWSC] values of 0-2. For PFCRPn[RWSC] values of 3-6, the expected UMn[MISR] values will not include the data read from the very last address and thus the value expected should be for the data read up to the 2nd-last address in the selected address sequence. For a PFCRPn[RWSC] value of 7, the Array Integrity Check should not be used at all.

e3659: FLASH: Resuming after a suspend during an Erase may prevent the erase from completing.

Errata type: Errata

Description: If an erase suspend (including the flash put into sleep or disabled mode) is done on any block in the low Address Space (LAS) or the Mid-Address Space (MAS) except the 16KB blocks, or if a suspend is done with multiple non-adjacent blocks (including the High Address Space [HAS]), the flash state machine may not set the FLASH_MCR[DONE] bit in the flash Module Control Register. This condition only occurs if the suspend occurs during certain internal flash erase operations. The likelihood of an issue occurring is reduced by limiting the frequency of suspending the erase operation.

Workaround: If the suspend feature (including disable and sleep modes) of the flash is used, then software should ensure that if the maximum time allowed for an erase operation occurs without a valid completion flag from the flash (FLASH_MCR[DONE] = 1), the software should abort the erase operation (by first clearing the Enable High Voltage (FLASH_MCR[EHV]) bit, then clearing the Erase read/Write bit (FLASH_MCR[ERS] bit) and the erase operation should be restarted.

Note: The cycle count of the sector is increased by this abort and restart operation.

e3853: Flash array reads may be incorrect after wake up from sleep mode

Errata type: Errata

Description: Code execution from flash immediately after going out of sleep mode, may return incorrect data. Issue may affect both data and instruction reads to any array location.

Workaround: The assertion of a system reset (internal WD) will correct the flash reads. Also, a sleep mode entry and exit sequence will correct flash reads.

Using the software watchdog timer, to ensure that code is properly executing from flash after Sleep mode, is recommended.

e2501: LPM: High VDD Sleep Mode Current

Errata type: Errata

Description: The VDD Sleep Mode currents are 350uA (typ, 25C) / 2500uA (max, 150C) compared to the targets in the preliminary Data Sheet specification of 100uA (typ, 25C) / 900uA (max, 150C).

Workaround: None.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

Document Number: PXN20_1M09S
Rev. 11 APR 2012