Mask Set Errata for Mask 1M00S

Introduction

This report applies to mask 1M00S for these products:

- MCF51EM256
- MCF51EM128

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0J27F. All standard devices are marked with a mask set number and a date code.

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "0301" indicates the first week of the year 2003.

Some MCU samples and devices are marked with an SC, PC, or XC prefix. An SC prefix denotes special/custom device. A PC prefix indicates a prototype device which has undergone basic testing only. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC or SC prefix.

SE184-FLVD-STOP3: False low voltage detect when exiting stop3

Errata type: Silicon
Affects: SoC level behavior
Description: If the low voltage detect (LVD) is enabled (LVDE = 1) but not in stop mode (LVDSE = 0), on some devices the low voltage detect flag (LVDF) will occasionally be set when exiting stop3 mode. If the LVD interrupt is enabled (LVDIE = 1) the interrupt vector will be fetched. If the LVD reset is enabled, the part will reset, and the LVD bit in the System Reset Status (SRS) register will be set. The correct operation of the device is to wake and execute the code immediately after the STOP instruction.

If the LVD is not enabled (LVDE = 0) or if LVD is also enabled during stop mode (LVDSE = 1) then this issue will not occur. If the LVD is enabled during stop mode the stop3 current will increase.

Workaround: A software level change to reliably eliminate the issue is to use only the LVD interrupt (LVDE = 1, LVDIE = 1, and LVDRE = 0). Inside the LVD interrupt service routine, a short state of health check can be made to verify the supply level before proceeding. In this routine, the LVDF should be cleared and then read to determine whether a true low voltage event is present. If the LVDF is set when it is read, then a true LVD condition exists and the MCU can be reset by forcing the execution of an illegal op-code.

SECF176: XTAL2/EXTAL2 pin functions selected when XOSC1 used as ICS source

Errata type: Silicon
Affects: Pin
Description: If XOSC1 (32 kHz IRTC oscillator) is configured as the MCU clock source (CCSCTRL:SEL = 1, ICSC2: EREFS = 1), the PTC0/KBIP6/EXTAL2/RX3 and PTC1/KBIP7/XTAL2/TX3 pins are dedicated as EXTAL2 and XTAL2 functionality, respectively, and cannot be configured for any other multiplexed pin functions.

Workaround: In order to use the PTC0 and PTC1 pins as any other function than EXTAL2 and XTAL2, the oscillator must be disabled (ICSC2:EREFS = 0) and an alternate clock source must be selected for the ICS (external clock or internal reference).

SECF177: ADCOFS registers do not update with values determined during calibration

Errata type: Silicon
Affects: ADC
Description: Offset correction registers ADCxOFSH:ADCxOFSL are $0000 by default on POR, but are supposed to be auto-updated with a value determined through the ADC calibration process. Instead, the offset correction registers remain in their default POR states after calibration. There is no automatic offset correction for ADC conversions performed after calibration..

Workaround: The user may still write an offset correction value to the ADCxOFSH:ADCxOFSL registers and this value will be subtracted from subsequent ADC conversion results. It is recommended that the user implement a gain/offset determination during factory test, as ADC internal calibration was never intended to compensate for system gain or offset error.

SECF206-iRTC: iRTC repeatedly loops within the hour after Daylight Saving Time (DST) falls back

Errata type: Silicon
Affects: iRTC
Description: iRTC repeatedly loops within the hour after Daylight Saving Time (DST) falls back. This erratum only impacts iRTC when daylight saving falls back. Other features including DST forward are not impacted.

Following is an example where the erratum occurs:

If the iRTC is configured to have DST forward on day A at 14:00:00 and to have DST falls back on day B at 16:00:00 then the following behavior will be observed.

Forward on date A:
13:59:59 ->15:00:00

Fallback on date B:
The erratum behavior occurs in ***bold italics***: 15:59:59 -> 15:00:00 -> 15:59:59 **-> *15:00:00***
The correct behavior occurs in **bold**: 15:59:59 ->15:00:00 -> 15:59:59 **-> 16:00:00**

In the example above, the iRTC correctly rolls from 15:59:59 to 15:00:00 when fallback occurs. After the fallback occurs, the next hour roll over should be from 15:59:59 to 16:00:00 but it is incorrectly roll back to 15:00:00. iRTC then falsely loops between 15:59:59 and 15:00:00 repeatedly.

Workaround: This issue can be resolved by software where the iRTC Alarm feature disables the DST after the fallback event occurs. Then re-enables the DST after the iRTC passes the next hour (e.g after 16:00:00). Make sure the DST is re-enabled before the next DST event occurs.

Note that this workaround requires MCU to wake up when DST fallback event occurs once a year. Therefore, in additional to have power present at VBAT pin, it is also required to have power present at MCU VDD pins when DST fallback occurs.

Following is an example of the workaround:

15:59:59 -> 1st alarm (counter ==0)

- 15:59:59 falls back to 15:00:00
- In Alarm interrupt service routine :
  - Update software counter = 1 ;
  - Re-configure next alarm to a time before the next 15:59:59 roll over. In this example we keep the alarm time same as the first one at 15:59:59.

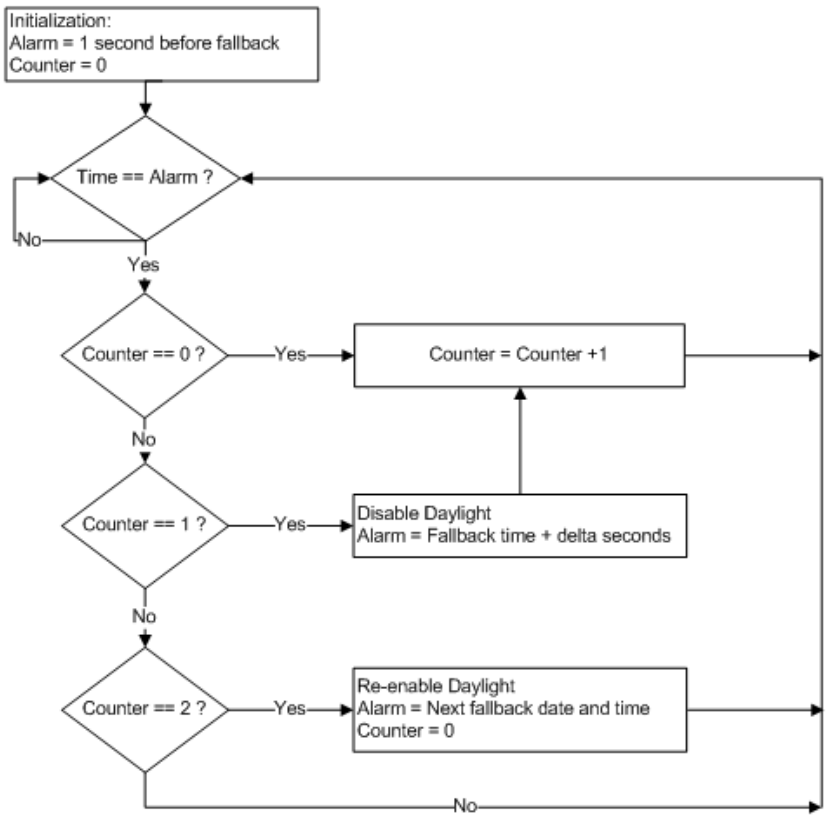
15:59:59 -> 2nd alarm (counter ==1)

- In Alarm interrupt service routine:
  - Disable DST feature. This allows 15:59:59 to correctly roll to 16:00:00
  - Re-configure next alarm to a time after 16:00:00. We recommend choosing a time long enough to account for alarm interrupt service routine execution time. Testing showed that with 15 seconds after roll over time is a safe delay. In this example the next alarm is set to 16:00:15
  - Set software counter = 2;

16:00:15 -> 3rd alarm (counter ==2)

- Re-enable DST feature so that the next DST event can occur.
- Re-configure alarm to the next DST fallback date and time
- Reset counter (counter = 0)

See following flow chart for the workaround example described above:


Initialization:
Alarm = 1 second before fallback
Counter = 0
Time == Alarm ?
No
Yes
Counter == 0 ?
Yes
Counter = Counter +1
No
Counter == 1 ?
Yes
Disable Daylight
Alarm = Fallback time + delta seconds
No
Counter == 2 ?
Yes
Re-enable Daylight
Alarm = Next fallback date and time
Counter = 0
No

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