MSE908QL4_0L76W
Rev. 0, 8/2005

Mask Set Errata for Mask 0L76W

Introduction

This mask set errata applies to the mask 0L76W for these products:

- MC908QL4

MCU Device Mask Set Identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0L76W. All standard devices are marked with a mask set number and a date code.

WAKETX — Wakeup Pulse on the LIN Bus

SE100-WAKETX

Description

If the LIN bus has been idle for more than 4096 CPU bus clock cycles before setting the WAKETX bit, a wakeup pulse will not be transmitted on the LIN bus.

freescale™
semiconductor

Workaround

1. Switch the SLIC module into BTM mode by setting the BTM bit in SLCC2
2. Set an appropriate bit time value so that a 0x00 data character (9 bit times) will be transmitted long enough to appear as a valid wakeup pulse on the LIN bus. (refer to appropriate LIN specification for exact timing requirements of the wakeup symbol)
3. Write a non-zero value to SLCID register (required step)
4. Write a 0x00 value to the SLCID register
5. Write the TXGO bit in SLCDLC register to initiate transmission of 0x00 character
6. Clear the BTM bit in the in SLCC2 register to return to LIN operation

CHKSUM — Byte Framing Error Can Corrupt Checksum Calculation of the Next Message Frame

SE101-CHKSUM

Description

If a byte framing error is detected in the identifier byte of a message header, it can corrupt the checksum calculation of the next message frame. If the next received message header is received properly and determined to use the enhanced checksum method (identifier byte is included in the checksum calculation), the checksum for that second message may be corrupted. The identifier byte that contained the byte framing error will be included in the checksum calculation of the subsequent message frame.

Workaround

If a byte framing error is encountered, set the CHKMOD bit in the SLCDLC register with a data length of 0x00 to reset the checksum calculator.

SLIC — Bit Errors May Go Undetected

SE102-SLIC

Description

Bit errors are not detected above certain LIN bus speeds, given certain SLIC clock settings. Table 1 shows the LIN bus speed at which bit errors will no longer be detected, given a specific CPU bus speed. The cutoff values assume the internal oscillator has been trimmed:

Table 1. Cutoff Values

Frequency (MHz)	Bit Error Cut Off Frequency (kbps)
2	10

Table 1. Cutoff Values

Frequency (MHz)	Bit Error Cut Off Frequency (kbps)
3.2	16
6.4	32
8	40

Workaround

Operate the device with the CPU at 6.4 MHz (trimmed) and all valid LIN bus speeds are achievable with bit error detection operational.

LIN — Bit Errors Undetected in LIN Message Bits

SE103-LIN

Description

Bit errors will not be properly detected in the following LIN message bits (at any LIN bus speed):

Bit 7 of all data/checksum bits

STOP bit of checksum byte

STOP bit of 8th, 16th, 24th, 32nd, 40th, 48th, 56th data bytes of extended frames handled in LIN mode

Workaround

None.

BTM — In BTM mode, SLIC Will Not Transmit a Byte if the Value Matches the Value in SLCID

SE104-BTM

Description

When the SLIC is operating in BTM mode, the SLIC will not transmit a byte if the value matches the value currently loaded in the SLCID register.

Workaround

When the SLIC is operating in BTM mode, the SLCID register must be loaded with a value that differs from the value currently in the register to transmit when the TXGO bit (SLCDLC register) is set. One way to ensure that this happens on each transmission is to:

1. Create a temporary byte value equal to the desired transmit byte plus one
2. Load that temporary value into SLCID
3. Load correct byte to be transmitted into the SLCID register
4. Set TXGO to initiate transmission