MSE908QB8_3M62B
Rev. 0, 6/2006

Mask Set Errata for Mask 3M62B

Introduction

This mask set errata applies to the mask 3M62B for these products:

- MC68HC908QB8
- MC68HC908QB4
- MC68HC908QY8

MCU Device Mask Set Identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 3M62B. All standard devices are marked with a mask set number and a date code.

CONFIG2 Register Bit RSTEN Is Cleared by an LVI Reset

SE111-RSTEN

Description

The $\overline{\text{RST}}$ pin functionality is enabled in the CONFIG2 register by RSTEN. In the data sheet, this bit is described to be unaffected by all resets other than a power-on reset (POR).

RSTEN in the CONFIG2 register is cleared by an LVI reset only. This behavior prevents the $\overline{\text{RST}}$ pin from driving low during an LVI reset when the $\overline{\text{RST}}$ function is enabled.

The MCU will perform an internal reset as expected. All other reset sources will drive the $\overline{\text{RST}}$ pin low during an internal reset if the $\overline{\text{RST}}$ function is enabled. This is a known issue and will be fixed on subsequent masks.

Workaround

RSTEN must be configured by application code after an LVI reset has occurred. This ensures that the $\overline{\text{RST}}$ pin is configured as expected.

If necessary, an indication of LVI reset can be forced in user code by monitoring the LVI bit in SRS and immediately driving PTA3 low for any number of cycles during program startup. The CONFIG registers can then be written to enable the $\overline{\text{RST}}$ function. Note that this may cause an extra apparent reset low signal because the LVI bit in SRS is typically set during power-up.