Mask Set Errata

MSE08JL3_1K24E
12/2002

Mask Set Errata for 08JL3, Mask 1K24E

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Introduction

This mask set errata applies to this 08JL3 MCU mask set:

- 1K24E

MCU Device Mask Set Identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 1K24E. All standard devices are marked with a mask set number and a date code.

MCU Device Date Codes

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code “0201” indicates the first week of the year 2002.

MCU Device Part Number Prefixes

Some MCU samples and devices are marked with an SC, PC, or XC prefix. An SC prefix denotes special/custom device. A PC prefix indicates a prototype device which has undergone basic testing only. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC or SC prefix.

Glitch on Timer Buffered PWM Output

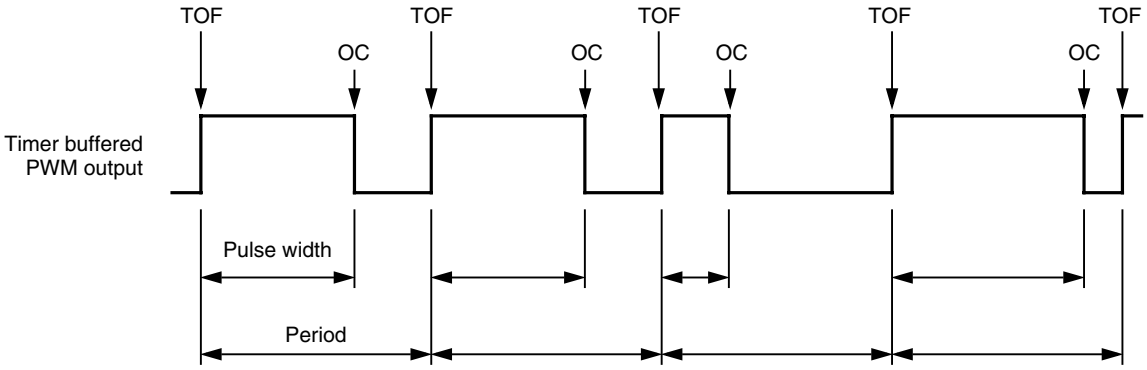
SE30-PWM

In timer buffered PWM operation, when a timer overflow (TOF) event or an output compare (OC) event coincides with a write to either pair of the timer channel registers (TCHxH/L), the duty cycle at the PWM output glitches to 0% or 100% momentarily, then returns to proper operation.

To avoid the glitches when changing the PWM duty cycle, do not write to either pair of the timer channel registers at the TOF or OC.

For example, in the TOF interrupt service routine: If the OC occurs near the last TOF, write to the timer channel registers after the OC; if the OC occurs near the next TOF, write to the timer channel registers before the OC. A write to the channel register high byte (TCHxH) should immediately followed by a write to the low byte (TCHxL) to avoid TOF or OC occurring between the writes. Instruction cycle times must be included when making timing calculations.

The figure below shows a typical timer buffered PWM output waveform, indicating the TOF and OC events.



NOTES:

Do not write to either pair of timer channel registers at:
TOF (timer overflow), or
OC (timer output compare) edges.

In buffered PWM, the pulse width is defined by the last written pair of timer channel registers.
Each pair of timer channel registers consist of a high byte register (TCHxH) and a low byte register (TCHxL).

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