Silicon Errata for the MSC8102 Processor, Mask 1K94M

This document presents the errata for the 1K94M mask of the Freescale MSC8102 device. The errata are classified and numbered, and each erratum is provided with a description and workarounds.

Silicon Errata

Errata Number	Errata Description	Mask
QSE1	**Prefetch Fault** **Date Added:** 2/2002 **Description:** In PPC-Little-Endian mode, a 32-bit bus prefetch fault cause a prefetch in the wrong order. **Impact:** The option to use prefetch is eliminated in this mode (32-bit PPC little endian), causing a delay in data reads **Workaround:** Disable the prefetch when this mode is in use. **System Number:** 7588	1K94M
QSE2	**DSI Protocol Violation** **Date Added:** 2/2002 **Description:** During 64-bit read accesses in synchronous mode, the DSI may violate the DSI protocol, causing data loss or invalid bus behavior. **Impact:** Eliminates the use of 64-bit burst read reads in synchronous mode (a minor impact on DSI throughput). **Fix Plan:** HIP8 Version of MSC8102, which is the MSC8122 device **Workaround:** Do not perform burst read when at 64bit synchronous mode. **System Number:** 7434	1K94M
QSE9	**Synchronous, 64-Bit Mode DSI Protocol Violation** **Date Added:** 4/15/2002 **Description:** In a DSP Farm application running in Synchronous 64-bit mode, when a read or write is performed to one DSI after a write burst is performed to another DSI, a contention may occur on the HTA_B signal. This contention may cause the DSI to violate DSI protocol, resulting in data loss or bus invalid behavior. **Impact:** Eliminates the use of a burst write in 64-bit at synchronous mode in DSP farm applications (a minor impact on DSI throughput). **Fix Plan:** HIP8 Version of MSC8102, which is the MSC8122 device **Workaround:** Do not perform a burst write in Synchronous 64-bit mode in DSP farm applications. **System Number:** 7852	1K94M

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QSE12	**Write Immediate Through Write Buffer** **Date Added:** 5/2002 **Description:** If the SC140 core initiates a "write immediate" (see EQBS chapter) when the Write Buffer is not empty, the SC140 core may continue before the end of the write. The SC140 core may continue when the data of the write is still in the Write Buffer. The write eventually arrives at its destination, but there is no guarantee of synchronization with the SC140 core. **Impact:** "Write immediate" through the Write Buffer may not freeze the SC140 core. **Fix Plan:** HIP8 Version of MSC8102, which is the MSC8122 device **Workaround:** *Option 1:* Write 2 "write immediate" at the same execution set. *Option 2:* Write "write immediate" with read from external memory, at the same execution set. *Option 3:* Write "write immediate" when the Write-Buffer is empty. *Option 4:* Do not use write immediate through the Write Buffer. If it is necessary, turn the Write Buffer off. Then, all writes are immediate. **System Number:** 7896	1K94M
QSE14	**Incorrect Masking of Machine Check Interrupt** **Date Added:** 5/2002 **Description:** **Incorrect Masking of** Machine Check Interrupt (MCP)**.** **Impact:** Because of data errors (parity / ECC), the MCP is masked by the SYPCR[30]:SWRI bit. **Fix Plan:** HIP8 Version of MSC8102, which is the MSC8122 device **Workaround:** Clear SYPCR[30]:SWRI to get a data error indication. Clearing of SWRI also means an MCP generation instead of a hard reset generation on Software Watchdog time-out. **System Number:** 3695	1K94M
QSE17	**Attributes are Not Captured Due to Data Parity Error** **Date Added:** 5/2002 **Description:** **When a data parity error occurs, the Machine Check Procedure (MCP) is generated, but the transaction attributes, such as address and TC, are not captured in the** TESCR registers. **Impact:** Cannot locate the initial cause of the parity error. **Fix Plan:** HIP8 Version of MSC8102, which is the MSC8122 device **Workaround:** None. **System Number:** 7775	1K94M
QSE24	**Illegal Execution Set Freezes SC140 Core** **Date Added:** 5/2002 Date Revised: 4/2003 **Description:** In rare situations, an illegal execution set fetched by the SC140 core can alter the settings of system registers or cause the SC140 core to enter a freeze state that can only be released by reset. **Impact:** The SC140 illegal instruction trap does not provide 100 percent protection against execution of illegal instructions. **Workaround:** No workaround available. **System Number:** 7541	1K94M

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QSE26	**Bus Error Interrupt After Access to Non-valid Address** **Date Added:** 5/2002 **Description:** Bus error interrupts are for recognizing accesses from the SC140 core that are for non-valid addresses in internal memory space. A non-valid address is an address that is not mapped in the internal memory system (EQBS, EOnCE, L1 Memory). In some cases, the bus error interrupt does not occur after access to a non-valid address in internal memory. **Impact:** In some cases a bus error interrupt is not asserted. **Workaround:** No workaround available. **System Number:** 7894, 7693, 7864	1K94M
QSE30	**Bus Monitor Asserts Spurious $\overline{\text{TEA}}$ After Address Retry** **Date Added:** 6/2002 **Description:** The bus monitor does not recognize the competition of an Address Retry transaction and will assert $\overline{\text{TEA}}$ if there is no bus activity for a time equal to the expiration time. **Fix Plan:** HIP8 Version of MSC8102, which is the MSC8122 device **Workaround:** Disable the bus monitor in systems where Address Retry cycles are used. **System Number:** 6997	1K94M
QSE31	**Use Only Compliant Arbiter** **Date Added:** 6/2002 **Description:** This is a compatibility note. An external arbiter must assert DBG in the same clock in which TS is asserted (there may be a one clock delay if the PPC_ACR[2]:DBGD bit is set. However, after reset, this bit is not set by default). Some external arbiters violate this requirement. As a result, the system hangs following the first bus access after reset. **Fix Plan:** HIP8 Version of MSC8102, which is the MSC8122 device **Workaround:** Use only a compliant external arbiter or the internal MSC8102 arbiter. **System Number:** 6998	1K94M
QSE32	**Error in Parity Operation when BRx[30]:DR = 1** **Date Added:** 6/2002 **Description:** When data pipeline mode is chosen and port size is less then 64bit, parity check will fail for read access of size bigger then the port size, on the second data beat (psdval). **Fix Plan:** HIP8 Version of MSC8102, which is the MSC8122 device **Workaround:** Use BRx[30]:DR = 0. **System Number:** 7570	1K94M

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QSE34	**Bus Busy Disable Mode Can Hang 60x Bus in Multi-Master Systems** **Date Added:** 6/2002 **Description:** The bus busy disable mode (SIUMCR[0]:BBD = 1) cannot be used if the MSC8102 is not the only master on the 60x system bus. Using this mode in such a system can cause the 60x bus to hang. **Fix Plan:** HIP8 Version of MSC8102, which is the MSC8122 device **Workaround:** 1. If the external master supports the $\overline{\text{ABB}}$ signal, do not use the bus busy disable mode and connect this signal to the MSC8102. The $\overline{\text{DBB}}$ signal can either be connected or can be pulled up. 2. If the external master does not support the $\overline{\text{ABB}}$ signal, do one of the following: a. Do not use the bus busy disable mode and generate the $\overline{\text{ABB}}$ signal externally. The $\overline{\text{DBB}}$ signal can either be connected or can be pulled up. The following external $\overline{\text{ABB}}$ implementation should be sufficient to work around the problem: Assert the $\overline{\text{ABB}}$ signal whenever a qualified bus grant for the external master is sampled (Bus grant asserted while $\overline{\text{ARTRY}}$ and $\overline{\text{ABB}}$ are negated). Negate the $\overline{\text{ABB}}$ signal when there is no qualified bus grant. The negation of $\overline{\text{ABB}}$ should be as follows: Drive $\overline{\text{ABB}}$ to VDD for half a clock cycle and then stop driving it (HIGH-Z). b. If the internal arbiter and up to two external masters are used, connect the external bus grants (through an AND gate if more than one) to an available external bus request and define the priority for that request to be the highest in the PPC_ALRH register. The $\overline{\text{DBB}}$ signal can either be connected or can be pulled up.	1K94M
QSE37	**Broadcast failure After Burst (64bit/sync mode)** **Description:** When a broadcast is performed before previous write burst data propogates to its target, it may cause an overflow of the write FIFO with no error indication in the DSI status bit of the DSI Error Register (DER). **Fix Plan:** HIP8 Version of MSC8102, which is the MSC8122 device **Workaround:** Do not perform a broadcast as the next access after a write burst. Perform another type of access in between. **System Number:** 7839	1K94M
QSE39	**Bus Monitor Stuck Pending for PSDVAL.** **Description:** When an extenal slave that does not use PSDVAL is accessed, if it returns $\overline{\text{TA}}$ on the same cycle that $\overline{\text{TS}}$ is asserted, then the bus monitor may be stuck, causing $\overline{\text{TEA}}$ after timeout. **Fix Plan:** HIP8 Version of MSC8102, which is the MSC8122 device **Workaround:** Disable the bus monitor (SYPCR[PBME]=0 in systems that have external slaves without PSDVAL or define a pipeline depth 1 (BCR[PLDP]=1) to avoid concurrent $\overline{\text{TA}}$ and $\overline{\text{TS}}$ **System Number:** 3759	1K94M
QSE40	**Device Withstands ESD CDM Stress of 400V Instead of 500V** **Device Withstands ESD MM Stress of 185V Instead of 200V** **Date Added:** 3/31/2004 **Description:** Device meets the ESD specifications for Human Body Model (HBM) of 1000V, but devices does not withstand Machine Model (MM) of 200V, and it does not withstand the Charged Device Model (CDM) of 500V. **Workaround:** N/A **System Number:**	1K94M

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