MSC7118 Device Errata for Mask 2M88B

ID Number	Errata	Product Affected
FS01	**Date Published:** 9/14/2005 **Description:** Under certain conditions, some DMA transfers from any internal memory to DDR using a TCD DSIZE value of 101 (32-byte transfers) may not function as expected and causes incorrect data to be written to external DDR memory. **Module(s) Affected:** DMA controller, DDR controller, memory controller interface (MCIF) **Impact:** Low **Workaround:** • Use a DSIZE value of 011 (8 byte transfers) when transferring data from internal memory to DDR. This workaround is not expected to have any performance impact. • Program the DDR controller SCFG[2TEN] bit to enable 2T timing (2TEN = 1). This workaround is expected to have a minor impact on performance. **Fix Plan:** None. **System Number:** None.	MSC7118
FS02	**Date Published:** 9/15/2005 **Description:** All SPI boot modes that use the PLL are unavailable. **Module(s) Affected:** Boot ROM, GPIO/SPI **Impact:** Medium **Workaround:** Use the SPI boot mode that configures the PLL to work in Bypass mode. **Fix Plan:** None. **System Number:**	1M88B

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FS04	**Date Published:** 12/15/2005 **Description:** The Instruction Fetch Unit will issue accesses on AMIC in response to a program miss that may not match the attributes (prefetch enable, primary set size, and burst size) defined in IRCR[0-3] for the corresponding region, when the icache regions are configured as follows. The number (0-3) corresponding to each enabled region is greater than the number (0-3) corresponding to each disabled region. Example1: region 0: enabled; region 1: disabled; region 2: disabled; region 3: enabled The issue occurs on a program miss to region 3. When this occurs, the cache parameters defined in IRCR1 are used instead of those defined in IRCR3. Example2: region 0: disabled; region 1: enabled; region 2: disabled; region 3: disabled The issue occurs on a program miss to region 1. When this occurs, the cache parameters defined in IRCR0 are used instead of those defined in IRCR1. This errata effects all 711x devices. **Module(s) Affected:** Instruction Fetch Unit **Impact:** Low **Workaround:** There are two workarounds available for this errata. Implementing either workaround is adequate for ensuring the issue does not occur. 1) The problematic icache region configuration can be avoided by ensuring that each enabled region number is less than each disabled region number. (i.e. All disabled regions are assigned to the most significant region numbers.) 2) Each region that is desired to be disabled should: be enabled (IRCR#[EN] = 1),have base address = $00000000, and have size = 64kB. **Fix Plan:** None **System Number:** None.	MSC7118

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SL23	**DMA Debug Mode Error** **Date Published:** 05/26/2005 **Description:** When a hardware-initiated DMA channel is running, data can become corrupted when the devices enters Device Debug mode and *all* of the following conditions are true: • The DMACR[EDBG] is set, so the DMA controller is programmed to stall when the device enters Device Debug mode. • The TCD7[BWC] bit field contains a value of either 10 or 11 to specify DMA stalls of either 4 or 8 cycles for that hardware channel. • The TCD1[SSIZE] < TCD2[NBYTES] for that hardware channel. • The TCD1[DSIZE] < TCD2[NBYTES] for that hardware channel. • The device enters Device Debug mode, placing the DMA controller into its debug mode. Under these conditions, the hardware peripheral may generate a double request for the same data. **Module(s) Affected:** DMA controller **Impact:** High **Workaround:** Because this is not typical usage for hardware-initiated DMA channels, the workaround is straightforward. When hardware-initiated DMA channels are in use, a fast response is desired, so the channel is typically programmed *without* DMA stalls. If you want to use the DMA Debug mode by setting the DMACR[EDBG] bit, you can set the channel for no stalls by assigning a value of either 00 or 01 to the TCD7[BWC] field of all hardware-initiated DMA channels. **Fix Plan:** None **System Number:** CDCpp49316 (SL) and CDCpp49317 (FS)	MSC7118

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