

MSC7118 Device Errata for Mask 2M88B

ID Number	Errata	Product Affected
FS01	<p>Date Published: 9/14/2005</p> <p>Description: Under certain conditions, some DMA transfers from any internal memory to DDR using a TCD DSIZE value of 101 (32-byte transfers) may not function as expected and causes incorrect data to be written to external DDR memory.</p> <p>Module(s) Affected: DMA controller, DDR controller, memory controller interface (MCIF)</p> <p>Impact: Low</p> <p>Workaround:</p> <ul style="list-style-type: none"> • Use a DSIZE value of 011 (8 byte transfers) when transferring data from internal memory to DDR. This workaround is not expected to have any performance impact. • Program the DDR controller SCFG[2TEN] bit to enable 2T timing (2TEN = 1). This workaround is expected to have a minor impact on performance. <p>Fix Plan: None.</p> <p>System Number: None.</p>	MSC7118
FS02	<p>Date Published: 9/15/2005</p> <p>Description: All SPI boot modes that use the PLL are unavailable.</p> <p>Module(s) Affected: Boot ROM, GPIO/SPI</p> <p>Impact: Medium</p> <p>Workaround: Use the SPI boot mode that configures the PLL to work in Bypass mode.</p> <p>Fix Plan: None.</p> <p>System Number:</p>	1M88B

ID Number	Errata	Product Affected
<p style="text-align: center;">FS04</p>	<p>Date Published: 12/15/2005</p> <p>Description: The Instruction Fetch Unit will issue accesses on AMIC in response to a program miss that may not match the attributes (prefetch enable, primary set size, and burst size) defined in IRCR[0-3] for the corresponding region, when the icache regions are configured as follows. The number (0-3) corresponding to each enabled region is greater than the number (0-3) corresponding to each disabled region.</p> <p>Example1: region 0: enabled; region 1: disabled; region 2: disabled; region 3: enabled The issue occurs on a program miss to region 3. When this occurs, the cache parameters defined in IRCR1 are used instead of those defined in IRCR3.</p> <p>Example2: region 0: disabled; region 1: enabled; region 2: disabled; region 3: disabled The issue occurs on a program miss to region 1. When this occurs, the cache parameters defined in IRCR0 are used instead of those defined in IRCR1.</p> <p>This errata effects all 711x devices.</p> <p>Module(s) Affected: Instruction Fetch Unit</p> <p>Impact: Low</p> <p>Workaround: There are two workarounds available for this errata. Implementing either workaround is adequate for ensuring the issue does not occur.</p> <p>1) The problematic icache region configuration can be avoided by ensuring that each enabled region number is less than each disabled region number. (i.e. All disabled regions are assigned to the most significant region numbers.)</p> <p>2) Each region that is desired to be disabled should: be enabled (IRCR#[EN] = 1), have base address = \$00000000, and have size = 64kB.</p> <p>Fix Plan: None</p> <p>System Number: None.</p>	<p>MSC7118</p>

ID Number	Errata	Product Affected
<p style="text-align: center;">SL23</p>	<p style="text-align: center;">DMA Debug Mode Error</p> <p>Date Published: 05/26/2005</p> <p>Description: When a hardware-initiated DMA channel is running, data can become corrupted when the device enters Device Debug mode and <i>all</i> of the following conditions are true:</p> <ul style="list-style-type: none"> • The DMACR[EDBG] is set, so the DMA controller is programmed to stall when the device enters Device Debug mode. • The TCD7[BWC] bit field contains a value of either 10 or 11 to specify DMA stalls of either 4 or 8 cycles for that hardware channel. • The TCD1[SSIZE] < TCD2[NBYTES] for that hardware channel. • The TCD1[DSIZE] < TCD2[NBYTES] for that hardware channel. • The device enters Device Debug mode, placing the DMA controller into its debug mode. <p>Under these conditions, the hardware peripheral may generate a double request for the same data.</p> <p>Module(s) Affected: DMA controller</p> <p>Impact: High</p> <p>Workaround: Because this is not typical usage for hardware-initiated DMA channels, the workaround is straightforward. When hardware-initiated DMA channels are in use, a fast response is desired, so the channel is typically programmed <i>without</i> DMA stalls. If you want to use the DMA Debug mode by setting the DMACR[EDBG] bit, you can set the channel for no stalls by assigning a value of either 00 or 01 to the TCD7[BWC] field of all hardware-initiated DMA channels.</p> <p>Fix Plan: None</p> <p>System Number: CDCpp49316 (SL) and CDCpp49317 (FS)</p>	<p style="text-align: center;">MSC7118</p>

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
+1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. StarCore is a licensed trademark of StarCore LLC. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2007, 2008.