Errata

MMC2114DE/D
Rev. 2, 5/2003

MMC2114 Device Errata

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This document identifies implementation differences between the MMC2114 and the description contained in the *MMC2114 Advance Information Reference Manual*. The errata items listed in this document (summarized in Table 1) describe differences from the following documents:

- *MMC2114 Advance Information Reference Manual*
- *M•CORE Programmer's Reference Manual*

Table 1. Summary of MMC2114 Errata

Errata ID	Errata Title	Mask Sets Affected	Date Errata Added
1	When operating in PLL 1:1 mode, disabling CLKOUT will unlock the PLL.	01K08Y 02K08Y	08 Oct 2002
2	RAM Standby mode does not function correctly.		
3	The PM bits in the OnCE OSR are incorrect for the STOP case.		
4	Unimplemented QADC port pins read 1s in the PORTQA/PORTQB registers instead of 0s.		
5	If Q1 is in any continuous conversion mode and Q2 is enabled, Q1 may sequence incorrectly and Q2 may be locked in the suspended state.		
6	Q1 may fail to retrigger if the CCW at the BOQ2 address contains the EOQ code.		
7	Flash command may be executed on the wrong bank if both banks are being programmed concurrently.		
8	Electrostatic discharge protection does not meet specified targets		
9	Write Collisions can occur even after SPIF is set for slower baud rates		06 Dec 2002
10	Program/Erase Interlock writes will set ACCERR when running out of a memory with > 1 waitstate		17 Apr 2003

Errata 1 When operating in PLL 1:1 mode, disabling CLKOUT will unlock the PLL

1.1 Description

Either of the following cases will kill the feedback source to the PLL, while running in PLL 1:1 mode, and the PLL will unlock:

- The DISCLK bit is set in the SYNCR
- The STMPD bits in the SYNCR are set to 01 and the stop instruction is executed

This will cause both the loss of clock and loss of lock conditions.

1.2 Workaround

If the CLKOUT disable feature is required in the application, use PLL normal mode. The feature works as specified in this mode.

Errata 2 RAM Standby mode does not function correctly

2.1 Description

An error in the VSTBY pin's ESD protection causes a diode to be forward biased from VSTBY to VDD in RAM Standby mode. This diode will cause VSTBY to power the rest of the chip in Standby mode, creating an additional 1–20mA of current on VSTBY in Standby mode.

2.2 Workaround

It may be possible to minimize the extra current by lowering the voltage on VSTBY to 2–2.2V.

Errata 3 The PM bits in the OnCE SR are incorrect for the STOP case

3.1 Description

The PM bits in the OnCE status register incorrectly read 00 when the CPU is in the STOP state. The PM bits correctly read 01 for the DOZE and WAIT states. Normally, entry into debug mode (when the processor is stopped) causes the CPU to wake up, and by the time the user can read the OSR, the state will indicate debug mode. The CPU can go back into STOP (via another stop instruction) only after running a “Go” + “Exit” command. In this case, the OSR[PM] will read 00 instead of 01 as specified.

Errata 4 Unimplemented QADC port pins in the PORTQA/PORTQB registers read 1s instead of 0s

4.1 Description

Unimplemented port pins in the PORTQA and PORTQB registers will always read 1s instead of the 0s specified in the manual. Analog-to-digital conversions on the unimplemented pins will still convert to the voltage on VSS.

4.2 Workaround

Don’t rely on the unimplemented bits that read 0 in the register.

Errata 5 If Q1 is in any continuous conversion mode and Q2 is enabled, Q1 may sequence incorrectly and Q2 may be locked into the suspended state

5.1 Description

This problem appears in the following circumstances:

- Q1 is in a continuous conversion mode
- Q2 is in the suspended state due to the triggering of Q1

The error causes Q1 to ignore an EOQ condition and it will repeatedly convert CCW1 to CCW(EOQ + 1) without a new trigger condition. At this point, Q2 will never finish and will be stuck in the suspended state.

5.2 Workaround

When Q2 is disabled, Q1 should be used only in a continuous conversion. Continuous modes can be emulated in software by using the single-scan modes and an interrupt handler to re-enable the Q1 trigger with the SSE1 bit.

Q1 can also be used in a continuous conversion mode if both of the following conditions are met:

- Q2 will always trigger after or at the same time as Q1
- Q2 will finish before Q1 is retriggered.

These conditions can be met with PIT triggering if the Q2 sequence is short compared to the PIT timeout. They might also be met using an external trigger if both external trigger sources are related.

Errata 6 Q1 may fail to retrigger if the CCW at the BOQ2 address contains the EOQ code

6.1 Description

Q1 may fail to retrigger under the following circumstances:

- The first CCW location of Q2 contains the EOQ code
- Q1 has just finished execution and Q2 is in the trigger pending state
- Q1 is retriggered just when Q2 begins to start

The error causes the Q1 trigger to be ignored.

6.2 Workaround

Do not put an EOQ code in the first CCW location of Q2 when Q2 is enabled. This is not recommended in any case, since Q2, which will have a zero length queue, will do nothing.

Errata 7 Flash command may be executed on the wrong bank if both banks are being programmed concurrently

7.1 Description

If a command starts on one bank (clear CBIEF) in the same cycle that a command finishes on another (CCIF goes high), then the command will be executed on the wrong bank.

7.2 Workaround

Program only one bank at a time, or be sure not to start commands when other banks are close to finishing.

Errata 8 Electrostatic discharge protection does not meet specified targets

8.1 Description

The electrostatic discharge (ESD) protection levels for device numbers XMC2114CFCPV33, MMC2114CFCPV33, XMC2114CFCPU33, MMC2114CFCPU33, XMC2114CFCVF33, MMC2114CFCVF33, XMC2113CFCPV33, MMC2113CFCPV33, XMC2113CFCPU33, MMC2113CFCPU33, XMC2113CFCVF33, and MMC2113CFCVF33 do not meet the specified ESD protection targets for human body model (HBM) and machine model (MM). The targets for HBM and MM protection are 2000V and 200V, respectively. The actual protection for HBM is 1000V and for MM, 50V.

8.2 Workaround

Proper handling methods should be observed to prevent damage to the device caused by electrostatic discharge.

Errata 9 Write collisions can occur even after SPIF is set for slower baud rates

9.1 Description

The SPIF bit is set on the last SCK edge of a transfer. Write collision detection occurs up to the negation of SS. Therefore, there is a 1/2 SCK time where a write to the data register can cause an inadvertent write collision during back-to-back transfers.

9.2 Workaround

Always check the WCOL bit after writing the data register. If it is set, then rewrite the data register with the desired value.

Alternatively, the user could wait for 1/2 SCK time between SPIF being set and writing the data register.

Errata 10 Program/Erase Interlock writes will set ACCERR when running out of a memory with > 1 waitstate

10.1 Description

If the cycle before a Flash interlock write contains waitstates > 1, then the interlock write will inadvertently set the ACCERR bit in the Flash user status register.

10.2 Workaround

The Flash program/erase code should reside in memories that use 0 or 1 waitstates. This is the case for the internal SRAM and Flash. If running out of external memory, then the memory must be fast enough to operate with 1 waitstate.

11 Revision History

Table 2 provides a revision history for this document.

Table 2. Document Revision History

Rev. No.	Substantive Changes	Date of Release
0	Initial Release	December 2002
1	Added MMC2114CFC*xxnn*/MMC2113CFC*xxnn* device numbers to Errata 8.	January 2003
1.1	Table 1: added “02K08Y” under “Masks Sets Affected.”	January 2003
2	Added Errata 9 and Errata 10.	May 2003

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