

# MCXC162VFT\_0P18R

## Mask Set Errata

Rev. 1.0 — 1 June 2026

Errata

## 1 Mask Set Errata for Mask 0P18R

### 1.1 Revision History

This report applies to mask 0P18R for these products:

- MCXC151VFT
- MCXC161VFT
- MCXC151VLF
- MCXC161VLF
- MCXC162VLF
- MCXC162VFT
- MCXC151VFG
- MCXC161VFG
- MCXC162VFG
- MCXC151VFK
- MCXC161VFK
- MCXC162VFK
- MCXC151VFM
- MCXC161VFM
- MCXC162VFM

Table 1. Revision History

| Revision | Release Date | Significant Changes |
|----------|--------------|---------------------|
| 1.0      | 6/2026       | Initial Revision    |

### 1.2 Summary of Arm Software Developers Errata Notice

This table summarizes all known Arm errata and lists the corresponding silicon revision level to which they apply. A 'Yes' entry indicates the erratum applies to a particular revision level, and a 'No' entry means it does not apply.

Table 2. Summary of Arm Software Developers Errata Notice

| SDEN ID        | Category | NXP Errata Number | Summary of Erratum                                                                                                                                                   | Silicon Rev. |
|----------------|----------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|
|                |          |                   |                                                                                                                                                                      | 1            |
| Arm Cortex-M23 |          |                   |                                                                                                                                                                      |              |
| 1078140        | CatC     | ERR053213         | Arm Errata 1078140 [Cortex-M23]: Cortex-M23 might not respond with DAP PWRUPACK for DAPPWRUPREQ, when DAPPWRUPREQ is asserted and debug domain is already powered up | Yes          |
| 2640347        | CatC     | ERR053214         | Arm Errata 2640347 [Cortex-M23]: Non-secure write to SHCSR.HARDFaultPENDED                                                                                           | Yes          |



Table 2. Summary of Arm Software Developers Errata Notice...continued

| SDEN ID | Category | NXP Errata Number | Summary of Erratum                                     | Silicon Rev. |
|---------|----------|-------------------|--------------------------------------------------------|--------------|
|         |          |                   |                                                        | 1            |
|         |          |                   | NS incorrectly updates state when AIRCR.BFHFNMINS is 0 |              |

1.3 Errata and Information Summary

Table 3. Errata and Information Summary

| Erratum ID                | Erratum Title                                                                                    |
|---------------------------|--------------------------------------------------------------------------------------------------|
| <a href="#">ERR053261</a> | LPI2C: Controller: Back-to-Back Read Command in Transmit FIFO does not work always               |
| <a href="#">ERR053423</a> | MCU can't wakeup from Sleep (CMC CKCTRL[CKMODE] = 1b), Deep Sleep, Power Down modes by interrupt |

## 2 Known Errata

### ERR053261: LPI2C: Controller: Back-to-Back Read Command in Transmit FIFO does not work always

#### Description

Transmit FIFO of LPI2C (accessed via MTDR register) stores command and data to initiate various I2C operations, similarly Receive FIFO (accessed via MRDR register) stores receive data during controller-receiver transfers. Ideally, LPI2C controller should stall the transfer by keeping SCL line low when the Receive FIFO is full, but this does not happen if the transmit FIFO is not empty and the next command is a READ, so the receive data is lost.

#### Workaround

Always interleave consecutive READ commands by any one of STOP, Start or Repeated Start command.

### ERR053423: MCU can't wakeup from Sleep (CMC CKCTRL[CKMODE] = 1b), Deep Sleep, Power Down modes by interrupt

#### Description

Due to different Wakeup Interrupt Controller (WIC) implementation on M23, MCU can't wakeup from Sleep (CMC CKCTRL[CKMODE] = 1b), Deep Sleep, Power Down modes by interrupt, while it can wakeup from Sleep (CMC CKCTRL[CKMODE] = 0b) and Deep Power Down modes.

#### Workaround

There're two methods to wakeup MCU as workaround.

1. Enable Core mode controller interrupt by enabling IRQ number 1, i.e. "enableIRQ(CMC\_IRQn);".

In this way, any interrupt can wakeup MCU from low power modes. Users need to disable the unwanted interrupts before entering low power modes. The RTC Time Invalid Flag/Interrupt is set by default, and it must be cleared to avoid blocking the SoC from entering low power mode when the CMC interrupt is enabled.

2. Set the given wakeup interrupt as Non-Maskable Interrupt (NMI) interrupt by setting NMISRC register, and enable NMI interrupt as wakeup source (enable SYSCON NMISRC[NMIENCPU0], CMC CORECTL[NPIE] and NMI interrupt in NVIC). In this way, NMI interrupt will wakeup MCU but users should be aware that it is NMI interrupt service routing instead of the normal ISR.

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