

MCXA346VLQ_0P89K

Mask Set Errata

Rev. 1.0 — 19 August 2025

Errata

1 Mask Set Errata for Mask 0P89K

1.1 Revision History

This report applies to mask 0P89K for these products:

- MCXA346VLQ
- MCXA345VPN
- MCXA345VLQ
- MCXA345VLL
- MCXA345VLH
- MCXA346VPN
- MCXA346VLL
- MCXA346VLH

Table 1. Revision History

Revision	Release Date	Significant Changes
1.0	8/2025	Initial Revision

1.2 Errata and Information Summary

Table 2. Errata and Information Summary

Erratum ID	Erratum Title
ERR050501	Core: DFSR.EXTERNAL is not set correctly when waking up from sleep
ERR050502	Core: Execution priority might be wrong for one cycle after AIRCR is changed
ERR051588	LPSPi:Reset transmit FIFO after FIFO underrun by LPSPi Slave.
ERR051728	Arm Errata 1080541: [Cortex-M33] Access permission faults are prioritized over unaligned Device memory faults
ERR051731	Arm Errata 1435973: [Cortex-M33] Execution priority might be wrong for one cycle after AIRCR, NVIC_ITNS, NVIC_IPR, NVIC_ISER, or NVIC_ICER is changed
ERR051734	Core: DWT comparator match on cycle count is not reported to the ETM if there is no instruction executing on the processor
ERR052343	I3C: Target Early Termination Feature not available with DMA controller
ERR052558	FlexCAN: Message buffer (MB) overrun status is cleared when reading Enhanced RX FIFO (ERF)



2 Known Errata

ERR050501: Core: DFSR.EXTERNAL is not set correctly when waking up from sleep

Description

Cortex-M33 1367266-C:

An external debug event which causes the processor to enter Debug state or the debug monitor should set DFSR.EXTERNAL. It has been found that this field is not set if the event occurs while the processor is asleep.

Workaround

There is no workaround.

ERR050502: Core: Execution priority might be wrong for one cycle after AIRCR is changed

Description

Cortex-M33 1435973-C:

AIRCR is used in the NVIC active tree to calculate the execution priority, which in turn is used to determine fault escalation, exception preemption, and other NVIC-related behaviors. When the active tree is pipelined and there are high latency IRQs active, there might be a glitch in the active tree output for one cycle after AIRCR is changed. The glitch results in NVIC producing wrong execution priority that is neither based on the old AIRCR value nor the new one.

Workaround

There is no workaround for this erratum.

ERR051588: LPSPI:Reset transmit FIFO after FIFO underrun by LPSPI Slave.

Description

Transmit FIFO pointers are corrupted when a transmit FIFO underrun occurs (SR[TEF]) in slave mode.

Workaround

When clearing the transmit error flag (SR[TEF] = 0b1) following a transmit FIFO underrun, reset the transmit FIFO (CR[RTEF] = 0b1) before writing any new data to the transmit FIFO.

ERR051728: Arm Errata 1080541: [Cortex-M33] Access permission faults are prioritized over unaligned Device memory faults

Description

Affects: Cortex-M33

Fault Type: Programmer Category C

Fault Status: Present in r0p0, r0p1, r0p2, r0p3, r0p4, and r1p0. Open.

A load or store which causes an unaligned access to Device memory will result in an UNALIGNED UsageFault exception. However, if the region is not accessible because of the MPU access permissions (as specified in MPU_RBAR.AP), then the resulting MemManage fault will be prioritized over the UsageFault.

Workaround

There is no workaround.

However, it is expected that no existing software is relying on this behavior since it was permitted in Armv7-M.

ERR051731: Arm Errata 1435973: [Cortex-M33] Execution priority might be wrong for one cycle after AIRCR, NVIC_ITNS, NVIC_IPR, NVIC_ISER, or NVIC_ICER is changed

Description

Affects: Cortex-M33

Fault Type: Programmer Category C

Fault Status: Present in r0p0, r0p1, r0p2, r0p3, r0p4, and r1p0. Open.

Programmable registers are used in the Nested Vectored Interrupt Controller (NVIC) to determine execution priority, interrupt priority, and in turn exception pre-emption, fault escalation and other NVIC behavior.

As a result of this erratum, when at least one interrupt is configured as higher-priority and specific programmable register values are changed, there is a one-cycle window where execution and interrupt priority might be wrong, leading to incorrect NVIC behavior such as exception pre-emption and fault escalation.

Workaround

There is no workaround for this erratum.

Typical applications do not need a workaround for this erratum because registers related to interrupt priority are typically programmed during boot-up and then remain static.

The UFRDY bits in FPCCR might be wrong when the write to the NVIC-related register is followed immediately by a VLSTM instruction.

Instruction stepping, asynchronous debug events, and breakpoints might be incorrectly triggered or missed in the cycle after the write to the NVIC-related register.

ERR051734: Core: DWT comparator match on cycle count is not reported to the ETM if there is no instruction executing on the processor**Description**

Cortex-M33 2435965-C

The Cortex-M33 Data Watchpoint and Trace (DWT) unit supports a Cycle count match event which can be used to trigger the Embedded Trace Macrocell (ETM) to generate a trace packet from the processor. Due to this erratum the event signal is only propagated when an instruction is executing in the pipeline and so no event will be transferred to the ETM if the processor is idle.

Workaround

There is no workaround for this erratum, however, non-debug operation of the core is not affected.

ERR052343: I3C: Target Early Termination Feature not available with DMA controller**Description**

The indication of Early read termination by I3C Target is reflected by register status and interrupt in I3C Controller. Due to custom interface of DMA controller

this pre-mature termination information is not propagated to it consequently the partial data is not transfer into memory in case of Early termination by Target.

So, Early termination cannot be used with this DMA controller for I3C.

Workaround

- 1) If DMA is used, do not use Target Early termination feature. Instead use smaller data size which is guaranteed to be arranged by Target always and early termination will never occur.
- 2) Do not use DMA , use Host to do all transfers and handle Early termination by ISR or by polling of status method.

ERR052558: FlexCAN: Message buffer (MB) overrun status is cleared when reading Enhanced RX FIFO (ERF)**Description**

Message buffer status becomes "full" when a frame arrives, and status becomes "overrun" when a second message arrives in the same message buffer, if first message has still not been read. If frame reception is happening in ERF and the frame is being read from ERF, these reads could incorrectly clear the MB overrun status. As a result, the overrun event can be missed by the application.

Workaround

Use one of the following workarounds:

Workaround #1: Don't use Enhanced RX FIFO (ERF).

Workaround #2: Don't use any of the message buffers from MB0 to MB7 for reception if ERF is enabled. MB0 to MB7 can be used for transmission.

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