Chip Errata

MC68SZ3280L95JCE/D
Rev. 1.2, 3/2004

MC68SZ328 Integrated Processor (DragonBall™): 0L95J Mask

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This document details silicon errata information for the 0L95J mask of the MC68SZ328 (Dragonball™ Super VZ) integrated processor.

Erratum Number 6 has been updated since the last release of this document (Rev 1.1).

Table 1. Silicon Errata to MC68SZ328 (OL95J Mask)

Erratum Number	Erratum Description	Impact, Workaround, and Fix Status
1.	**Module: Chip-Select** **Early Cycle Detection function for Dynamic Memory (SDRAM and EDO DRAM)** The chip-select module fails to support the early cycle detection function for Dynamic Memory: Program the ECDD bit of chip-select control register 2 (0xFFFFF10C) to 1. In this case, SDRAM and EDO memory access cycle cannot be further reduced by one wait state.	**Impact**: There is no impact. This function is originally designed to further enhance the DRAM access performance. **Workaround**: There is no workaround for this issue. **Fix status:** The root cause of this design bug has been identified. No solution is available.
2.	**Module: ASP** At QVDD=1.8V, the ADC can only guarantee 8-bit accuracy.	**Impact**: The maximum resolution that can be provided to touch the panel application is 256 x 256 (pixel). **Workaround**: There is no workaround for this issue. **Fix status:** No solution is available.
3.	**Module: ASP** **The maximum input voltage of U analog input cannot be higher than QVDD (Typical: 1.8 V).** If U input is higher than QVDD, it introduces unexpected current offset to Pen ADC during X and Y sampling and affects the accuracy of digital data output.	**Impact**: Some applications such as battery measurement cannot be implemented by using direct connection of voltage output to U input. A potential divider is needed to limit the voltage range. **Workaround**: It is advised to limit the U channel input voltage to the range from 0 V to QVDD. This can be done by using potential divider circuitry. **Fix status:** The root cause of this design bug has been identified. No solution is available.

Table 1. Silicon Errata to MC68SZ328 (OL95J Mask) (Continued)

Erratum Number	Erratum Description	Impact, Workaround, and Fix Status
4.	**Module: USBD and DMA** **Data corruption/loss occurs when doing a DMA transfer with the USB module with the EOBE bit (in the I/O channel control register) enabled for packet size of 32/64 bytes.**	**Impact:** Because the end-of-burst operation cannot be used in DMAC when enabled, the size of the OUT (from the host to the device) transfer and DMA burst length must already be defined rather than be controlled automatically by the USBD. **Workaround**: The workaround is to disable the EOB mechanism and use regular DMA transfer mode. In addition, the FIFO alarm must be set properly (so that both the EOF and the FIFO alarm generate a request to the DMA). To use the regular DMA transfer mode with the USB module, it is advised to: 1) Clear the EOBE bit in the I/O channel control register. 2) Set the burst length to packet size. 3) Set the DMA count to the total number of bytes to be transferred. 4) Set the USB_EPn_FALRM register of the USB module to the value of the FIFO size—packet size (for example, if you use a FIFO of size 128 and packet size is 32, the register should be set to 128-32=96). **Fix status:** The root cause of this design bug is being investigated.
5.	**Module: DMA** **Cannot use the DMA to do transfers when using an external DTACK signal on the same chip-select.**	**Impact:** When the DMA is set to transfer data and the chip-select for that channel is set to use an external DTACK signal, the chip-select signal will assert during the DMA transfer but it will never de-assert. **Workaround**: Use the CPU instead of using DMA to do transfers between peripheral and memory when using an external DTACK signal for that particular chip-select. **Fix status:** The root cause of this design bug has been identified. No solution is available.
6.	**Module: LCDC** **VGA resolution cannot be supported.**	**Impact:** Flickering may be noticed when running an image at 640 x 480 resolution. **Workaround**: There is no workaround for this issue. **Fix status:** The root cause of this design bug has been identified. No solution is available.

Table 1. Silicon Errata to MC68SZ328 (OL95J Mask) (Continued)

Erratum Number	Erratum Description	Impact, Workaround, and Fix Status
7.	**Module: SDRAMC** **Failure to send a self refresh command to the SDRAM before the processor goes into sleep mode.**	**Impact:** At times the SDRAM controller will not send self-refresh commands to the SDRAM before the processor goes into sleep mode. This will cause data loss since the SDRAM will not be able to refresh. **Workaround**: A software workaround has been implemented to bypass this issue. Please refer application note, AN2550, for details on the workaround. **Fix status:** The root cause of this design bug has been identified. No solution is available.
8.	**Module: ASP** **The Enhanced ADC is dependant on ambient temperature.**	**Impact:** The accuracy of the EADC can be compromised since it cannot compensate over temperature. **Workaround**: There is no workaround for this issue. **Fix status:** The root cause of this design bug has been identified. No solution is available.

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