



REVISION C CHANGES

February 27, 1997

68PM302 INTEGRATED MULTIPROTOCOL PROCESSOR DEVICES

This document covers the 68PM302 Revision C.1, Mask 1F85S. Some minor new features have been added to the 68PM302 Revision C device. These new features are not required to be used, and the revision C device is fully compatible with the revision B device. The main purpose of the revision C device is to allow the use of a 32Khz crystal with the on-chip PLL. Revision C is visually labeled with mask number 1F85S.

NOTE: The following information is not described in the MC68PM302 Reference Manual. However, the use of that manual, plus this document, will fully describe revision C device operation.

1. Use of 32Khz crystal with on-chip PLL

On previous versions of the PM302 (Rev A and B), users were unable to use a 32KHz crystal with the on-chip PLL due to excessive jitter. This has been fixed on Rev C by rerouting the pins, **ONLY** when using 32KHz mode. When using any other mode, the PM302 pinout does not change, and remains as it was on Rev B. When using the 32KHz mode on Rev C, follow these instructions:

1. Signal PC_A4 from the PCMCIA connector is connected to pin NC1.
2. Signal PC_A5 from the PCMCIA connector is connected to pin NC2.
3. Pin PC_A4 (next to XTAL) on the chip should be grounded.
4. Pin PC_A5 (next to XTAL) on the chip should be grounded.
5. The serial resistor between XTAL and the Crystal changes to 1K Ohms. Capacitors between the Crystal and GND are 10 pf.

Notes: Changes 3,4 (grounding the pins) are not mandatory, but helped a lot in our environment. Changes 5,6 (different caps and resistors) helped in our environment, but they depend on the layout of the board and the crystal used. Once again, these changes only occur when using the 32KHz crystal mode of the PLL.

2. Errata Fixes

Most rev B errata are fixed in rev C. See the MC68PM302 revision C device errata sheet for details. An errata sheet also exists for the MC68PM302 Reference Manual.



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