DEVICE ERRATA

October 28, 1996

68PM302 INTEGRATED MULTIPROTOCOL PROCESSOR DEVICES

This document covers the XC68PM302 Mask 1F80S. Errata listed in italics and which have change bars are new since the last published errata.

1. Use of 32KHz crystal with on-chip PLL

Using a 32KHz crystal or external oscillator with the onchip PLL may generate an unreliable clock signal to the chip. The CLKO signal may jitter or stop toggling when the PC_A4 or PC_A5 address lines change state. This problem is mostly seen when PC_EN=1 and the PC host does not disable the address buffers to the card for accesses not addressed to the card. This bug will be fixed in Rev C silicon (Mask F85S).

Workaround: Use a 4MHz crystal in place of the 32KHz crystal.

2. Low Power modes current drain

In PC Enabled mode (PC_EN=1), if PA13 is programmed as an input there is a floating node intthe silicon which can draw about 0.5mA of current. This will be fixed in Rev C (Mask F85S).

Workaround: If PC_EN=1, program PA13 as an output.

3. *Assertion of HALT by an external master during Low Power results in a contention on the address bus when the chip resumes operation.*

Workaround: Do not assert HALT in an attempt to acquire the bus while in low power modes. This will be fixed in Rev. C.

4. 16650 Break Indication

The 68PM302 16550 emulation of the following sequence is incorrect.

1. long break -> BRK bit in LSR is set
2. idle (during this period, the PC reads the LSR register and BRK bit is reset)
3. long break -> BRK bit in LSR is set again.

The actual 16550 will indicate break twice.

This sequence is emulated on the 68PM302 by the following sequence:

1. Stop Transmit Command by the 68k -> BRK bit in LSR is set
2. Restart Transmit Command by the 68k but no data to transmit -> wait idle period (during this period the PC reads the LSR register and BRK bit is reset)
3. Stop Transmit Command -> BRK bit in LSR is NOT set again !

The 68PM302's16550 emulator will indicate break only once. That's because between the two Stop Transmit Commands no data was transmitted. The 68PM302 'sees' this sequence as one long Stop Transmit Command (break).

5. PCMCIA Fast Read cycles

Timing spec 332 (shown in Figure 7-25 of the 68PM302 Addendum) is not accurate. Spec 332 is 68K Data Bus Valid to PC_Data Bus Valid and is specified to be 25 nS. This is not always the case.

D15-D0 is sampled with CLKO HIGH. Timing 332 is applicable if D15-D0 is valid in the time window of 10ns before the rising edge of CLKO and 10ns before the falling edge of CLKO. If D15-D0 is valid any other time, add to spec 332 the time elapsed until 10ns before rising edge of CLKO.

This will be fixed in Revision C.

6. Interrupt Vectors in Slave Mode

If the 68PM302 is used in slave mode with the PCMCIA disabled or in the PGA package (conditions where the function code pins, FC2-0, are available), **AND** and an external asynchronous master is used **AND** the external master has not performed an internal read cycle since the previous IACK cycle, then during the current IACK cycle, the 68PM302 will drive the previous interrupt vector and the IPR and ISR registers will not be updated.

Workaround: The user should perform an internal read cycle (i.e. read the IPR or ISR or any other internal register) during the Interrupt routine. This will be fixed in Rev. C.

7. Very Short Frames in Synchronous Protocols

If a 68PM302 SCC is used in a synchronous protocol mode (HDLC, BISYNC, or Transparent), AND the transmit frame is stored in just one data buffer, AND the transmit frame is only 1 or 2 bytes in total length (i.e. 1 or 2 bytes stored in the data buffer) AND more than one 68PM302 SCC is operating simultaneously,

it is possible after some amount of time (minutes, hours, or days) for a frame to be reported as being transmitted successfully (i.e. the Tx BD shows that it has been transmitted without errors), but in reality, the frame was not transmitted over the TXD pin.

Workarounds:

1. In the case of transmitting a two byte frame, simply split the frame into 2 one-byte buffers. This will eliminate the problem, and will not affect serial performance.

2. Do nothing. Since the problem occurs very rarely, wait for the missing frame to be detected by the higher layers of the software, and a retransmission requested.