Preliminary

Release Notes

MC68EZ328 - DragonBall™-EZ Masket 1J75C

This document covers errata information which relates to the maskset 1J75C of the DragonBall-EZ MC68EZ328.

1. Items 2,3,4,5,9,11 in Maskset J75C errata has been fixed.

2. Bit 0 of DRAMCONT ($FFFC02) becomes write only bit. Cannot be read.

This is will modify in future version of User's Manual.

3. On DRAM page mode, an intermittent suprious 68K data read is found at the end of LCD DMA cycle.

A timing problem has been identified. For current maskset, it is recommended user to use EDO mode for DRAM. This will be corrected in the all layer fix.

4. Zero wait state 68K access to DRAM may cause data corruption and spurious data reading. Some extra small pulses can be seen on signal RAS0 and RAS1. This does not appear all the time.

For current maskset, it is recommended not to use 0 ws for 68K DRAM access. This item will be corrected with all layer fix.

5. DMA data of beginning of each line maybe incorrect when use LCD screen panning feature.

It is due to the fact that RAS address does not change when starting a non-consecutive new line of pixel. This item will be corrected with all layer fix.

6. Address to CAS setup time is negative for some address values at a lower voltage.

Increased address driver of EZ328 in 1J75C. The setup time is now improve to 10-12ns. However, it is still recommended to set MUX-SLOW bit of DRAM control register, which insert one clock before CAS asserts. This item will be fixed in all layer fix.

7. LCD contrast control multfuction when the last write to any LCD internal register is odd vaule. This does not affect the other functions of LCD controller.

Work-around: Perform an extra "00" data byte write to LCD unused register, e.g. $FFFA40.

8. Pin PE3/UCLK/DWE cannot be configured to UCLK function.

Work-around: No.

9. In EDO mode, pixel shifts at page switching at a lower voltage level.

Work-around: Adjust VDD to above 3.6V, or use PLL VCO frequency less than 13MHz.

Freescale Semiconductor, Inc.
ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

SEMICONDUCTOR PRODUCT INFORMATION

For More Information On This Product,
Go to: www.freescale.com