68840 IFDDI (0C67T) ERRATA

(June 13, 1995)

The 0C67T mask conforms with the full specification of the 68840, with the following exceptions.

1. The internal pull down for the DA pin is not functional.

Workaround

The DA pin should be connected during power up reset to GND or Vcc in order to define the 68840 in either IFDDI-mode or FSI-mode. The pin may be driven high by connecting a 1.3K pull up resistor, or driven low by connecting a 1K pull down resistor. It is recommended that a pin is not driven with a register but with a driver to reduce power consumption.

2. Short Frame Storm Reception

When the IFDDI is bombarded with short frames and the bus latency is such that an overrun condition occurs, a memory overrun (MOV) may also occur. When receiving very small frames (17-20 bytes), the interval between frame reception and the FSI core asserting RABORT is such that the MAC core receives the RABORT signal after the frame has already been sent to the FSI core. Therefore, a receive overrun condition may eventually result in internal memory being overrun if the IFDDI cannot transfer the shorter frames to system memory. To recover, perform a software reset from the FSI Control Register (FCR).

3. Ring State Machine transition to COMPLETE

In very rare cases the Transmit Ring State Machine does not transition to the COMPLETE state. In this situation, performing a Define Ring command on an already defined ring may lock the ring operation.

Workaround

Issue a Ring Reset command previous to the Define Ring command.

4. Other Port's Address in Pipeline Mode

When using non-multiplexed pipeline operation, connecting the AREADY to the BREADY pin will cause the address counter on the BDATA lines to not increment following the first address read. This is only neccesary in situations when a DMA transfer occurs from the IFDDI to RAM. Note that this workaround will be compatible with later revisions that do not contain this bug.

Workaround

Use an external register to latch the first address provided on BDATA. This will also delay BREADY from AREADY by one clock.

5. 68840 PNOP to NOP transition drives data bus

When the bus controller changes the CNTL lines from a PNOP to a NOP, switching the operating mode from pipeline to normal mode, on the first cycle after this transition, the 840 will

drive the data and parity buses for one clock regardless of the state of the R/W line.

Option 1:
The first bus cycle in which the CNTL lines transition from PNOP to NOP must be a "dummy" read cycle with the R/W line set equal to 1 assuring that any other device that might drive the data bus is forced into a tristate position during the first NOP cycle.

Option 2:

Using this workaround, it is assumed that the default mode when using both pipemode and normal mode in the same implementation is normal mode.

Each time the controller receives a request from the IFDDI, the controller moves to pipemode via PNOP, and then issues the burst.
When the REQ lines have negated, the design then returns to normal mode via a NOP access. At this time, the IFDDI drives the bus due to this errata, but the processor does not since the controller returns the bus to the processor (bus grant) only after the transfer cycle to normal mode has been completed. At this point the processor can read/write the IFDDI registers until the next DMA burst is requested.

The advantage of Option 2, is that only the controller hardware is affected by the errata while the software remains the same.
The PNOP to NOP cycle is a lost cycle, but occurs for 1 or multiple data bursts, and not on register accesses. This workaround will work with the fixed revision as well.

7. Erroneous SI_ERR Interrupt in MAC

If MAC_ON is asserted while the MACIF is attempting to transmit frames, the SI_ERR interrupt may be erroneously set. All other operations function correctly since there is no interface error, in spite of the interrupt. This situation can occur whether the PSF is used or bypassed, but the probability that it will occur is larger if the PSF is used (non-bypass).

Workarounds
Option 1:
Mask out the SI_ERR bit as there is no bus between the FSI and MAC cores which is visable to the user

Option 2:
Mask out the SI_ERR bit before asserting MAC_ON if the MACIF transmission is enabled (TE bit in MTR is set.)

Option 3:
Disable the MACIF transmission when MAC_ON is reset, and enable the tranmission only after MAC_ON has been set. Note that this option has ramifications at the system level since leaving the MACIF enabled aborts each frame continuously clearing the transmit ring. If the MACIF is disabled, the transmit frames will remain in the transmit ring and will be transmitted

later.