68839 FSI (0C66T) ERRATA

(October 14, 1993)

The 0C66T mask conforms with the full specification of the 68839, with the following exceptions.

1. Erroneous ROV error in Local Memory Mode

(previously titled "Receive Overrun error in receive Auto channel")

When the FSI is receiving in Local Memory mode, a Receive overrun Error (ROV4 or ROV5) may occur without exceeding the RMR value.

Workaround

1) Do not issue Port Operation Error (POE) on the Local Memory Port
2) Do not issue Abort Access on the Local Memory Port
3) Disable parity check on Receive Local Memory (i.e. set LPE to "0" on SPR4 and SPR5).

2. PER field problem in DMA Error Indications

The PER field in DMA Error Indications (Primary and Secondary) may specify the wrong error reason. Note that this error may occur only in Port to Port operation.

3. Receive Overrun error in Local Memory Mode

A lock-up situation may occur when ROV4 or ROV5 occurs. To eliminate the possibility of lock-up the following steps should be taken:

1) Disable the reception by resetting the Receive Enable (RE) bit in the Macif Receive Register (MRR).
2) Issue a Ring Reset command to the receive channel the ROV has occurred on.
3) Reset the ROV4 or ROV5 in the Status Register 1 (SR1).
4) Re-define the channel (Ring 4 or Ring 5) using a Define Ring command.
5) Enable the channel reception (set the RE bit in the MRR)

If Split Header mode is used, and the body of the frame is directed to Ring 5, when the Receive Overrun Error occurs, the following steps should be taken to avoid a lock-up situation:

1) Disable the reception - reset RE5 and RE4 in the MRR register
2) Issue a Ring Reset command to the receive channels (Ring 4 AND Ring 5)
3) Reset the ROV (ROV4 or ROV5) in Status Register 1 (SR1).
4) Re-define the receive channels (Ring 4 AND Ring 5) using a Define Ring command.

5) Enable the receive channels (Ring 4 AND Ring 5) by setting RE4 and RE5 in the MRR.

4. Delayed Indication in Receive Channel Split Header Mode

The FSI does not mark the "header" indication as an error indication when the Body indication is marked with an error indication.

5. Stop Transmit Ring/Ring Reset command in an endless loop transmission

A lock-up situation may occur when issuing a Stop Transmit Ring command or a Ring Reset command to a transmit ring that transmits an endless loop of descriptors as in the case of Directed Beaconing. To avoid a lock-up situation:

1) Disable the transmit channel transmission by setting the appropriate TR bit in the MTR, do not reset the TE bit in the MTR.
2) Issue the Stop Transmit Ring command or the Ring Reset command.
3) Redefine the ring used for beaconing previous to beginning another beaconing process

6. Discard Option in Receive or Destination Buffer Descriptor

When using the Discard Option in Receive or Destination Buffer Descriptors, misleading indications may be generated.

1) In a Receive or DMA Indication, bits 59:56 are set to 1001, and the PER field is meaningless. Bit 0 remains set identifying it as a "frame discard"
2) In a DMA source Indication, the ER bit is set and the PER field is meaningless.

7. Short Frame Storm Reception

When the FSI is bombarded with short frames and the bus latency is such that an overrun condition occurs, a memory overrun (MOV) may also occur. When receiving very small frames (17-20 bytes), the interval between frame reception and the FSI asserting RABORT is such that the MAC receives the RABORT signal after the frame has already been sent to the FSI. Therefore, a receive overrun condition may eventually result in internal memory being overrun if the FSI cannot transfer the shorter frames to system memory. To recover, perform a software reset from the FSI Control Register (FCR).

8. Ring State Machine transition to COMPLETE

In very rare cases the Ring State Machine may not transition to the COMPLETE state. In this situation, issuing a Define Ring command on an already defined ring may lock the ring operation.

Workaround

Previous to issuing a Define Ring command, issue a Ring Reset Command.

Notes:
1. All No Connect (NC) pins should be grounded.
2. Three pins are now open drain requiring a pull-up resistor on each pin. They are: AINT*, BINT* and MATCHO*.