Chip Errata
68341 Integrated Processor
3/28/96

This errata list applies to the following 68341 mask sets:

Mask	Processing Geometry	Part Number Suffix
E10K		"0"
E41R	0.8u	(none)
0F23F	0.65u	(none)

The mask set for each part is encoded into the device topside markings - for example, the following markings would indicate a device from the E41R mask, manufactured in the 12th week of 1994:

XC68341FT16
E41R
QEAQ9412

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E10K
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1. **Programmable Interrupt Register:** It is not possible to write the PIR. The PIR is used to enable the edge triggered interrupts, therefore only level sensitive interrupts are available. Micrion FIB fix has proven edge triggered interrupts.

2. **Real Time Clock:** The Real time clock module does not function.

   a) Register write and reset race condition; decal has been used to find additional races.

   b) RTCOUT, which is muxed with RMC, does not drive out when part is operated off battery supply.

   c) Power issues: RTC battery operation consumes 900uA, expected 10uA.

   d) Vbat provides power to VDD.

3. **DMA handshaking using RDYx signals:** This feature is not functional and should not be enabled. Setting PPARC bits 7 or 8 (to enable RDY1 or RDY2) will cause the next external bus cycle to hang waiting for RDYx, whether it is a CPU or DMA initiated bus cycle.

4. **QSM JTAG output enable:** The QSM pins come out of reset as inputs. There is no mechanism to force the pad drivers to be outputs during JTAG EXTEST. The fix is to add a JTAG control bit to each QSM output driver.

5. **TCLK Vil:** TCLK Vil is out of specification. TCLK must be driven to 0.1V for a logic zero to be asserted.

6. **BKPT and IFETCH synchronization:** BKPT and IFETCH are synchronized on the wrong clock edge. Their timing is inconsistent with the data sheet specification for these signals. This errata will affect only the design of emulation systems that use background debug mode.

7. **MOVEM instruction:** If the DMA is set for cycle steal and a DMA request occurs slightly before the last register move of a MOVEM instruction, data corruption occurs on the MOVEM data.

8. **Low frequency CPU32 STOP instruction:** At low frequencies, when the CPU executes a STOP instruction, power consumption actually increases by about 1mA instead of decreasing.

9. **Loss of crystal without limp mode operation:** At cold temperatures and in some corners of the manufacturing window, if the crystal oscillator stops oscillating, it is possible that the part will not enter limp mode operation and will cease to operate.

10. **VDDSYN supplies power to VDD:** If VDDSYN is powered (to operate the VCO/PLL), and the device is put into Low Power STOP operation, VDD must also remain powered, otherwise VDDSYN will supply power to VDD.

11. **SERIAL X1:** Frequency limits the minimum CPU frequency of operation.

12. **RDY1 and RDY2 oring:** RDY1 and RDY2 are not mapped to their respective DMA channels. RDY1 and RDY2 are logically ored together and assertion of either RDY pin will signal a ready condition to the active DMA channel.

13. **RDY with internal terminations:** The RDY pins will not inhibit internal bus termination.

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E41R
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1. **SIM LPSTOP and External Clock with VCO:** When using external clock with VCO mode, the CPU will not reliably exit LPSTOP if the SYNCR is programmed to turn off the VCO when in LPSTOP.

   Workaround: Program the SYNCR to enable the VCO in LPSTOP.

2. **SIM LOC:** Loss of Clock without Limp Mode Ñ If a loss of clock occurs while the VCO is set to a low operating frequency (131 KHz), the part may lock up and not enter limp mode.

3. **SIM POR with RTC:** When operating with a battery-backed RTC, the built-in POR delay of 328 input clocks may be insufficient for slower VCC rise times (>10ms with a 32KHz crystal).

   Workaround: Use an external power-on reset circuit. (The revised silicon will delay exit from reset until negation of BSW).

4. **SIM RMC/RTCOUT contention:** If RMC/RTCOUT is configured as RMC, and an RMC cycle (resulting from execution of a TAS instruction) is in progress when BSW is asserted, the weak internal RTCOUT pullup transistor will turn on, resulting in contention with the RMC pulldown. Note the RTCOUT pullup is current limited, restricting the resulting current flow to ~20ua.

   Workaround: This scenario typically would occur only on powerdown. Avoid by configuring RMC/RTCOUT as RTCOUT, or don't use TAS instructions.

5. **DMA Early Termination:** If CCR2 is written and BTC2 <= $0000 000F, and a request is pending for channel 1 and the BTC1 value following the transfer will be $xxxx xxx0, then channel 1 may terminate early after completion of the pending transfer. DONE1 (for external request modes) asserts for the transfer and the DONE flag in CSR1 is set.

   Workarounds:

   1) Avoid starting or stopping channel 2 with byte counts less than $10 if channel 1 is active.

   2) Disable channel 1 activity while writing CSR2. This can be done in software by raising the interrupt mask in the CPU32+'s SR register above the ISM level in the DMA MCR register.

   3) If the device connected to channel 1 can ignore the early DONE1 assertion, reset CSR1 and set the CCR1 start bit to restart the channel.

6. **DMA Configuration Error:** If a pending interrupt or an increase in the CPU status register interrupt priority mask bits forces DMA channel 2 off the bus in the middle of a multi-cycle DMA transfer (e.g. dual address), and the CCR1 STR bit is then set to start channel 1, a channel 1 configuration error will result.

   Workarounds:

   1) Select a channel 2 ISM value which prevents stopping channel 2 when channel 1 is to be initialized. In general, channel 2's ISM should be greater than or equal to channel 1's interrupt level (or any other interrupt source which vectors to code used to initialize channel 1). Setting channel 2's ISM to 7 avoids the problem entirely.

   2) Use channel 2 only for single address transfers.

7. **DMA DONEx Input:** In dual-address mode, if DONEx is asserted by an external device to stop the channel, only the read portion of the last transfer will complete.

   Workaround: Instead of asserting DONEx to stop the channel and cause the DMA to generate an interrupt, assert an interrupt directly on one of the processor IRQx inputs. The interrupt sevice routine can then explicitly stop the channel by clearing the start bit in the channel's DMACCR register.

8. **DMA Bus Error:** If the last transfer of a DMA module bus tenure is terminated with an externally generated bus error, the following CPU bus cycle may not be internally terminated by the SIM, or may be bus errored. An internal BERR assertion by the SIM's bus timeout circuit does not cause this problem.

9. **QSPM input buffers:** LPSTOP does not disable the QSPM input buffers - floating or high QSPM inputs during LPSTOP will result in higher ICC current. LPSTOP current can be minimized by tying unused QSPM inputs to ground during LPSTOP. The QSPM inputs are tested to VILmax=0.1*VCC vs. the spec limit of VILmax=0.2*VCC. (Note that the QSPM inputs are CMOS buffers with spec limits of VILmax=0.2*VCC and VIHmin=0.7*VCC - the MC68341 User's Manual electrical specifications incorrectly spec them as TTL level inputs).

10. **JTAG Reset:** When the JTAG RESET instruction is executed, some of the boundary scan control cell are reset to the wrong state. Then, when the part enters JTAG EXTTEST, the address pins and a few other control signals are left in the driving output condition, allowing possible contention with other chips at the board level. Do not rely on the JTAG Reset instruction to set the proper values in the output enable buffers.

11. **SIM:** Autovectored IACK and BR: If BR is asserted during an autovectored IACK cycle, AS will negate 1/2 clock early.

    Workaround: Decode the IACK address range (A19 & FC2 & FC1 & FC0 & !AS) and use the resulting signal to force BR high during IACK cycles.

12. **SIM:** Show Cycles and BR: If show cycles and external arbitration are enabled, and BR is asserted immediately before the clock edge from which DS asserts for a show cycle, the show cycle will be truncated. The data bus drive time for the show cycle will overlap the front end of the alternate master bus tenure by one clock (data will tristate from the clock falling edge one clock after the falling edge BG asserts from).

    Workarounds:

    1) Disable show cycles when alternate master bus activity is possible.

    2) Delay BG assertion to the system by one clock, or delay the alternate master from driving the data bus for one clock after BG asserts.

13. **SIM:** 68K Chip select pairing. The Map Select Register can map byte wide peripherals on the M68000 bus to either the upper or lower half of the data bus. Byte selects only work for word/longword accesses for M68000 bus cycles. For byte accesses, only the even chip select asserts.

14. **SIM 68K Chip Select :** If two chip selects overlap, and the lower priority chip select is configured for M68000 bus cycles, then accesses which match the higher priority chip select will always use M68000 timing.

    Example:

    CS2 programmed for $001000XX, M68300 bus cycles

    CS3 programmed for $00100XXX, M68000 bus cycles

    Accesses to $001000XX will assert CS2 with the correct CS2 port size and termination, but will use M68000 bus cycles.

15. **QSM Interrupt:** The QSM requests an interrupt by asserting an internal IRQ signal. Interrupt arbitration begins and the QSM wins arbitration, but the QSM does not assert an internal DTACK. The IACK code and the interrupt level on the address pins continues to be broadcast. The internal bus monitor does not check for DTACK termination on an IACK cycle, so the part locks up.

    Workaround: Program zeros for the IARB bit in the MCR of the QSM. When the QSM interrupts, no interrupt arbitration will occur during an interrupt acknowledge cycle. The bus error signal is asserted internally, and a Spurious Interrupt vector is supplied. The Spurious Interrupt routine can check for a QSM interrupt and service the QSM if needed.

16. **PIT/RTC/External Interrupt Vector contention.** If two SIM interrupts are pending, the lower priority interrupts will be driven when the higher is serviced.

    Example:

    If the PIT is programmed for a level 4 interrupt and a IRQ5 is assert. If both are pending, the IRQ5 will win. But instead of the External IRQ5 vector being driven on the IMB data bus the PIT vector will be driven.

17. **SIM RTC Alarm:** When in the alarm indicator pulsed mode, the alarm bit in the RTC Control/Status Register (RCR) will not clear when the RCR is read unless RTCOUT has been negated.

    Workarounds:

    1) Wait 30.5us until RTCOUT is negated on it's own before reading the RCR.

    2) Clear the AIE/C bit in the RCR. This will clear the alarm bit and negate RTCOUT.

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0F23F
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1. **SIM External Clock with VCO Mode:**

    a) When the external clock with VCO mode is implemented with an XFC capacitor in the 0.01-0.1uF range, the SIM may not reliably detect VCO lock on powerup. As a result, the part never releases the RESET signal even though the EXTCLK input clock and CLKOUT are in phase.

    Workaround: Use a smaller XFC capacitor. For frequencies > 1MHz start with a capacitance value of 10000pf/F_MHz. Example: for 16.0MHz the recommended XFC capacitance is approximately = 10000pf/16.0 = 625pf. An external POR circuit should be used for all external clock applications to guarantee RESET remains asserted until after VCC stabilizes.

    b) For an external reset after POR, the SLOCK bit may not be set. This is only a problem with the assertion of the SLOCK lock indication. The VCO and CLKOUT remain phase locked to the input clock both during and after the external reset.

2. **SIM EXTCLK to EXTAL coupling:** At higher frequencies (>20MHz) EXTCLK can couple to the XTAL output of the crystal oscillator and dampen out oscillation, causing the crystal oscillator to stop.

    Workaround: Coupling effects can be reduced and/or eliminated by routing the EXTCLK input to avoid the crystal circuitry as much as possible.

3. **SIM 3.3V TDICL Spec:** For 3.3V parts, Spec 27 (Data-In Valid to CLKOUT Low) is 8ns instead of 5ns.

4. **SIM BSW input levels:** The BSW pin requires CMOS drive levels - VILmax=0.2*VCC and VIHmin=0.7*VCC.

5. **RTC Ibat:** During battery backup if VDD rises to above 0.8 volt the current draw (Ibat) will increase. Maximum of 1.5mA.

6. **SIM: Clock Skew in External Clock with VCO Mode:** The skew between the EXTAL input falling edge and CLKOUT output falling edge is specified as +/-5ns. Depending on processing, operating voltage, and input clock frequency the skew may exceed this limit. Current production material is tested at skew limits of +8.5/-5.5ns for 5V product, and +10.5/-7.5 for 3.3V product.

    As noted in the MC68341 UMAD/AD user manual update, the PLL phase locks the falling edges of the EXTAL and CLKOUT clocks, not the rising edge as stated in the manual.

7. **RTC:** The RTC registers cannot be updated because the data becomes invalid before it it is clocked into the part. This renders the RTC to be non-functional. This errata item will be fixed in the next revision of the part. This errata applies only to the 0F23F mask set.

NOTES

1. **PIT, Background Mode:** If Background Debug Mode is entered and exited while the PIT is running and the FRZ1 bit in the SIM40 MCR is set, the PIT value may decrement by an extra count, shortening the timeout period. This will typically only affect emulation.

2. **Serial: RTS operation:** In the hardware flow-control mode of operation, the first assertion of RTSx* after enabling the RxRTS bit (MR1 register bit 7) does not have to be done manually. If a FIFO position is available, RTSx* is enabled immediately when the RxRTS bit is set.

3. **DACKx assertion for M68000 bus cycles:** Normal DACK timing for M68000 bus cycles is the same as AS68K. The user's manual and design spec indicate that DACK should have AS timing. DONEx uses the same timing, but was never documented.