Semiconductor Products Sector
Inter-Office Correspondence

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MC145572 MASKSETS G70B3, F26P3, G32G3 ERRATA
Sept 22, 1997
Rev. 9

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This version of the MC145572 silicon has BR15 mask code = $46.

Note: This series of devices does not have the mask versions silk-screened on the package.

This errata is a list of device problems and key data book clarifications to date for the version of silicon that it covers. In some cases evaluation of later versions of silicon may uncover a problem that could exist in this version but is not documented in the errata for this version.

Revision 9: Sept 22, 1997.
1) Modified item 7 to indicate that theoretically the problem may appear in NT mode.

Problem #1

Device errata:
When data is written to NR0 it is latched but not acted upon until the next assertion of CS (Chip Select) when operating in Parallel Port mode.

Work around: Immediately follow an NR0 write with a NR0 read. The additional read cycle causes the previously written NR0 data to take effect. Also the NR0 read has no effect on any status bits so this code fix can be left in any final production firmware if so desired.

Problem #2.

Databook errata:
Failure to activate in LT mode. This happens when the SFAX pin is not driven as an input or it has not been enabled as an output.

Work around 1: Include a 10K pulldown on the TxSFS/SFAX/S0 pin when SFAX is not enabled as either an input or output.
Work around 2: Set both OR8(b5) and OR8(b1) to a "1" after any reset to enable the SFAX output. This eliminates the need for the 100K ohm resistor.

Note: This is a data book and usage clarification.

Problem #3

Device errata:
The I/O pads have an ESD sensitivity. Measured figures are human body model is 1.5KV and machine model is approximately 100V. The specifications are 2KV and 400V respectively.

Problem #4

Device errata:
When the MC145572 is operated in absolute power down mode the power consumption is 10 mW, not 5 mW as indicated in Section 10.3 of the databooks.

Problem #5

Databook errata:
Failure to go into analog loopback mode when operating as an NT. This problem occurs due to the MC145572 being internally reconfigured for LT mode when an analog loopback bit is set to 1.
Work around:: a) Put the NT configured MC145572 into LT mode by setting BR8(b0) to a 1.
b) Make sure that there is a 10 K ohm pulldown resistor on the SFAX pin.
c) Wait five seconds.
d) Set OR9(b5) = 1 to enable analog loopback.

To take the MC145572 out of loopback:
a) Clear OR9(b5) to "0".
b) Clear BR8(b0) to "0".
c) Clear OR8(b5) and OR8(b1) to "0".

Problem #6

Device errata:
When operating in full GCI mode the MC145572 returns a value of $0000 instead of $8000 in response to the Monitor Channel Device ID command. Section 8.3 of the databook MC145572/D Rev. 2 describes the operation of the Monitor Channel.

Problem #7

Device errata:
In LT mode the 20.48 MHz oscillator may take several seconds to stabilize after deassertion of any hardware or software reset. Wait five seconds after reset before initializing any registers and/or activating the device. The five second delay allows the oscillator to stabilize so internal register clocks operate correctly. It also allows the PLL to acquire lock to the external 8 kHz reference clock. This problem applies to GCI, and IDL modes of operation. It also applies when changing from NT mode to LT mode.

Theoretically this problem may appear in NT mode though it is expected to be rare.

Problem #8

Device errata:
In GCI mode the MC145572 drives the Monitor channel on DOUT with $00 as the default value instead of $FF.

Problem #9

Device errata:

It is not possible to independently enable D channel and B channel TSEN signals. See OR7(b5) and OR8(b3). To enable TSEN during the D channel time both OR7(b5) AND OR8(b3) must both be set to 1.

Problem #10

Databook errata:
For proper operation of the MC145572 in full GCI mode both the MCU/GCI and PAR/SER pins must be tied to Vss. If the MCU/GCI pin is tied to Vss and the PAR/SER pin is tied to Vdd the monitor channel transmits only $FF during its timeslot on the DOUT pin.

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