Chip Errata for the MC145572A

This document details all known silicon errata for the MC145572A. Table 1 provides a revision history for this document.

Table 1. Document Revision History

Revision Number	Date	Substantive Change(s)
0	Aug 2004	Initial release.

This version of the MC145572A silicon has **BR15 mask code = $52.**

This errata is a list of device problems and key data book clarifications to date for the version of silicon that it covers. In some cases evaluation of later versions of silicon may uncover a problem that could exist in this version but is not documented in the errata for this version.

Errata #1

Device errata: When data is written to NR0 it is latched but not acted upon until the next assertion of CS (Chip Select) when operating in Parallel Port mode.

Work around: Immediately follow an NR0 write with a NR0 read. The additional read cycle causes the previously written NR0 data to take effect. Also the NR0 read has no effect on any status bits so this code fix can be left in any final production firmware if so desired.

Errata #2

Device errata: When operating in parallel mode and the MC145572A is programmed in power-enable mode NR1=$4. The MC145572A will not come out of power-down mode.

Work around: Do not program the MC145572A in power-down enable mode.

Errata #3

Device errata: In LT mode only; the 20.48 MHz oscillator may take several seconds to stabilize after de-assertion of any hardware or software reset. Wait five seconds after reset before initializing any registers and/or activating the device. The five second delay allows the oscillator to stabilize so internal register clocks operate correctly. It

also allows the PLL to acquire lock to the external 8 kHz reference clock. This problem applies to GCI, and IDL modes of operation. It also applies when changing from NT mode to LT mode. This problem does not apply to operation in NT mode.

Errata #4

Databook errata: Failure to activate in LT mode. This happens when the SFAX pin is not driven as an input or it has not been enabled as an output.

Work around 1: Include a 10K pulldown on the TxSFS/SFAX/S0 pin when SFAX is not enabled as either an input or output.

Work around 2: Set both OR8(b5) and OR8(b1) to a "1" after any reset to enable the SFAX output. This eliminates the need for the 100K ohm resistor.

Note: This is a data book and usage clarification.

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