LPC553x

Errata sheet LPC553x

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Errata

1   Product identification

The LPC553x HLQFP100 package has the following top-side marking:

- First line: LPC553xJBD100
- Second line: xxxxxxx
- Third line: **zzz**yywwx**R**
  - **–** yyww: Date code with yy = year and ww = week.
  - **–** xR: Device revision 0A, 1B

The LPC553x HTQFP64 package has the following top-side marking:

- First line: LPC553x
- Second line: JBD64
- Third line: xxxx
- Fourth line: xxxx
- Fifth line: **zzz**yywwx**R**
  - **–** yyww: Date code with yy = year and ww = week.
  - **–** xR: Device revision 0A, 1B

The LPC553x HVQFN48 package has the following top-side marking:

- First line: LPC553x
- Second line: JHI48
- Third line: xxxxxxxx
- Fourth line: xxxx
- Fifth line: **zzz**yywwx**R**
  - **–** yyww: Date code with yy = year and ww = week.
  - **–** xR: Device revision 0A, 1B

2   Errata overview

Table 1. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
ADC.1	Missing code in Standard resolution mode.	0A	Section 3.1
I3C.1	Data lost when using the DMA to write transmit data to I3C, and the data size is greater than the I3C FIFO size.	0A, 1B	Section 3.2
CRP.1	Boot ROM does not give correct Code Read Protection (CRP) status when in CRP_LEVEL3.	0A	Section 3.3
I3C.2	IBI Slave Data EXTDATA is not abortable by another master on the bus.	0A, 1B	Section 3.4
PLL.1	PLL LOCK bit is not reliable	0A, 1B	Section 3.5
CDOG.1	Restart command can't let timer count down	0A, 1B	Section 3.6

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Table 2. AC/DC deviations table

AC/DC deviations	Short description	Product version(s)	Detailed description
n/a	n/a	n/a	n/a

Table 3. Errata notes

Errata notes	Short description	Revision identifier	Detailed description
ROM.1	ROM Flash APIs will not function properly unless FFR_Init is called after Flash_Init	1B	Section 5.1

3 Functional problems detail

3.1 ADC.1: Missing code in Standard resolution mode

Introduction

LPC553x device family contains two instances of Analog to Digital Converter (ADC), ADC0 and ADC1 . In single ended operation both ADCs support standard resolution mode (12-bit resolution) and High resolution mode (16-bit resolution).

Problem

In the standard resolution mode of single ended operation, both ADC0 and ADC1 may have approximately 1 missing code out of 20 codes. Both ADCs do not miss consecutive codes and maintain monotonicity in spite of missing codes.

Work-around

There is no work-around.

3.2 I3C.1: Data lost when using the DMA to write transmit data to I3C, and the data size is greater than the I3C FIFO size

Introduction

The LPC553x includes an I3C peripheral with a DMA interface that can be used to transfer data to or from the I3C data FIFO.

Problem

The issue occurs when using I3C to transmit data written by the SDMA to the Slave Write Data Half-word (SWDATAH)/Master Write Data Half-word (MWDATAH) registers or Master Write Message Data (MWMSG_SDR_DATA) register 2 bytes at a time. If the number of bytes to send exceeds the FIFO size of 8, data is overwritten by the SDMA after the FIFO becomes full.

Work-around

Set the DMAWIDTH field to 10 (Half word) in the Slave DMA Control (SDMACTRL)/Master DMA Control (MDMACTRL) registers and use the Slave Write Data Byte (SWDATAB)/Master Write Data Byte (MWDATAB)

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to write the SDMA data. Avoid using the Slave Write Data Half-word (SWDATAH)/Master Write Data Half-word (MWDATAH) registers or Master Write Message Data (MWMSG_SDR_DATA) register.

3.3 CRP.1: Boot ROM does not give correct Code Read Protection (CRP) status when in CRP_LEVEL3

Introduction

Code Read Protection (CRP) is a mechanism that allows the user to enable different levels of protections in the system, so that access to the on-chip flash and use of the ISP can be restricted.

The LPC553x device family contains 5 CRP levels:

- CRP_LEVEL0
- CRP_LEVEL1
- CRP_LEVEL2
- CRP_LEVEL3
- CRP_LEVEL4

Status of a CRP level can be returned by the LPC553x by using the debug mail box command get CRP Level (DM-AP command 2).

Problem

When the LPC553x is programmed with CRP_LEVEL3 (LC_STATE=0xF and ISP is disabled in CMPA), the Boot ROM does not return the correct status of CRP level.

It returns CRP_LEVEL2 instead. The CRP_LEVEL3 restrictions are not impacted by this problem.

Work-around

There is no work-around.

3.4 I3C.2: More than one In Band Interrupt (IBI) extended data bytes (EXTDATA) emitted by I3C slave are not abortable by the I3C bus master.

Introduction

On these devices, I3C peripheral works in master (controller) as well as in slave (target) mode. This I3C peripheral supports IN Band Interrupt (IBI) feature which allows it in target mode to notify the I3C controller of an interrupt . The I3C target on this device supports up to 7 bytes of extended IBI data following mandatory data byte (MDB). Most IBIs would not use EXTDATA and are only a single MDB.

Problem

When I3C peripheral, on these devices is working as a target device and transmits EXTDATA with more than one byte past the MDB, EXTDATA in IBI are not abortable by the controller on I3C bus.

Work-around

None.

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Workaround

Replace RESTART register write Instruction in all locations with a write to stop register immediately followed by a write to the RELOAD and START register. Both the STOP and START registers should be written with the same value in this situation.

4   AC/DC deviations detail

No known errata.

5   Errata notes detail

5.1 ROM.1: ROM Flash APIs will not function properly unless FFR_Init is called after Flash_Init

Introduction

On the LPC553x, ROM supports Flash based APIs to perform internal flash memory operations and FFR based APIs to configure the CFPA and CMPA flash regions. The flash_init API initializes the internal flash memory. The ffr_init API initializes the CFPA / CMPA regions.

Problem

If the FFR_Init API is not called after the Flash_Init API and before invoking any other API that exercises the flash, the APIs will return the kStatus_InvalidArgument error.

Workaround

To ensure proper functionality of the ROM Flash APIs on device revision 1B, the FFR_Init API must be called after Flash_Init ROM API and prior to using any Flash-related ROM APIs. Refer to SDK version 2.14 or later for reference.

6   Revision history

Table 4. Revision history

Document ID	Release date	Description
LPC553x v.1.7	13 October 2025	• Added Section 5.1.
LPC553x v.1.6	18 July 2024	• Added Section 3.6. • Updated the 'First line' under HLQFP100 package marking in Section 1.
LPC553x v.1.5	24 May 2023	• Added Section 3.5.
LPC553x v.1.4	23 Februrary 2023	• Updated revision identifiers in Section 1, and Section 2overview".
LPC553x v.1.3	11 July 2022	• Added I3C.2 Section 3.4bytes (EXTDATA) emitted by I3C slave are not abortable by the I3C bus master.". • I3C is renamed as I3C.1. • Updated revision identfier from A to 0A throughout the document.
LPC553x v.1.2	23 March 2022	• Added CRP.1 Section 3.3Protection (CRP) status when in CRP_LEVEL3"
LPC553x v.1.1	17 January 2022	• Added ADC.1 Section 3.1

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Table 4. Revision history...*continued*

Document ID	Release date	Description
		• Added I3C.1 Section 3.2I3C, and the data size is greater than the I3C FIFO size".
LPC553x v.1.0	16 September 2021	Initial release.

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