

## Mask Set Errata for Mask XN33G

This report applies to mask XN33G for these products:

- MWCT1000, MWCT1011, MWCT1101, MWCT1111 and MWCT1200

**Table 1. Errata and Information Summary**

Errata ID	Errata Title	Mask <sup>1</sup>	
		2N33G	3N33G
e11484	POR: Residual voltage on VDD may cause POR unsuccessful.	X	
e9432	eFlexPWM: Fractional delay block may power up with an output of 1 instead of 0.	X	X

1. 'X' represents the errata present in the mask.

**Table 2. Revision History**

Revision	Changes
Mar 2019	Public release revision.
May 2020	Applicable mask set or device part number update.
Dec 2020	Workaround description updated in the following errata: <ul style="list-style-type: none"> <li>• e11484</li> </ul>

### e9432: eFlexPWM: Fractional delay block may powerup with an output of 1 instead of 0.

**Description:** Any of the eFlexPWM outputs may be set to 1 upon powering up the fractional delay block. Because there is no reset signal to the flops in the fractional delay block to force a specific reset state, the output must be cleared by creating a pulse on the PWM. This issue only occurs when using the fractional delay block and only lasts until the first time that PWM channel transitions.



**Workaround:** After powering up the fractional delay block of the eFlexPWM by setting FRCTRL[FRAC\_PU] and waiting the required power up time, program the VAL2-5 registers in all submodules to create a PWM pulse (>0% duty cycle) and run for at least one PWM period to clear the state of the registers in the analog block. This can be done prior to enabling the PWM outputs so that external circuitry is not affected.

#### **e11484: POR: Residual voltage on VDD may cause POR unsuccessful.**

**Description:** When powered on with residual voltage larger than 0.2 V on VDD, there is a chance that POR signal releases when VDD rises to a value around 2.1 V, and VCAP has not reached 1.2 V yet. It may cause system to work abnormally, such as some internal peripherals cannot be reset successfully, or the core cannot run. The residual voltage may be caused by an external clamping diode to VDD with the anode powered up earlier than VDD, or VDD not fully dropped to below 0.2 V from last time powered off.

**Workaround:** To avoid formalizing a residual voltage, VDD ramp-up shall be monotonic increase, with ramp-up rate during 0 to 0.5 V not slower than the rest of ramp period, and the whole ramp-up time is between 1 ms and 200 ms.

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