ES_TJA1145A

TJA1145A errata sheet

Rev. 1.0 — 26 March 2026 **Errata**

1 Product identification

The TJA1145A is a high-speed controller area network (CAN) transceiver that provides an interface between a CAN protocol controller and the physical 2-wire CAN bus.

This document provides information about known deviations from the TJA1145A data sheet.

2 Errata overview

Table 1. Errata table

Errata	Short description	Severity level[1][2][3][4]	Solution	Detail description
ER1	Additional parameter for system controller activation	Low	—	Section 3.1
ER2	Full register reset only in unpowered state	Low	—	Section 3.2
ER3	Activity on pins INH and RXD at low V_{BAT}	Low	—	Section 3.3
ER4	Startup restrictions with fast V_{BAT} ramp-up	Medium	—	Section 3.4
ER5	VCS bit only relevant while in Normal mode	Low	—	Section 3.5
ER6	Processing of SPI frames with more than 64 bits	Low	—	Section 3.6
ER7	SPI write access to address 0	Low	—	Section 3.7
ER8	Clarifications of the CAN transceiver state diagram	Low	—	Section 3.8
ER9	Clarification of conditions for wake-up by CAN	Low	—	Section 3.9
ER10	Clarification of status bit COSCS	Low	—	Section 3.10
ER11	CANH/CANL input capacitance	Low	—	Section 3.11

[1] High: Failure mode that severely inhibits the use of the device for all or a majority of intended applications
[2] Medium: Failure mode that might restrict or limit the use of the device for all or a majority of intended applications
[3] Low: Unexpected behavior that does not cause significant problems for the intended applications of the device
[4] Enhancement: Improvement made to the device because of previously found issues on the design

3 Functional problem detail

3.1 ER1: Additional parameter for system controller activation

3.1.1 Severity level

Low

3.1.2 Description

The names of parameters $V_{th(det)pon}$ (power-on detection threshold voltage) and $V_{th(det)poff}$ (power-off detection threshold voltage) may be misleading because here, the terms "power-on/off" primarily refer to the logic state of the device's system controller, which assumes its digital logic is physically powered. A new parameter $V_{th(act)sys}$ (system controller activation threshold voltage) needs to be defined, which represents an additional V_{BAT} threshold below $V_{th(det)poff}$, see Table 2 and Figure 1. The device is physically powered while V_{BAT} (that is, the voltage level at the BAT pin) is above $V_{th(act)sys}$.

In the data sheet, Off mode does not distinguish between physically powered or unpowered state, but such differentiation has turned out to be relevant in the cases described in sections Section 3.2 through Section 3.4.

Table 2. New parameter to be added to the Static characteristics table

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin BAT						
$V_{th(act)sys}$	System controller activation threshold voltage		1.2	—	2.5	V

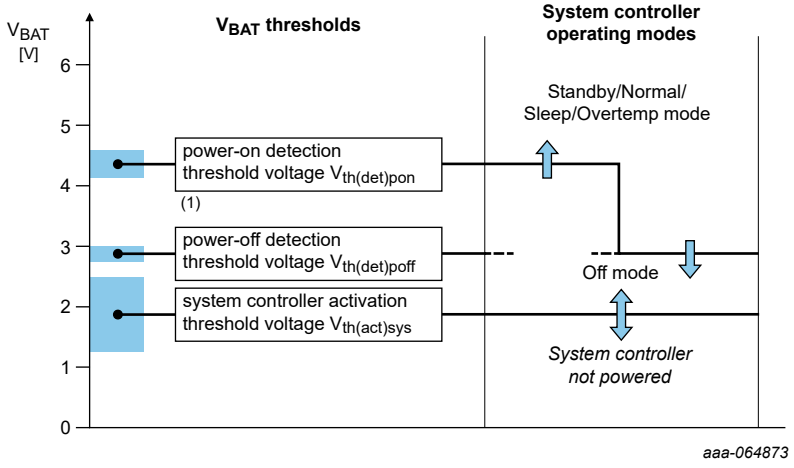

Figure 1. Illustration of V_{BAT} thresholds and related system controller states

(1) For exceptions, see Section 3.3 and Section 3.4

3.2 ER2: Full register reset only in unpowered state

3.2.1 Severity level

Low

3.2.2 Description

The register reset values as listed in Table 31 of data sheet Rev. 2 apply to a device entering Off mode from previous unpowered state,that is, when V_{BAT} rises above $V_{th(act)sys}$, see Section 3.1. When the device enters Off mode because of falling V_{BAT} without becoming unpowered, that is, without V_{BAT} falling further down below $V_{th(act)sys}$, only the following register bits get reset to their default values, automatically:

CDR, CFDC, CMC, COSCS, CPNC, CPNERR, CPNS, CTS, DMn, NMS, PNCOK, PNDM, PO and VCS.

Note: *The MC bits (mode control) are not included in that list. Accordingly, when V_{BAT} has been temporarily below $V_{th(det)poff}$ without going below $V_{th(act)sys}$, the device returns from Off mode to its previous mode before the undervoltage condition (Standby, Normal, or Sleep), as determined by the unchanged MC bits, but the PO bit is set to 1. When returning to Sleep mode this way, the power-on event (PO = 1) does not cause wake-up from Sleep mode, although it lets RXD drive a LOW level.*

3.2.3 Workaround

The application should not assume that with PO = 1 (power-on event) all registers have been reset to their default values. All registers should be initialized by software.

3.3 ER3: Activity on pins INH and RXD at low V_{BAT}

3.3.1 Severity level

Low

3.3.2 Description

While V_{BAT} is kept within a narrow voltage window around the system controller activation threshold $V_{th(act)sys}$ (see Section 3.1), the device may behave as if V_{BAT} was already above the power-on detection threshold $V_{th(det)pon}$. If this situation persists for longer than the startup time $t_{startup}$, the device may even transition to Standby mode. This is noticeable primarily as activity on pins INH and RXD, which may be unexpected at such low supply voltage. When the supply voltage exits this window, the device resumes regular operation as described in the data sheet.

This effect can be observed for both rising and falling V_{BAT}.

3.3.3 Workaround

Applications should be designed in a way that they tolerate any signals on pins INH and RXD while V_{BAT} is within the range of $V_{th(act)sys}$ Min and Max values (see Table 2).

3.4 ER4: Startup restrictions with fast V_{BAT} ramp-up

3.4.1 Severity level

Medium

3.4.2 Description

For a "slow" V_{BAT} ramp-up time from 2.8 V to 4.55 V of more than 175 µs, the power-on threshold $V_{th(det)pon}$ dictates the startup behavior, as described in data sheet (see Figure 2). This also applies to any return (with arbitrary slew rate) from a supply undervoltage condition $V_{th(act)sys} < V_{BAT} < V_{th(det)poff}$.

However, for a "fast" ramp-up time of less than 175 µs, the startup behavior may differ as illustrated in Figure 2:

- Device startup to Standby mode is triggered, at the latest, when the supply voltage exceeds 7.3 V (waveforms 1 and 2 in Figure 2) or has dropped below 4.87 V (waveform 4).
- If, after ramping up, V_{BAT} is kept continuously inside of a small voltage window, specific per sample and within the range 4.87 V to 7.3 V, system controller startup may fail (waveform 3) although V_{BAT} has already risen above $V_{th(det)pon}$. The device will enter Standby mode only after the system controller has recovered, which will happen when V_{BAT} exits this window (waveforms 2 and 4). Once running, the system controller remains active as expected at least until next power cycle with V_{BAT} falling below $V_{th(act)sys}$.

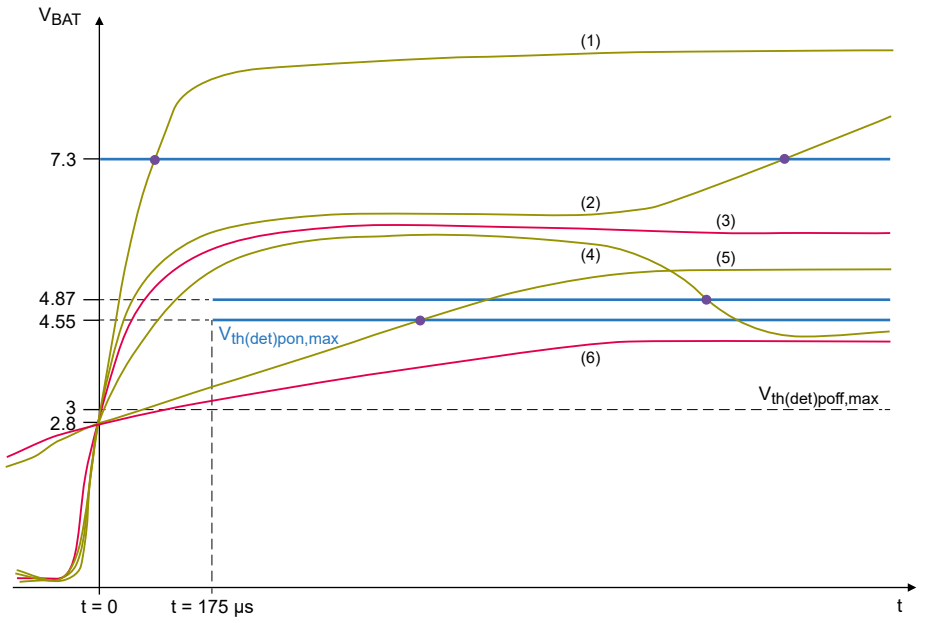

Figure 2. TJA1145A startup behavior with various supply waveform examples for slow or fast ramp-up

Waveforms (1) through (4) in Figure 2 represent examples for fast supply ramp-up, because the rise time from 2.8 V to 4.55 V is less than 175 µs. Waveform (1) can be considered as being typical for connection to a 12 V

car battery by closing a contact. Waveforms (2) through (4) could theoretically occur when closing contact to a discharged, aged and/or overloaded 12 V battery. Waveform (2) assumes battery recovery from initial overload, resulting in delayed but successful startup of the device. Waveform (3) represents a theoretical example without recovery of the battery voltage, which may prevent the device from starting up. Example waveform (4) would initially have the same effect as waveform (3), but it illustrates that device startup will still be triggered when the supply voltage goes down again, latest when it has fallen below 4.87 V.

Waveforms (5) and (6) represent examples for slow supply ramp-up, because the rise time from 2.8 V to 4.55 V is longer than 175 µs. Waveforms like (5) may occur during cranking of the combustion engine with a weak battery. For completeness, waveform (6) illustrates that startup can obviously not be guaranteed when the supply voltage does not exceed the max value of the power-on detection threshold voltage $V_{th(det)pon}$.

3.4.3 Workaround

When the BAT pin shall be supplied from a voltage regulator, its output voltage must be higher than 7.3 V.

3.5 ER5: VCS bit only relevant while in Normal mode

3.5.1 Severity level

Low

3.5.2 Description

The data sheet tells that the VCS bit (V_{CC} supply voltage status) is active only when CMC = 01. However, there is an additional condition: the device must be in Normal mode. While the device is not in Normal mode or CMC is not 01, reading the VCS bit returns a value that may not represent the V_{CC} status.

Note: *The mechanism of automatic transition to Sleep mode because of longtime V_{CC} (or V_{IO}) undervoltage is independent from the values of the bits CMC and VCS.*

3.5.3 Workaround

While the device is not in Normal mode or when CMC is not 01, the value of the VCS bit should not be evaluated by the application.

3.6 ER6: Processing of SPI frames with more than 64 bits

3.6.1 Severity level

Low

3.6.2 Description

Although the device rejects SPI frames with any bit count other than 16, 24, or 32, it accepts frames with multiples of 64 plus 16/24/32 bits.

3.6.3 Workaround

The SCSN signal should be controlled in an appropriate way, avoiding inadvertent SPI accesses because of a bit count exceeding 64 bits.

3.7 ER7: SPI write access to address 0

3.7.1 Severity level

Low

3.7.2 Description

The TJA1145A has no register with address 0. Although in general the device ignores an SPI write access to that address, there is one exception:

When the device is in Sleep mode with PO = 1 (see Section 3.2) or with SPIF = 1 (see next paragraph), a 16-bit SPI write access to address 0 causes a transition to Standby mode.

Note: *During Sleep mode with SPIFE = 1 an SPI failure sets the SPIF bit to 1, but does not cause a LOW level on pin RXD and does not cause a transition to Standby mode.*

3.7.3 Workaround

SPI write accesses to address 0 should be avoided.

3.8 ER8: Clarifications of the CAN transceiver state diagram

3.8.1 Severity level

Low

3.8.2 Description

A few details of the CAN transceiver state machine are not described correctly by the state diagram (Figure 5 in the data sheet) and by its textual explanation. The following corrections apply:

- When the conditions for entering Active mode are available but TXD is held LOW, Listen-only mode is entered instead (ad interim until the next TXD rising edge).
- There is no direct transition from CAN Offline to CAN Active. When the conditions for CAN Active are available, first CAN Offline Bias mode is entered (regardless of the V_{CC} level), then CAN Active (but only if $V_{CC} > V_{uvd(VCC)}$).
- In CAN Active mode, when the bus has been idle for already $t > t_{to(silence)}$ when a V_{CC} undervoltage gets detected and CMC is 01, then the bus silence timeout timer is restarted. Accordingly, the combination of CMC = 01 and $V_{CC} < V_{uvd(VCC)}$ can't cause a direct transition from CAN Active mode to CAN Offline.
- A bus silence timeout event is ignored if it occurs between a V_{CC}/V_{IO} undervoltage detection and entering Sleep mode (independent from the value of the CMC bits). The bus will then need to remain silent for a further $t_{to(silence)}$ to trigger a bus silence timeout event.
- In CAN Off mode, pin RXD behaves like in CAN Offline/Offline Bias. However, when V_{BAT} = 0 V, RXD is not able to pull its output HIGH.
- In Standby or Sleep mode, the transceiver is in CAN Offline/CAN Offline Bias mode, independent from the value of the CMC bits. Bias no/yes is determined by detection of bus silence/bus activity and is independent from the CWE bit. Wake-up by bus (if enabled) is possible in both CAN modes, see also Table 3.
- In Normal mode (MC = 111), the combination of selective wake-up (CPNC = PNCOK = 1) with CMC = 00 blocks the automatic transition between Offline and Offline Bias mode.

3.9 ER9: Clarification of conditions for wake-up by CAN

3.9.1 Severity level

Low

3.9.2 Description

The device supports two alternative CAN wake-up methods as defined by ISO11898-2:2016/2024:

- Basic wake-up by WUP (wake-up pattern),
- Selective wake-up by WUF (wake-up frame)

Some of the related device details are not described correctly in the data sheet. Table 3 represents the corrected description, in a concise format.

Table 3. Overview of CAN wake-up methods

	Desired CAN wake-up method	
	Standard/basic wake-up	Selective wake-up (partial networking = PN)
CAN bus activity causing wake-up	WUP, as usually included in every CAN frame	Matching WUF(s), as defined with the PN configuration registers, or any bus signal that causes error counter overflow
Method selection	CPNC = 0 and/or PNCOK[1] = 0	CPNC = 1 and PNCOK[1] = 1
Common CAN wake-up prerequisites	CWE = 1	
Applicable CAN transceiver modes	CAN Offline, CAN offline bias	CAN offline[2], CAN Offline Bias, CAN Active, CAN Listen-only
Wake-up event flag(s)	CW	CW and/or[3] PNFDE

[1] PNCOK gets automatically cleared by an SPI write access to any of the partial neworking configuration registers. It should be set to 1 by the application only after complete initialization of these registers.

[2] From Offline mode, two wake-up frames may be needed for selective wake-up: a WUP included in the first CAN frame (no matter if WUF or not) triggers a transition to Offline Bias mode without generating any wake-up event yet. This enables wake-up by WUF with the next CAN frames. Here, it is assumed that meanwhile the device did not return to Offline mode again (because of bus idle time longer than $t_{to(silence)}$), before the WUF started.

[3] When PNFDE is 1 but CW is 0, CW is blocked. It can be released in two ways:
- Either PNFDE gets cleared, then the next matching WUF will set CW,
- Or the wake-up method gets changed to standard/basic (by clearing PNCOK and/or CPNC), then the next WUP will set CW.

Note: *Status bit CPNERR* ***does not*** *tell if wake-up via standard wake-up is ready or not.*

3.10 ER10: Clarification of status bit COSCS

3.10.1 Severity level

Low

3.10.2 Description

A condition for an error counter decrement sets COSCS, even when the counter is already zero. A condition for an increment clears COSCS. COSCS also gets cleared when the PN decoder is not running (for example, while PNFDE = 1, or in Standby/Sleep mode upon entering CAN Offline mode).

3.11 ER11: CANH/CANL input capacitance

3.11.1 Severity level

Low

3.11.2 Description

Name and symbol of the parameter “common-mode input capacitance $C_{i(cm)}$” in the Static characteristics table of the data sheet should read “input capacitance C_i”, and conditions “CANH, CANL to GND” are missing.

4 Revision history

Table 4. Revision history

Document ID	Release date	Description
ES_TJA1145A v.1.0	26 March 2026	Initial version

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