ES_PN7642

Errata information PN7642

Rev. 1.0 — 30 September 2025 **Errata**

Document information

Information	Content
Keywords	PN7642, known limitations, errata sheet
Abstract	This errata sheet is valid for PN7642.

1 About this document

This document details all known silicon errata for the following product types:

Table 1. Product types

Product Type	12NC
PN7642EV/C100K (T&R)	935437887557
PN7642EV/C100Y (Multiple tray)	935437887518
PN7642EV/C101K (T&R)	935456302557
PN7642EV/C101Y (Multiple tray)	935456302518

2 Known Errata

2.1 I2CM data byte corruption in multi interface use case

2.1.1 Observation

- I2CM or Multi interface use cases are failing, which have two threads running with CLIF read/write operation, high priority events from PMU block or application FW interrupts at the same time.
- When an I2CM interface is used concurrently with any other interfaces (for example, SPI, UART), this issue may occur.
- In some cases, one extra byte (random value) is stored at the beginning of a DMA buffer for an I2C read transaction.

2.1.2 Root cause

Using the I2CM instance as the controller, a delay is observed in timely servicing of disabling DMA within the application domain interrupt service routine (I2C DMA ISR). This causes the controller to add one additional byte, with a random value, at the beginning of the subsequent read operation.

For example:

Actual Data: [11][22][33][44][55]

Erroneous read data: [AB][11][22][33][44][55]

- Delay in executing the application domain interrupt service routine (I2CM_DMA ISR) may occur due to the below conditions:
  - Events within secure FW domain (CLIF events, PMU events), customer application has no control over those, handled at highest priority compared to Non-secure FW domain, in which the customer application resides.
  - Application FW interrupts that have a higher priority than the I2CM_DMA interrupt.

2.1.3 Workaround

Due to inconsistent behavior, it is advised that the application shall perform I2C controller transactions exclusively without other activities on CLIF block or PMU block or other interfaces.

If the application can identify the erroneous additional first byte, it can ignore it. All other data stays valid.

2.2 GPADC error (0x001E) occurs after wakeup from ULPCD mode

2.2.1 Observation / impact to application

- Failure occurs after wake-up from ULPCD to normal mode
- Application using ULPCD gets an error during the call phNfcLib_Init() as GPADC_ERROR (0x001E) after the IC woke up due to either ULPCD_CALIBRATION or ULPCD_DETECTION operation.
- The failure occurrence is random

2.2.2 Root cause

The sporadic failure is root-caused by a metastability on PN7642 GPADC clock switch structure within the PCRM module during waking up from ULPCD operation.

The failure is linked to a deadlock of the PCRM GPADC glitch-free clock multiplexer structure during its transition from ULPCD clock domain to active / normal clock domain following ULPCD cycle. Such a clock mux structure needs a minimum of three clock cycles in the source clock domain before switching synchronously to the destination clock domain. In some corner cases, if the criteria of three clock pulses is not satisfied or fulfilled, it will lead to a deadlock situation.

2.2.3 Recovery mechanism

- Recovery from failure shall require a hard reset of the IC. This can be achieved by either calling PN76_Sys_Hal_HardReset() or VEN toggle.
- The minimum RESET pulse-width required to successfully hard reset the IC is 5ms, as defined in the data sheet (refer to the section "Timing characteristics" in ref.[1]).

3 Conclusion

Any issues (known or otherwise) will be rectified and/or handled appropriately during the preparation phase of the regular maintenance releases and documented in the release notes for SW/FW limitations (ref.[2]) and this document for PN7642 HW errata.

4 Abbreviations

Table 2. Abbreviations

Abbreviation	Description
API	Application programming interface
CLIF	Contactless interface
DCDC	Direct current voltage converter
DMA	Direct memory access
DPC	Direct power control
EEPROM	Electrically erasable programmable read-only memory
FW	Firmware
GPADC	General-purpose analog-to-digital converter
HF	High frequency
HW	Hardware
I2C	Inter-integrated circuit is a synchronous, multi-leader, multi-follower, serial communication protocol used for short-distance, intra-board communication, particularly between microcontrollers and peripheral devices
I2CM	I2C leader
IC	Integrated circuit
ISR	Interrupt service register
NFC	Near field communication
PCRM	Power control and reset management
PMU	Power management unit
RF	Radio frequency
SW	Software
ULPCD	Ultra low-power card detection

5 References

[1] Data sheet – PN7642 – Single-chip solution with high-performance NFC reader, customizable MCU, and security toolbox (link)

[2] Release notes – RN00257 – PN7642 firmware release notes (link)

6 Revision history

Table 3. Revision history

Document ID	Release date	Description
ES_PN7642 v.1.0	30 September 2025	Initial version.

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