ES_P89LPC9361

Errata sheet P89LPC9361

Rev. 3 — 28 July 2013 **Errata sheet**

Document information

Info	Content
Keywords	P89LPC9361 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table at the end of the document.

Revision history

Rev	Date	Description
3	20130728	• Added CLK.1.
2	20100308	• The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Removed DIVM.1
1	20090529	Initial version.

Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

1. Product identification

The P89LPC9361 devices typically have the following top-side marking:

P89LPC9361x x

xxxxxxx xx

xxYYWW R

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC9361:

Table 1. Device revision table

Revision identifier (R)	Revision description
'-'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier
ADC.1	Single Step mode multi channel boundary interrupt	'-'
CLK.1	External oscillator in medium frequency mode	'-'
PGA.1	PGA0 enabled by setting PGATRIM0 bit	'-'

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier
-	-	-

Table 4. Errata notes

Note	Short description	Revision identifier
-	-	-

3. Functional problems detail

3.1 ADC.1: Single Step mode multi channel boundary interrupt

Introduction:

The ADC on the P89LPC9361 is an Analog to Digital converter with 8 bits of resolution. The ADC has features such as a Single Step mode where the ADC will step through the selected channels on each ADC start condition.

Problem:

When the ADC is in Single Step mode with more than 1 channel selected, and a boundary interrupt occurs to any of the lower selected channel-bits, a write to the ADMODA register to clear the BNDI bit before all the selected channels are converted will reset the channel selection counter and the ADC will go back and wait at the lowest selected channel for the next conversion. This applies to both ADC0 and ADC1 on the P89LPC9361.

Work-around:

1. Clear the lower channel bits including the boundary interrupted channel in ADCINS registerbefore the next start request.
2. Use the default boundary channel, not clear BNDI bit until all channels are converted.

3.2 CLK.1: External oscillator in medium frequency mode

Introduction:

When using external oscillator, UCFG1 is used to select the range of the oscillator (Low / Medium / High).

Problem:

When using 4 MHz external oscillator in medium range (UCFG1=61), clock may become unstable. This may lead to unpredictable results; also entering ICP mode may be affected.

Work-around:

Make sure to select high frequency mode (UCFG1=60) when using 4 MHz external oscillator.

3.3 PGA.1: PGA0 enabled by setting PGATRIM0 bit

Introduction:

Register PGACON0 and PGACON0B are used for PGA0 configuration. In register PGACON0, ENPGA0 bit is used to enable PGA0. PGATRIM0 bit is used to enable PGA0 trim. If set, PGA0 is grounded for calibration mode.

Problem:

PGA0 is also enabled by setting PGATRIM0 bit. When disabling PGA0 by clearing ENPGA0 bit, PGA0 still functions. When entering power down mode or total power down mode, PGA module does not enter power down mode and will continue to consume power.

Work-around:

Make sure to clear both PGATRIM0 bit and ENPGA0 bit before entering power down mode or total power down mode. To disable PGA0, also make sure to clear both PGATRIM0 bit and ENPGA0 bit.

4. AC/DC deviations detail

No known errata

5. Legal information

5.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

5.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

5.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

6. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 28 July 2013
Document identifier: ES_P89LPC9361