ERRATA SHEET

Date: **2009 Feb 02**
Document Release: **Version 1.2**
Device Affected: **P89LPC936**

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

NXP
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Identification:

The typical P89LPC936 devices have the following top-side marking:

P89LPC936x x
xxxxxxx xx
xxYYWW R

The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC936:

Revision Identifier (R)	Comment
'-'	Initial device revision
'A'	Second device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	occurs in revision	added
ADC.1	Single Step mode multi channel boundary interrupt	-, A	v1.1
ADC.2	Timer/Edge with Scan Mode Counter Reset	-	v1.1
DIVM.1	Using DIVM in power-down mode	-, A	v1.0
I/O.1	Port 3.0 can be an output during a power-up cycle	-	v1.1
UART.1	Breakdetect trips after 10 zero bits	-, A	v1.1

Errata Overview - AC/DC Deviations

AC/DC Deviation	Short Description	occurs in revision	added
-	-	-	-

Errata Notes

Note	Short Description	occurs in revision	added
V_{DD}.1	V_{DD} Power cycling.	-	v1.0
IRC.1	Internal RC oscillator accuracy.	-, A	v1.0

Functional Deviations of P89LPC936

ADC.1: Single Step mode multi channel boundary interrupt

Introduction: The ADC on the LPC936 is an Analog to Digital converter with 8 bits of resolution. The ADC has features such as a Single Step mode where the ADC will step through the selected channels on each ADC start condition.

Problem: When the ADC is in Single Step mode with more than 1 channel selected, and a boundary interrupt occurs to any of the lower selected channel-bits, a write to the ADMODA register to clear the BNDI bit before all the selected channels are converted will reset the channel selection counter and the ADC will go back and wait at the lowest selected channel for the next conversion. This applies to both ADC0 and ADC1 on the LPC936.

Workarounds:
1) Clear the lower channel bits including the boundary interrupted channel in ADCINS register before the next start request.
2) Use the default boundary channel, not clear BNDI bit until all channels are converted.

ADC.2: Timer/Edge trigger with scan mode

Introduction: The ADC on the LPC936 is an Analog to Digital converter with 8 bits of resolution. The ADC has features such as a Timer / Edge trigger mode where the ADC will generate an ADC start condition on the timer or edge on a pin. Scan mode is an ADC feature where the ADC will scan through all selected channels on an ADC start condition.

Problem: When the ADC is in Timer or Edge mode, with scan mode, and more than 1 channel is selected, and the repeat conversion on timer or edge is selected, the channel counter increments to last selected channel on first conversion, but on all subsequent conversion triggers the counter is not reset, so only the last channel is converted over and over again. This applies to both ADC0 and ADC1 on the LPC936.

Workarounds:
1) To reset the counter that sticks on the last channel the ADC can be disabled and enabled again.
2) Switch from ADC mode to DAC mode and back.

DIVM.1: Using DIVM in power-down mode

Introduction: The LPC936 has a DIVM register that can be used to divide the cclk down. Using DIVM can greatly reduce power when in active mode.

Problem: When DIVM is used in active mode and power-down mode is then entered the LPC936 can not be waken up from power down mode.

Workaround: Before entering powerdown mode set DIVM back to 0x00. This way the LPC936 will be operating full speed for one instruction before entering power-down mode. After the LPC936 has been waken up DIVM can be set back to its original value.

I/O.1: Port 3.0 can be an output during a power-up cycle

Introduction: The LPC936 can be selected to be clocked by an internal RC oscillator. When the internal RC oscillator is selected, P3.0 and P3.1 (which would be used for the crystal oscillator circuit) pins can now be used as general purpose IO pins.

Problem: When the LPC936 is powered up the configuration of the UCFG1 is read out and the LPC936 configured accordingly. The UCFG1 gets read out on the low brownout level of the LPC936 (typically around 2.3V). Before the UCFG1 is read out the crystal oscillator circuit might be enabled. When the crystal circuit is enabled P3.0 is driven to the inverse state of P3.1.

Workaround: Please make sure your external circuitry connected to P3.0 is not affected by this behaviour. Otherwise it is recommended to switch to a different port pin.

RESET.1: External reset does not function correctly when using DIVM

Introduction: The LPC936 can be set up to use either an internal reset or an external reset pin on P1.5. The DIVM register can be used to divide down the internal CCLK down.

Problem: When the LPC936 is configured to have an external reset pin on P1.5 and in the program the DIVM register is programmed to a value different from 0x00 to slow down CCLK, then the next reset pulse will not generate a proper reset for the LPC936. A power cycle has to be applied for the LPC936 to start up again properly.

Workaround: Use the internal reset function.

UART.1: Breakdetect trips after 10 zero bits

Introduction: The UART on the LPC936 has the ability to detect a breakdetect signal, a break signal is a 11 bit long low signal on the RxD input of the UART.

Problem: The breakdetect flag will be set after 10 low bits on the RxD input of the UART. When 9 bit mode is used and all 9 data bits are 0 and the start bit is zero this will be detected as a breakdetect.

Workaround: No known workaround.

Electrical and Timing Specification Deviations of P89LPC936

No known errata

Errata Notes

V_{DD}.1: V_{DD} Power cycling

To generate a proper Power-On-Reset (POR), V_{DD} must have dropped below 0.2V before being powered back up. Power-cycling without V_{DD} having dropped below 0.2V may result in incorrect Program Counter values.

Please also see the V_{POR} specification in LPC936 Datasheet, DC electrical characteristics. The Reset section states that during a power cycle, V_{DD} must fall below V_{POR}.

IRC.1: Internal RC oscillator accuracy

To be able to guarantee the Internal RC oscillator accuracy over the full operating range the V_{DD} supply has to be decoupled sufficiently. Sufficient decoupling is dependant on the noise level in the application, typically a 1uF should be sufficient for most applications.

Noise on the V_{DD} supply pins can cause the Internal RC oscillator to go slightly outside of the specified range.