ES_P89LPC935

Errata sheet P89LPC935

Rev. 02 — 10 May 2010 **Errata sheet**

Document information

Info	Content
Keywords	P89LPC935 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table at the end of the document.

Revision history

Rev	Date	Description
02	20100510	• The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.

Contact information

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1. Product identification

The P89LPC935 devices typically have the following top-side marking:

P89LPC935x x

xxxxxxx xx

xxYYWW R

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC935:

Table 1. Device revision table

Revision identifier (R)	Revision description
'A'	Initial device revision
'B'	Updated device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Occurs in revision
ADC.1	Single Step mode multi channel boundary interrupt	'A', 'B'
ADC.2	Timer/Edge with Scan Mode Counter Reset	'A'
CCU.1	CCU in Alternate output mode inverting	'A'
CCU.2	CCU in Alternate output mode halting	'A'
CCU.3	CCU PLL divider	'A'
CCU.4	CCU capture reading ICRxH	'A'
DIVM.1	Using DIVM in power-down mode	'A', 'B'
EEPROM.1	EEPROM lock-up on power up	'B'
I/O.1	Port 3.0 can be an output during a power-up cycle	'A', 'B'
RESET.1	External reset does not function correctly when using DIVM	'A'
UART.1	Breakdetect trips after 10 zero bits	'A', 'B'

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Occurs in revision
-	-	-

Table 4. Errata notes

Note	Short description	Occurs in revision
V_{DD}.1	V_{DD} power cycling	'A', 'B'
IRC.1	Internal RC oscillator accuracy	'A', 'B'

3. Functional problems detail

3.1 ADC.1: Single Step mode multi-channel boundary interrupt

Introduction:

The ADC on the P89LPC935 is an Analog to Digital converter with 8 bits of resolution. The ADC has features such as a Single Step mode where the ADC will step through the selected channels on each ADC start condition.

Problem:

When the ADC is in Single Step mode with more than one channel selected, and a boundary interrupt occurs to any of the lower selected channel-bits, a write to the ADMODA register to clear the BNDI bit before all the selected channels are converted will reset the channel selection counter and the ADC will go back and wait at the lowest selected channel for the next conversion. This applies to both ADC0 and ADC1 on the P89LPC935.

Work-around:

1. Clear the lower channel bits including the boundary interrupted channel in ADCINS register before the next start request.
2. Use the default boundary channel, not clear BNDI bit until all channels are converted.

3.2 ADC.2: Timer/Edge trigger with scan mode

Introduction:

The ADC on the P89LPC935 is an Analog to Digital converter with 8 bits of resolution. The ADC has features such as a Timer/Edge trigger mode where the ADC will generate an ADC start condition on the timer or edge on a pin. Scan mode is an ADC feature where the ADC will scan through all selected channels on an ADC start condition.

Problem:

When the ADC is in Timer or Edge mode, with scan mode, and more than 1 channel is selected, and the repeat conversion on timer or edge is selected, the channel counter increments to last selected channel on first conversion, but on all subsequent conversion triggers the counter is not reset, so only the last channel is converted over and over again. This applies to both ADC0 and ADC1 on the P89LPC935.

Work-around:

1. To reset the counter that sticks on the last channel the ADC can be disabled and enabled again.
2. Switch from ADC mode to DAC mode and back.

3.3 CCU.1: CCU in symmetrical mode when used with CCU prescaler

Introduction:

The CCU in the P89LPC935 is the capture compare unit, which has the option to generate alternate output on two PWM signals.

All PWM signals can be inverted.

Problem:

In the inactive state of the alternate output mode the inverted PWM signal is always low.

Work-around:

No known work-around.

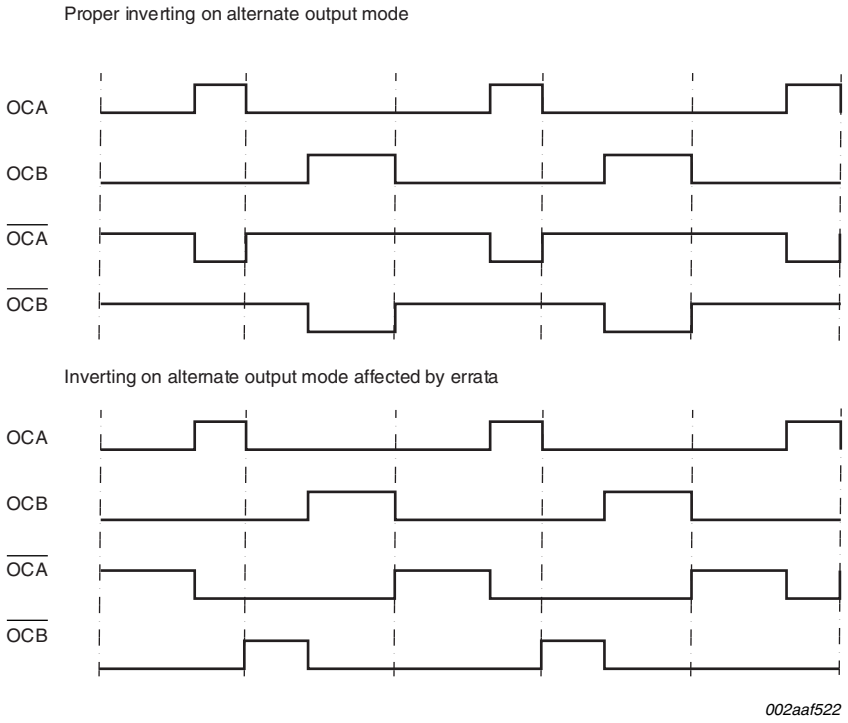

Fig 1. Inverting on alternate output mode

3.4 CCU.2: CCU in Alternate output mode halting

Introduction:

The CCU in the P89LPC935 is the capture compare unit, which has the option to generate alternate output on 2 PWM signals. When a halt condition occurs all the PWM outputs go to the predefined state of FOCx.

All PWM signals can be inverted.

Problem:

In the inactive state of the alternate output mode the inverted PWM signal is always low, even during a halt condition.

Work-around:

No known work-around.

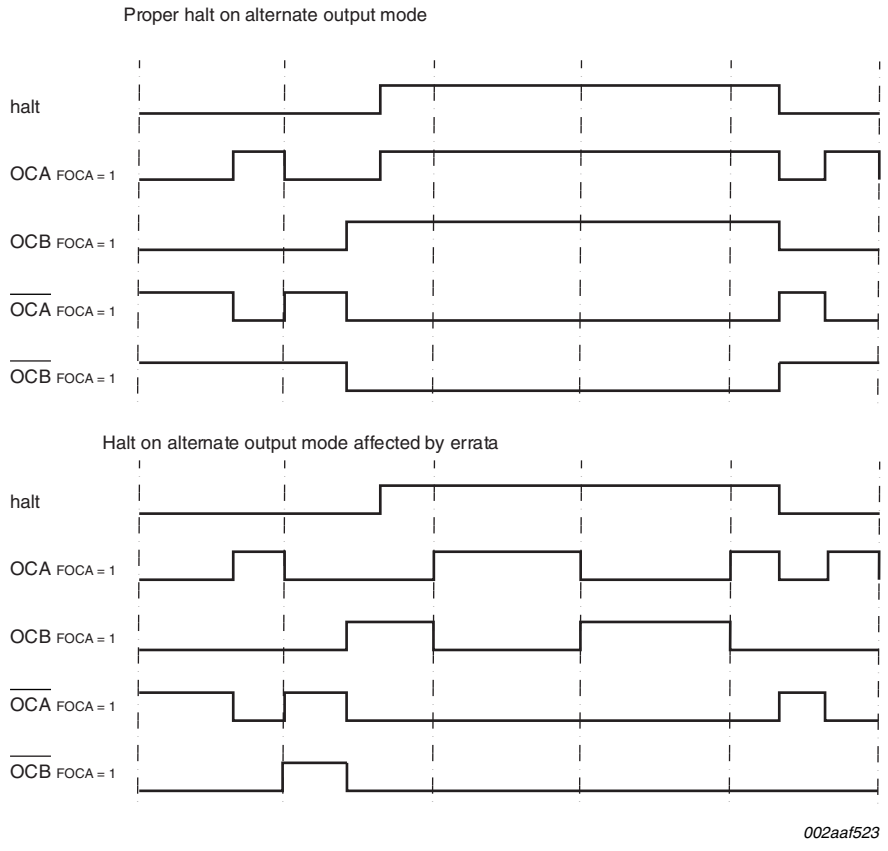

Fig 2. Halt on alternate output mode

3.5 CCU.3: CCU PLL divider

Introduction:

The CCU in the P89LPC935 is the capture compare unit, which has a PLL to boost the frequency of the CCU block. The PLL has an input range between 0.5 MHz and 1 MHz. Different clock dividers such as the DIVM and PLLDIV can be used to get the desired input frequency to the PLL.

Problem:

When the PLLDIV is selected to divide by 0, the PLL circuit does not lock and output the correct frequency.

Work-around:

Use a different combination of DIVM and PLLDIV where PLLDIV is not 0.

3.6 CCU.4: CCU capture reading ICRxH

Introduction:

The CCU in the P89LPC935 is the capture compare unit, which has the option to capture external signals on the ICA and ICB channels.

The capture event is read out in two registers: the capture low register ICRxL and ICRxH.

Problem:

When reading out ICRxH the data will not be correct, the data in ICRxH will be updated after ICRxH is read.

Work-around:

Read ICRxH twice, the second read of the ICRxH will have the correct data.

3.7 DIVM.1: Using DIVM in power-down mode

Introduction:

The P89LPC935 has a DIVM register that can be used to divide the cclk down. Using DIVM can greatly reduce power when in active mode.

Problem:

When DIVM is used in active mode and power-down mode is then entered the P89LPC935 can not be waken up from power-down mode.

Work-around:

Before entering power-down mode set DIVM back to 0x00. This way the P89LPC935 will be operating full speed for one instruction before entering power-down mode. After the P89LPC935 has been waken up DIVM can be set back to its original value.

3.8 EEPROM.1: EEPROM lock-up on power up

Introduction:

The P89LPC935 has onboard data EEPROM, which allows the storing of non-volatile data bytes on the P89LPC935 that will hold their value when the power is not applied to the P89LPC935.

Problem:

With a slow rising V_{DD} (slower than 10 ms) there is a chance that the EEPROM circuitry will lock up, and incorrect data will be read out.

The EEPROM itself still has the correct data.

Work-around:

The data EEPROM can be unlocked by a dummy write cycle. The following function shows a dummy write cycle.

```
void dummywrite(void)
{
  DEECON &= 0x0E;          // EEPROM write mode
  DEEDAT = 0x5A;           // dummy data
  DEEADR = 0x00;           // dummy write address 0x000
  while(!(DEECON&0x80))    // wait till interrupt flag is set
  {
  }
}
```

3.9 I/O.1: Port 3.0 can be an output during a power-up cycle

Introduction:

The P89LPC935 can be selected to be clocked by an internal RC oscillator. When the internal RC oscillator is selected, P3.0 and P3.1 (which would be used for the crystal oscillator circuit) pins can now be used as general purpose IO pins.

Problem:

When the P89LPC935 is powered up the configuration of the UCFG1 is read out and the P89LPC935 configured accordingly. The UCFG1 gets read out on the low brownout level of the P89LPC935 (typically around 2.3 V). Before the UCFG1 is read out the crystal oscillator circuit might be enabled. When the crystal circuit is enabled P3.0 is driven to the inverse state of P3.1.

Work-around:

Please make sure your external circuitry connected to P3.0 is not affected by this behavior. Otherwise it is recommended to switch to a different port pin.

3.10 RESET.1: External reset does not function correctly when using DIVM

Introduction:

The P89LPC935 can be set up to use either an internal reset or an external reset pin on P1.5. The DIVM register can be used to divide down the internal CCLK down.

Problem:

When the P89LPC935 is configured to have an external reset pin on P1.5 and in the program the DIVM register is programmed to a value different from 0x00 to slow down CCLK, then the next reset pulse will not generate a proper reset for the P89LPC935. A power cycle has to be applied for the P89LPC935 to start up again properly.

Work-around:

Use the internal reset function.

3.11 UART.1: Breakdetect trips after 10 zero bits

Introduction:

The UART on the P89LPC935 has the ability to detect a breakdetect signal. A break signal is a 11 bit long low signal on the RxD input of the UART.

Problem:

The breakdetect flag will be set after 10 low bits on the RxD input of the UART. When 9 bit mode is used and all 9 data bits are 0 and the start bit is zero this will be detected as a breakdetect.

Work-around:

No known work-around.

4. AC/DC deviations detail

No known errata

5. Errata notes

5.1 V_{DD}.1: V_{DD} power cycling

To generate a proper Power-On Reset (POR), V_{DD} must have dropped below 0.2 V before being powered back up. Power-cycling without V_{DD} having dropped below 0.2 V may result in incorrect Program Counter values.

Please also see the V_{POR} specification in P89LPC935 data sheet, DC electrical characteristics. The Reset section of the data sheet states that during a power cycle, V_{DD} must fall below V_{POR}.

5.2 IRC.1: Internal RC oscillator accuracy

To be able to guarantee the Internal RC oscillator accuracy over the full operating range the V_{DD} supply has to be decoupled sufficiently. Sufficient decoupling is dependent on the noise level in the application, typically a 0.1 uF capacitor should be sufficient for most applications.

Noise on the V_{DD} supply pins can cause the Internal RC oscillator to go slightly outside of the specified range.

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