ES_P89LPC912

Errata sheet P89LPC912

Rev. 03 — 12 March 2010 **Errata sheet**

Document information

Info	Content
Keywords	P89LPC912 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table at the end of the document.

Revision history

Rev	Date	Description
03	20100312	• The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Added Revision D.
02	20091116	• Added Revision A and C.
01	20080310	Initial version.

Contact information

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1. Product identification

The P89LPC912 devices typically have the following top-side marking:

P89LPC912x x

xxxxxxx xx

xxYYWW R

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC912:

Table 1. Device revision table

Revision identifier (R)	Revision description
'-'	Initial device revision
'A'	Second device revision
'C'	Third device revision
'D'	Fourth device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Fixed in revision
I/O.1	Port Configuration	'A'
I/O.2	Port 2.4 can draw additional power	'A'
ICP.1	ICP Global Erase	'A'
RESET.1	External reset does not function correctly when using DIVM	'A'
DIVM.1	Using DIVM in power-down mode	none
I/O.3	Port 3.0 can be an output during a power-up cycle	'D'
RESET.2	External Pin Reset/Watchdog timer reset may not function correctly	'D'

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Fixed in revision
-	-	-

Table 4. Errata notes

Note	Short description	Fixed in revision
V_{DD}.1	V_{DD} Power cycling.	'C'
IRC.1	Internal RC oscillator accuracy	none

3. Functional problems detail

3.1 I/O.1: Port configuration

Introduction:

The I/O ports of the P89LPC912 can be configured to four different modes by writing to the PxM1 and PxM2 registers. The default mode after Reset is ‘Input Only’.

Problem:

Coming out of Reset, the P89LPC912 port registers should be initialized as follows. Without executing this sequence, the P89LPC912 could consume additional power.

Work-around:

Initialize the P89LPC912 ports in two steps:

Step 1: Configure all port registers with this initialization.

```
P0M1 = 0x00;          // set P0 to quasi-bidirectional

P1M1 = 0x00;          // set P1 to quasi-bidirectional

P2M1 = 0x00;          // set P2 to quasi-bidirectional

P3M1 = 0x00;          // set P3 to quasi-bidirectional
```

Step 2: Configure the port pins on the P89LPC912 to their required mode **using only AND and OR** operations. Make sure to modify only the port pins available on the P89LPC912.

3.2 I/O.2: Port 2.4 can draw additional power

Introduction:

Port 2.4 is a general purpose I/O pin.

Problem:

P2.4 always has an active internal pull-up, which will draw additional power when the port is written low.

Work-around:

No known workaround.

3.3 ICP.1: ICP Global Erase

Introduction:

The P89LPC912 can be programmed using ICP (In Circuit Programming). One of the ICP functions is the Erase Global command, which will erase the entire chip including the security bytes and configuration information.

Problem:

When giving the Erase Global command through the ICP interface the P89LPC912 will not clear the busy flag and stay busy forever.

Work-around:

The workaround can be done in 4 steps:

Step 1: Shift out the WR_FMCON command followed by the Erase Global opcode.

Step 2: Wait 5ms.

Step 3: Do 8 dummy reads with the RD_FMDATA_I command.

Step 4: Read FMCON until the busy flag gets cleared.

Please also see Figure 1.

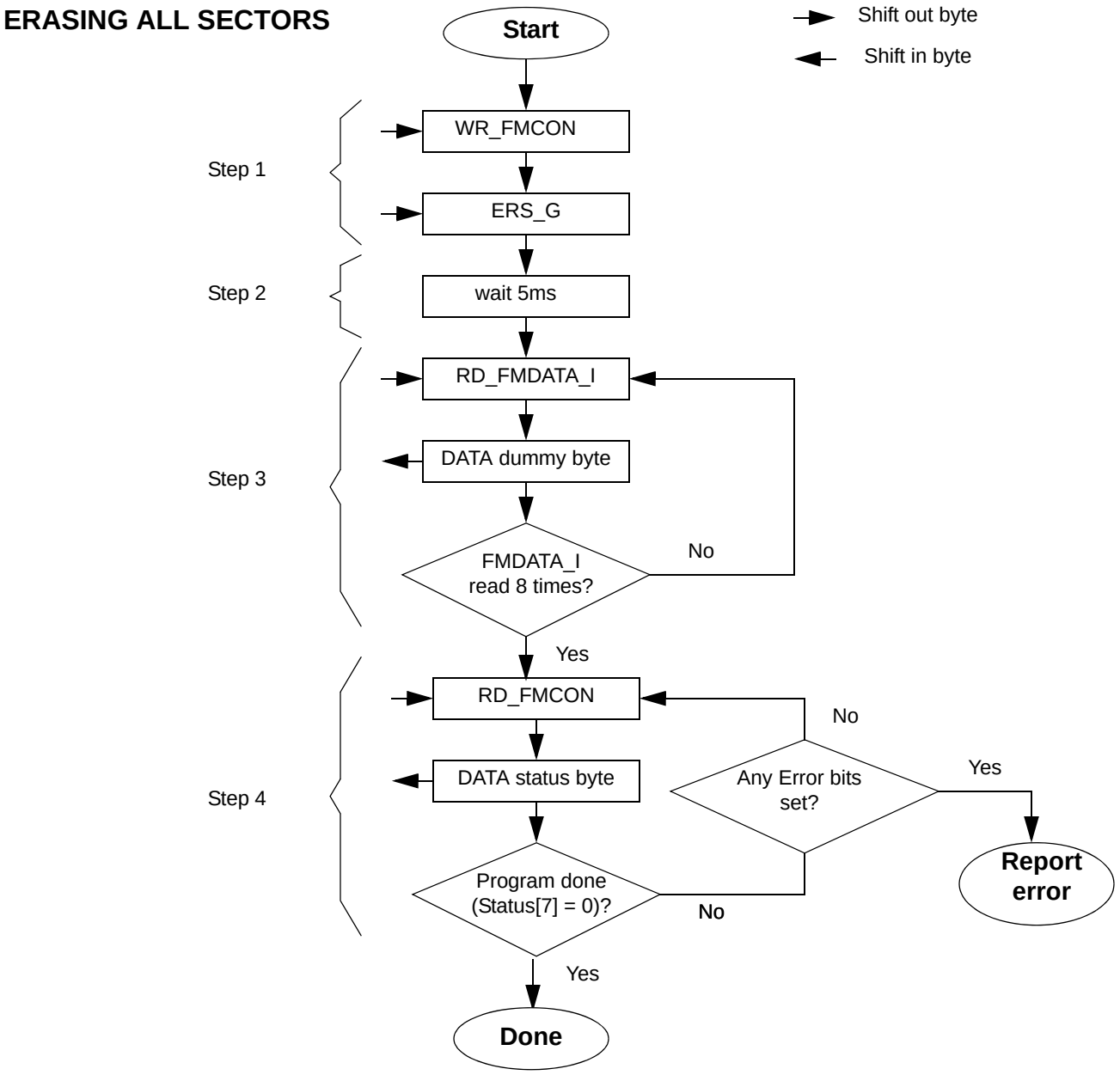

Fig 1. Flowchart ICP global erase

3.4 RESET.1: External reset does not function correctly when using DIVM

Introduction:

The P89LPC912 can be set up to use either an internal reset or an external reset pin on P1.5. The DIVM register can be used to divide down the internal CCLK down.

Problem:

When the P89LPC912 is configured to have an external reset pin on P1.5 and in the program the DIVM register is programmed to a value different from 0x00 to slow down CCLK, then the next reset pulse will not generate a proper reset for the P89LPC912. A power cycle has to be applied for the P89LPC912 to start up again properly.

Work-around:

Use the internal reset function.

3.5 DIVM.1: Using DIVM in power-down mode

Introduction:

The P89LPC912 has a DIVM register that can be used to divide the cclk down. Using DIVM can greatly reduce power when in active mode.

Problem:

When DIVM is used in active mode and power-down mode is then entered the P89LPC912 can not be waken up from power down mode.

Work-around:

Before entering powerdown mode set DIVM back to 0x00. This way the P89LPC912 will be operating full speed for one instruction before entering power-down mode. After the P89LPC912 has been waken up DIVM can be set back to its original value.

3.6 I/O.3: Port 3.0 can be an output during a power-up cycle

Introduction:

The P89LPC912 can be selected to be clocked by an internal RC oscillator. When the internal RC oscillator is selected, P3.0 and P3.1 (which would be used for the crystal oscillator circuit) pins can now be used as general purpose IO pins.

Problem:

When the P89LPC912 is powered up the configuration of the UCFG1 is read out and the P89LPC912 configured accordingly. The UCFG1 gets read out on the low brownout level of the P89LPC912 (typically around 2.3V). Before the UCFG1 is read out the crystal oscillator circuit might be enabled. When the crystal circuit is enabled P3.0 is driven to the inverse state of P3.1.

Work-around:

Please make sure your external circuitry connected to P3.0 is not affected by this behavior. Otherwise it is recommended to switch to a different port pin.

3.7 RESET.2: External Pin Reset/Watchdog timer reset may not function correctly

Introduction:

P89LPC912 can be set up to use P1.5 as an external reset pin or to use the watchdog timer as a reset source.

Problem:

When the P89LPC912 is either configured to apply the external pin reset (P1.5) or watchdog timer reset,this reset signal may not generate a proper reset for the P89LPC912 when watchdog oscillator is running.A power cycle has to be applied for the P89LPC912 to start up again properly.

Work-around:

1. For watch timer reset:use PCLK as clock source for watchdog timer,or use software reset function (watchdog timer reset generates interrupt,in interrupt routine watchdog oscillator is stopped and reset is started).
2. For external reset:do not use watchdog oscillator when reset may happen on P1.5.When watchdog functionality is needed,do not use watchdog oscillator as clock source,but select another one.

4. AC/DC deviations detail

No known errata

5. Errata notes

5.1 V_{DD}.1: V_{DD} power cycling

To generate a proper Power-On-Reset (POR), V_{DD} must have dropped below 0.2V before being powered back up. Power-cycling without V_{DD} having dropped below 0.2V may result in incorrect Program Counter values.

Please also see the VPOR specification in P89LPC912 Datasheet, DC electrical characteristics. Section 8.15 (Reset) states that during a power cycle, V_{DD} must fall below VPOR.

5.2 IRC.1: Internal RC oscillator accuracy

To be able to guarantee the Internal RC oscillator accuracy over the full operating range the V_{DD} supply has to be decoupled sufficiently. Sufficient decoupling is dependant on the noise level in the application, typically a 0.1uF should be sufficient for most applications.

Noise on the V_{DD} supply pins can cause the Internal RC oscillator to go slightly outside of the specified range.

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