# ERRATA SHEET

**Date:** **June 24, 2002**
**Document Release:** **Version 1.0**
**Devices Affected:** **P89C660, P89C662, P89C664, P89C668 (referenced to as P89C66x in this document)**

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

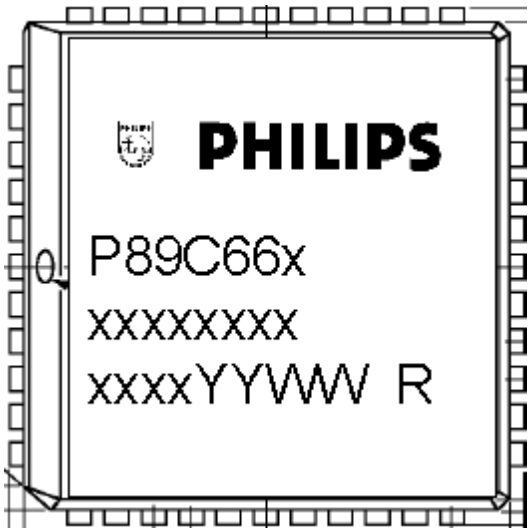
2002 Jun 24

**Philips Semiconductors**

PHILIPS

## IDENTIFICATION:

The P89C66x devices have the following top-side marking (PLCC44 package shown):




The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89C66x:

| Revision Identifier (R) | Comment |
|---|---|
| 'G' | |

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that same year.

## FUNCTIONAL DEVIATIONS OF P89C66X

**ISP/IAP.1:** **Erase / Erase Verify problem regarding Boot Vector and Status Byte**

Introduction: The P89C66x contains two special Flash registers: the BOOT VECTOR and the STATUS BYTE. At the falling edge of reset, the P89C66x examines the contents of the Status Byte. If the Status Byte is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Status Byte is set to a value other than zero, the contents of the Boot Vector is used as the high byte of the execution address and the low byte is set to 00H. The factory default setting is 0FCH, corresponding to the address 0FC00H for the factory masked-ROM ISP boot loader. A custom boot loader can be written with the Boot Vector set to the custom boot loader. When erasing the Status Byte or Boot Vector, both bytes are erased at the same time. It is necessary to reprogram the Boot Vector after erasing and updating the Status Byte.

Problem: During the Erase operation, the Status Byte and the Boot Vector might not be erased thoroughly enough. Therefore, after the Status Byte and Boot Vector have been programmed, a read operation may deliver the wrong contents of these registers.

Workaround: Depending on the type of Flash programming, the following can be used:

**Flash programming using an external Programmer:**
Philips has notified the supported parallel programmer vendors.
Check with your programmer vendor to verify that their latest algorithm includes the extra erase cycles for the Boot Vector and Status Byte.

**Flash programming using ISP (In-System Programming):**
The following ISP Flash programming tools are available with additional erase cycles for the Boot Vector and the Status Byte:
**1) WinISP Version 2.28** (or higher, from Philips):
**2) FlashMagic Version 1.25** (or higher, from Embedded Systems Academy)
(See next page how to download these tools.)

**Flash programming using IAP (In-Application Programming):**
Use only the latest version of the ISP/IAP Flash Programming Application Note AN461 from October 2001 to do In-Application Programming. It describes how to add additional erase cycles to the Status Byte / Boot Vector Erase operation.
(See page 5 for instructions on how to download this Application Note.)

**$I^2C$.1:** **Using timer1 as the $I^2C$ clock source:**

Introduction: The P89C668 $I^2C$ peripheral may be clocked from the system clock ($f_{OSC}/n$) or from timer1. The clock source for $I^2C$ is selected via the S1CON SFR, specifically the CR0, CR1, and CR2 bits. Setting these bits selects timer1 as the clock source for $I^2C$.

Problem: When timer1 is selected as the source for the $I^2C$ clock (CR0=CR1=CR2=1) the clock rate deviates from the formula specified in the datasheet.

Workaround: Use only the system clock (fixed prescaler) as the $I^2C$ clock source, do not use timer1 as the $I^2C$ clock source.

**NOTE: PORTS.1:**

It has been observed that ports are sensitive to negative going signals, in particular port zero. It is important that signals applied to port pins are within specification. The minimum input low voltage ($V_{IL}$) specification for this device is -0.5V. Excessive negative-voltage signals can cause erratic program operation.

## ELECTRICAL AND TIMING SPECIFICATION DEVIATIONS OF P89C66X

No known deviations at the release of this document.

## HOW TO DOWNLOAD THE LATEST ISP SOFTWARE:

Free ISP software is available on the Philips web site: “WinISP”, Version 2.29 or later

- Direct your browser to the following page:

  **http://www.semiconductors.com/mcu/download/80c51/flash/**

- Download “WinISP.exe”
- Execute WinISP.exe to install the software

Free ISP software is also available from the Embedded Systems Academy: “FlashMagic”, Version 1.53 or later

- Direct your browser to the following page:

  **http://www.esacademy.com/software/flashmagic/**

- Download FlashMagic
- Execute “flashmagic.exe” to install the software

## HOW TO DOWNLOAD THE ISP/IAP APPLICATION NOTE (AN461):

There is an application note available that deals with In-System and In-Application Programming (AN461).

At http://www.philipsmcu.com, search for “IAP”, then select AN461 from the search results.

## ERRATA HISTORY - FUNCTIONAL PROBLEMS

| Functional Problem | Short Description | problem occurs in device revision |
|---|---|---|
| ISP/IAP.1 | Erase / Erase Verify problem regarding Boot Vector and Status Byte | 'G' |
| $I^2C$.1 | Unable to clock $I^2C$ using Timer1 | 'G' |

## ERRATA HISTORY - AC/DC DEVIATIONS

| AC/DC Deviation | Short Description | problem occurs in device revision |
|---|---|---|
| - | - | |