ERRATA SHEET

Date: **April 17, 2002**
Document Release: **Version 1.0**
Devices Affected: **P87LPC764**

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

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Philips Semiconductors

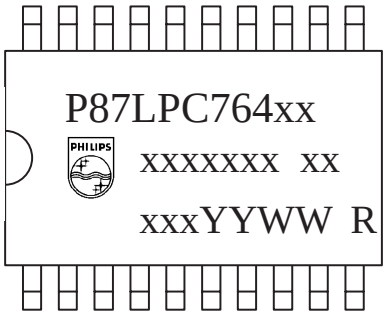
PHILIPS

Low pincount 8-bit microcontroller Errata Sheet

P87LPC764

IDENTIFICATION:

The typical P87LPC764 devices have the following top-side marking (SO 20 package shown):



The last letter in the third line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the P87LPC764:

Revision Identifier (R)	Comment
A, B, E, F	

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

FUNCTIONAL DEVIATIONS OF P87LPC764

RESET.1: **Duration of External Reset at Power-Up**

Clarification: If you are using the internal reset function on the 87LPC764 (highly recommended), the following problem description does NOT apply.

Problem: If P1.5 of the 87LPC764 is used as external reset input and a power-up reset is performed, then the rising edge of the external reset signal MUST occur within 120µs after the rising edge of V_{DD}, otherwise the device is not guaranteed to reset correctly.

Figure 20 in the current 87LPC764 Data Sheet from January 8, 2001 shows external components connected to the reset pin. These components are not necessary and should be removed from the circuit design. Please refer to the newest revision of the Data Sheet which can be found here:

http://www.semiconductors.com/pip/P87LPC764BD

Workaround: 1) Use the internal power-on reset (enabled by default) by leaving the RPD bit in the UCFG1 Register set to 1. No external components are necessary.

2) If P1.5 is used as the external reset input (bit UCFG1.RPD = 0), make sure that during power-up the rising edge of the external reset signal occurs within 120µs after the rising edge of V_{DD}. Please note that this restriction is only necessary during power-up. If V_{DD} stays constant (warm reset), there is no restriction on the length of the external reset signal.

ELECTRICAL AND TIMING SPECIFICATION DEVIATIONS OF P87LPC764

DC.VIL.1: **V_{IL} (input low voltage) of External Reset Pin $\overline{RST}$ (P1.5)**

Deviation: A logic low level at pin P1.5 can only be guaranteed up to 0.2 V_{DD} instead of 0.3 V_{DD}.

ERRATA HISTORY - FUNCTIONAL PROBLEMS

Functional Problem	Short Description	problem occurs in device revision	problem does not occur in device revision
RESET.1	Duration of External Reset at Power-Up	B, E	A, F

ERRATA HISTORY - AC/DC DEVIATIONS

AC/DC Deviation	Short Description	problem occurs in device revision	problem does not occur in device revision
DC.VIL.1	V_{IL} (input low voltage) of External Reset Pin $\overline{RST}$ (P1.5)	B, E	A, F