MOTOROLA

Chip Errata
DSP96002 Digital Signal Processor
Mask: D42G

ERRATA

Errata Description	Applies to Mask
1. Sign extension instruction, EXTB, does not work correctly when bit 7 in the register is one.	D42G

The workaround is to execute the following instruction sequence:

```
MOVE    #$FF,d0.l
AND     d0,d1 d1.l,d2.l
ORC     d0,d2 d1.l,d0.l
LSL     #$19,d0.l
JCC <   ENDEXT
MOVE    d2.l,d1.l

ENDEXT
```

Assume d1.l contains input and output values whereas d0.l and d2.l contain temporary data.

	Applies to Mask
2. I-Cache Problem:	D42G

When the DSP96002 is in the Cache Enable Mode (CE = 1), the bus arbitration protocol does not function correctly on the port where the missed fetches are performed. The arbitration protocol does function correctly on the other port.

NOTES

1. An over-bar (i.e. $\overline{\text{xxxx}}$) indicates an active-low signal.
2. The letters seen to the right of the errata tell which DSP96002 mask numbers apply.

-end-