MOTOROLA

Chip Errata
DSP56303 Digital Signal Processor
Mask: 1F94R

General remark: In order to prevent the usage of instructions or sequences of instructions that do not operate correctly, the user is encouraged to use the “lint563” program to identify such cases and use alternative sequences of instructions. This program is available as part of the Motorola DSP Tools CLAS package.

Silicon Errata

Errata Number	Errata Description	Applies to Mask
ES2	Description (added 2/18/1996): The DSP56303 cannot work with a low frequency crystal (less than 500 KHz) connected as its clock source between EXTAL and XTAL pins. Workaround: Not available	1F94R
ES3	Description (added 2/18/1996): If any DMA channel is active and a second DMA channel is enabled by writing DE = 1 and TM = 011 to its control register, and the next instructions cause “transfer stall” (see Appendix B-3.4.2 in the DSP56300 core specification) or “conditional transfer interlock” (see paragraph B-3.5.1 in the DSP56300 core specification), then the second DMA channel does not start data transfer. Workaround: Insert one NOP instruction between the DMA control register write and the sequence causing the “transfer stall” or “conditional transfer interlock”. Do not place a write instruction to the DMA control register with DE = 1 and TM = 011 as a second word of a fast interrupt routine.	1F94R

Errata Number	Errata Description	Applies to Mask
ES4	Description (added 2/18/1996): Two sequential 1-cycle writes to the same peripheral do not work properly. Workaround: Not available	1F94R
ES5	Description (added 2/18/1996): When external bus activity is disabled (OMR[4] is set) and there is a contention between the DMA and core access to internal memory (access to the same 256-word bank), the DMA does not function properly. Workaround: Do not disable external bus activity (do not set OMR[4]) if the DMA will be used.	1F94R
ES6	Description (added 2/18/1996): When the stack extension is enabled and a nested DO loop with consecutive LAs ends causing SP to return to 0, a stack extension operation which fills the HW stack is wrongly executed (but no stack error occurs), causing EP to be decremented under its lowest permitted value. If this section of the memory belongs to another program task, damage will be caused because of stack extension operation that will overwrite these two memory locations (EP-1 and EP-2). Workaround: Any of the following alternatives can be used: a. Guarantee that EP-1 and EP-2 memory locations are not used by any task. b. Separate the two consecutive LAs by one instruction. c. Push a dummy value onto the stack before the nested DO loop.	1F94R

Errata Number	Errata Description	Applies to Mask
ES7	Description (added 2/18/1996): The STOP instruction does not work properly. Workaround: Not available	1F94R
ES8	Description (added 2/18/1996): The $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, PINIT/$\overline{\text{NMI}}$, HCLK, and $\overline{\text{RESET}}$ pins do not have the proper 5 volt protection. Workaround: Not required. The pins function correctly as specified. There is no significant reliability degradation expected. It is recommended that the system apply only 3.3 volt levels to these pins if possible.	1F94R
ES10	Description (added 2/18/1996): Stack extension mechanism does not work properly if a conditional jump or branch to subroutine is used. Workaround: For the proper operation, the following instructions should not appear immediately after conditional jump or branch to subroutine: XY Memory Data Move (A-6.76) X Memory Move (A-6.71) Y Memory Move (A-6.73) Long Memory Data Move (A-6.75) Immediate Short Data Move (A-6.68) Register to Register Data Move (A-6.69) Address Register Update (A-6.70) X Memory and Register Data Move (A-6.72) Y Memory and Register Data Move (A-6.74) Arithmetic Instructions that allow Parallel Moves listed above IFcc and IFcc.U (A-6.41) Note: For this workaround, any of the listed above instructions should not be the first instruction of interrupt service routine.	1F94R

Errata Number	Errata Description	Applies to Mask
ES11	Description (added 2/18/1996): When the DMA channel is enabled in triggered by request mode and the core is in the WAIT state, a false DMA data transfer might occur (e.g., one DMA request might cause two data transfers instead of one). Workaround: Not available	1F94R
ES14	Description (added 2/18/1996): When the DMA performs external memory accesses with priority higher than the core and both continuous mode and interrupt enable bits are set in the channel's control register, then the DMA interrupt might not occur if the core performs external memory access immediately after the enabling (DE = 1) of the DMA channel. Workaround: In this scenario any of the following alternatives can be used: a. Do not set continuous mode. b. Use dynamic DMA-core priority. c. Guarantee that the core will perform at least two instructions fetched from internal memory immediately after setting of the DE.	1F94R

ES15	Description(added 2/18/1996):
	
	While stack extension is enabled and MOVE to/from SSH is followed by Address Generation Interlock of Type0, then improper operation may occur. For example, the following sequence may generate incorrect results:
	
	`MOVE SSH,A`
	`MOVE #0,R7`
	`MOVE A,X:(R7)`
	
	Workaround:
	
	After MOVE to/from SSH use any instruction sequence that does not cause Address Generation Interlock of Type0.
	
	Note: No interrupt service routine should start with Address Generation Interlock of Type0).
		1F94R

Errata Number	Errata Description	Applies to Mask
ES16	Description (added 2/18/1996): When the chip is powered up with PLL enabled (PINIT = 1), the skew between EXTAL and CLKOUT after the PLL locks cannot be guaranteed at high frequency (over 50 MHz, not 100% tested). Workaround: If skew between EXTAL and CLKOUT is needed, power up with PINIT = 0, and then enable the PLL by software.	1F94R

Errata Number	Errata Description	Applies to Mask

ES17	Description (added 2/18/1996):
	
	A change-of-flow instruction that appears at LA-1 or LA-2 (or two-words change of flow instruction at LA-3) while stack extension is enabled may cause improper operation if the preceding instruction activates the stack. For example, the following sequences may generate incorrect results:
	
	a. Example 1
	
	`DO #N,LABLE`
	`...`
	`MOVE SSH,N3 ; stack activating instruction`
	`JSR R1 ; LA-1`
	`NOP ; LA`
	
	`LABLE`
	
	b. Example 2
	
	`DO #M,LABLE1`
	`DO #N,LABLE2`
	`...`
	`NOP ; stack activating instruction`
	
	`LABLE2`
	`JSR R1 ; LA-1`
	`NOP ; LA`
	
	`LABLE1`
	
	Workaround:
	
	For proper operation the following should be guaranteed:
	
	a. Stack activating instruction does not appear immediately before the restricted above change of flow instruction.
	
	None: Any instruction at LA is a stack activating instruction, for example, in the case of nested DO-loops.
	
	b. Interrupt service routine should not include more than fifteen stack pushes and pops.
		1F94R

Errata Number	Errata Description	Applies to Mask

ES21	Description (added 4/16/1996):
	
	If the DMA channel performs non-zero wait state data accesses to/from external memory and the DMA interrupt is enabled, a false interrupt may occur in addition to the correct one.
	
	Workaround:
	
	Ensure that the channel's DTD status bit in the DSTR register is set before jumping to the interrupt service routine (i.e., the interrupt is correct only when DTD is set).
	
	Example:
	
	`ORG P:I_DMA2`
	
	`JSSET #M_DTD2,X:M_DSTR,ISR_ ; ISR_ is interrupt`
	`; service routine label`
	
	`; for DMA channel 2`
		1F94R

ES22	Description (added 4/16/1996): Normally, if the PLL disabled, the PCAP pin may be connected to V_{CC}, to Ground, or be left floating. However, this device has a latchup sensitivity on the PCAP pin. Workaround: Do not connect the PCAP pin to Ground. If the PLL is not being used, PCAP may be connected to V_{CC} or be left floating. There is no possibility of latchup if a capacitor is the only connection to PCAP.	1F94R
ES24	Description (added 6/26/1996): Trace mode (TME bit is set in OSCR) does not work properly during REP instruction execution. Workaround: Host debugging software should disable tracing during REP instruction execution and enable it only after the whole REP cycle is complete. If the debugging software does not disable tracing during REP instruction execution, the user must ensure that programs do not enter the trace mode while executing a REP instruction.	1F94R

Errata Number	Errata Description	Applies to Mask
ES27	Description (added 9/10/1996): If the chip is in the Debug mode and the $\overline{\text{RESET}}$ pin is asserted to bring the chip into Normal mode without asserting $\overline{\text{TRST}}$ at the same time, the chip status will continue to be read as “Debug” mode instead of the expected “User” mode, when the status is read afterwards through the JTAG port. Workaround: Assert the $\overline{\text{TRST}}$ pin while asserting the $\overline{\text{RESET}}$ pin.	1F94R
ES28	Description (added 9/10/1996): If the chip is in the Debug mode and the $\overline{\text{TRST}}$ pin is asserted, the chip status will show the chip status as “User” mode instead of the expected “Debug” mode, when the status is read afterwards through the JTAG port,. Workaround: Execute the following JTAG commands before reading the JTAG status: a) Enable OnCE b) DEBUG request Afterwards, the status bits will reflect the actual status of the chip and the $\overline{\text{DE}}$ pin will acknowledge “re-entering” the Debug mode.	1F94R

Errata Number	Errata Description	Applies to Mask
ES30	Description (added 11/18/96): After the $\overline{BB}$ pin output is driven high and released, the pin output voltage level may not reach V_{CC}. The issue depends on the application board layout and the parameters of the chip process. Workaround: Use a restricted board layout that includes a 1 kΩ pull-up resistor connected to the $\overline{BB}$ pin with a 100 Ω resistor connected in series with, and as close as possible to, the pin. The board route from the $\overline{BB}$ pin to any component should guarantee the following parameters: a. Route inductance < 40 nH b. Route capacitance < 15 pF c. Input capacitance < 8 pF Such restrictions guarantee that when $\overline{BB}$ is driven high (deasserted), the output voltage level will be above 2.25 V at V_{CC} = 3.3 V.	1F94R
ES33	Description (added 3/3/1997): When using the JTAG instructions SAMPLE/PRELOAD, EXTEST, and CLAMP, erroneous data may be driven out on the parallel pins and TDO. Data cannot be shifted through the Boundary Scan Register (BSR) using the SAMPLE/PRELOAD instruction. Because the BSR must be preloaded using the SAMPLE/PRELOAD instruction, the EXTEST and CLAMP instructions cannot be used for testing the board connections. Workaround: None available.	1F94R

Errata Number	Errata Description	Applies to Mask
ES54	Description (added 1/27/98): When a DMA channel is configured using its DMA Control Register (DCR) in the following manner: • Line Transfer mode is selected (DTM[2:0] = 010) • Non-Three-Dimensional Address mode is selected (D3D = 0) • Destination Address Offset Register DOR1 or DOR3 is selected (DAM[5:3] = 001 or 011) • No Source Address Offset is selected (DAM[2:0] = 100 or 101) The DMA transfer does not function as intended. Workaround: Select Destination Address Offset Register DOR0 or DOR2 by setting DAM[5:3] = 000 or 010.	1F94R
ES56	Description (added 2/18/1996): JTAG-related errors: The reset value of the JTAG Instruction Register is 1 (SAMPLE/PRELOAD), instead of 2 (IDCODE) which is required by the standard. Workaround: Not available	1F94R
ES59	Description (added 2/18/1996): JTAG-related errors: The user may not write the OnCE™ Command Register (OCR) when in a daisy-chain configuration. Workaround: Write OCR register while keeping all the other devices in BYPASS.	1F94R
ES60	Description (added 2/18/1996): JTAG-related errors: The data in the $\overline{BL}$ pin, Port A data bus D[23:0], and the HI32 pins HP[50:0] might be erroneous in EXTEST JTAG mode. Workaround: Do not use EXTEST for these pins.	1F94R

Errata Number	Errata Description	Applies to Mask
ES61	Description (added 2/18/1996): JTAG-related errors: After exiting EXTEST, a false debug request might be received. Workaround: After exiting EXTEST, assert $\overline{\text{TRST}}$ pin (Test Reset) before normal activity.	1F94R
ES62	Description (added 5/12/1997): Expansion Port does not provide proper Dynamic RAM support. Workaround: Not available	1F94R
ES64	Description (added 2/10/1997): When using the 5 V-tolerant pin in open drain mode (i.e., $\overline{\text{DE}}$, $\overline{\text{HREQ}}$/$\overline{\text{HTRQ}}$, $\overline{\text{HACK}}$/$\overline{\text{HRRQ}}$ and TXD), the chip clamps the voltage at the pin to about V_{CC} + 0.4 V. Workaround: Not available.	1F94R
ES65	Description (added 2/18/1996): Memory Switch mode is not functional in the DSP56303/Rev0 (0F94R, 1F94R). Workaround: Not available	1F94R
ES66	Description (added 4/16/1996): DMA transfers from the external memory space to the internal or to the external memory space require four (or more) wait states. Note: Transfers from internal memory space are not affected. Workaround: Program four or more wait states for all DMA transfers from the external memory space.	1F94R

Errata Number	Errata Description	Applies to Mask
ES67	Description (added 4/16/1996): After the HC bit is set by the host processor writing to the HCVR, the Host Command interrupt is executed as defined by the specification. However, if the host processor performs a read access from the HI08 port concurrently with the servicing the Host Command interrupt request by the DSP core, the HC bit in the ISR may remain set even after the HCP status bit in the HSR is cleared. Workaround: Either of the following alternatives may be used: a. Do not allow the host processor to read any HI08 register while the DSP is servicing the Host Command interrupt request. b. Use a handshake protocol with host flags instead of polling the HC bit in the ISR. A host flag (in the HCR) should be changed by the DSP (e.g., using the BCHG instruction) while performing the Host Command interrupt service routine. The host processor should read the corresponding host flag (in the ISR) before writing a new Host Command to the HCVR and then poll this flag for the change. When the flag is changed, signifying that the DSP has serviced the HC interrupt request, the host processor may clear the HC bit or send a new Host Command.	1F94R
ES68	Description (added 5/7/1996): Device operation is normally guaranteed to +85°C ambient temperature. Due to speed paths on this silicon, the ambient temperature can only be guaranteed up to +60°C. Workaround: Not available.	1F94R

Errata Number	Errata Description	Applies to Mask

ES84	Description (added 5/13/98):
	
	When software disables a DMA channel (by clearing the DE bit of the DCR) , the DTD status bit of the channel may not be set if any of the following events occur:
	
	a. Software disables the DMA channel just before a conditional transfer stall (Described by App B-3.5.1,UM).
	
	b. Software disables the DMA channel at the end of the block transfer (that is after the counter is loaded with its initial value and transfer of the last word of the block is completed).
	
	As a result, the Transfer Done interrupt might not be generated.
	
	Workaround:
	Avoid using the instruction sequence causing the conditional transfer stall (See DSP56300 UM, App B-3.5.1 for description) in fast interrupt service routines. Every time the DMA channel needs to be disabled by software, the following sequence must be used :
	
	`bclr #DIE,x:M_DCR ; not needed if DIE is cleared`
	`bclr #DE,x:M_DCR`
	`; instead of two instructions above, one 'movep' instruction may be used`
	`; to clear DIE and DE bits`
	`movep #DCR_Dummy_Value,x:M_DCR`
	`bclr #DE,x:M_DCR`
	`nop`
	`nop`
	
	Here, the `DCR_Dummy_value` is any value of the DCR register that complies with the following requirements:
	
	• DE is set;
	• DIE is set if Transfer Done interrupt request should be generated and cleared otherwise;
	• DRS[4:0] bits must encode a reserved DMA request source (see the following list of reserved DRS values);
	
	List of reserved DRS[4:0] values (per device):
	
	• DSP56302, DSP56309, DSP56303, DSP56304, DSP56362 — `10101-11111`
	• DSP56305 — `11011`
	• DSP56301 — `10011-11011`
	• DSP56307 — `10111-11111`
		1F94R

Errata Number	Errata Description	Applies to Mask
ES89	Description (added 6/25/98): If the SCI Receiver is programmed to work with a different serial clock than the SCI Transmitter so that either the Receiver or Transmitter is using the external serial clock and the other is using the internally-generated serial clock—RCM and TCM in the SCCR are programmed differently)—then the internal serial clock generator will not operate and the SCI portion (Receiver or Transmitter) clocked by the internal clock will be stuck. Workaround: Do not use SCI with the two SCI portions (Receiver and Transmitter) clocked by different serial clocks; use either both externally or both internally clocked. Or: When using both portions of the SCI (Receiver & Transmitter), do not program different values on RCM and TCM in the SCCR.	1F94R

Errata Number	Errata Description	Applies to Mask

ES91	Description (added 7/22/98):
	
	If the Core reads data from the HRX while instructions are fetched from the memory Expansion Port (Port A) using 2 or more wait states, data may be lost.
	
	Workaround :
	
	There are three possible workarounds:
	
	1) The host should guarantee that there is no more than one word in the TXH:TXM:TXL-HRX data path at any time. This can be achieved if the host writes a word to the HI08 only when the TRDY flag is set (i.e. the data path is empty).
	
	2) Use a service routine running from fast (i.e. one wait state) external memory or internal memory to read the HRX read code; ensure that code that is fetched from slow (i.e. more than 1 wait state) external memory is located at least 4 instructions after the HRX register is read. For example:
	
	`READ_HRX_DATA`
	`NOP`
	`NOP`
	`NOP`
	`NOP`
	
	Note:
	
	a) Interrupt requests that fetch instructions from slow external memory should be masked during this service routine. Nonmaskable interrupt (NMI) request routines must not be in external memory.
	
	b) If running from fast external memory and if a DMA channel accessing external memory is used, then the DMA may cause extra wait states to the core. Thus, the DMA should have a lower priority than the core so that the core can access the external memory with no more than 1 wait state.
	
	c) Read the HRX using one of the channels of the on-chip DMA controller.
		1F94R

Errata Number	Errata Description	Applies to Mask
ES95	Description (added 8/15/98): If more than a single DMA channel is enabled while the DSP stays in the WAIT processing state, and triggering one of the DMA channels causes an exit from the WAIT state (See A-6.115, UM), triggering another DMA channel might cause improper DMA operation. Workaround: Assure that only a single DMA channel can be triggered during DSP WAIT state. If the application cannot guarantee this, other DMA channels should be disabled before the WAIT processing state is entered and then reenabled after WAIT state is exited.	1F94R
ES104	Description: (added 11/24/98): An improper operation may occur when all the following conditions apply: • The DMA channel is in a mode that does not automatically clear the DE bit at the end of the block (DTM[2:0] = 1xx in DCR). • This channel is disabled by software (by clearing DE in DCR) while it is triggered for a new transfer. • The previous operation is not yet completed. Workaround: The DMA channel should be disabled only when it is not triggered for a new transfer, i.e. when the DACT bit in the DSTR register is cleared. **Note:** To perform this operation most efficiently, all other DMA channels should be disabled.	1F94R

Errata Number	Errata Description	Applies to Mask

ES105	Description (added 11/25/98):
	
	If the core clears HCIE bit on HCR register, while the interrupt was issued, and the vector was read by the interrupt controller, then when the interrupt is serviced, HCP will not be cleared, since the clear equation is conditioned by HCIE=1.
	
	Workaround :
	
	There are two possible workarounds:
	
	1) If only host commands are used as possible interrupt source to the CORE (i.e. HTIE and HRIE are both 0), then instead of bit-set and bit-clear to HCIE, do bit-set and bit-clear instructions on IPRP register for the HIE bit.
	
	2) If option "1" can not be used, then the user should first turn off host interrupt requests (all the possible sources) by clearing HIE bit on IPRP register, then issue 6 NOP instructions, then clear HCIE bit on HCR, issue another 6 NOP instructions and finally re-enable the HIE bit on IPRP as shown below:
	
	`;; Clear the relevant bits on IPRP register acording to`
	`;; the current host interrupt priority settings`
	
	`BCLR #M_HPL0,x:M_IPRP`
	`BCLR #M_HPL1,x:M_IPRP`
	`;; Issue 6 NOP instructions`
	`NOP`
	`NOP`
	`NOP`
	`NOP`
	`NOP`
	`NOP`
	`;; Clear the HCR[HCIE] bit to turn off host commands`
	`BCLR #M_HCIE,x:M_HCR`
	`;; Issue 6 NOP instructions`
	`NOP`
	`NOP`
	`NOP`
	`NOP`
	`NOP`
	`NOP`
	`;; Restore the required host interrupt level`
	`BSET #M_HPL0,x:M_IPRP`
	`BSET #M_HPL1,x:M_IPRP`
		1F94R

Errata Number	Errata Description	Applies to Mask
ES114	Description (added 4/19/99, revised 4/30/99): A DMA channel may operate improperly when the address mode of this channel is defined as three-dimensional (D3D=1) and DAM[5:0] = 1xx 1 10 or DAM[5:0] = 01xx 10 (i.e., triple counter mode is E). Workaround: Use the triple counter modes C(DAM[1:0]=00) or D(DAM[1:0]=01) instead of the E(DAM[1:0]=10) mode.	1F94R

ES115	Description (added 4/19/99):
	
	When a DMA channel (called channel A) is disabled by software clearing the channel's DCR[DE] bit, the DTD bit may not get set, and the DMA end of the block interrupt may not happen if one of the following occurs:
	
	1. There is another channel (channel B) executing EXTERNAL accesses, and the DE bit of channel A is being cleared by software at the end of the channel B word transfer - if channel B is in Word transfer mode, or at the end of the channel B line transfer - if channel B is in Line Transfer mode, or at the end of the channel B block transfer - if channel B is in Block transfer mode.
	
	2. This channel (A) is executing EXTERNAL accesses, and the DE bit of this channel (A) is being cleared by software at the end of the channel B word transfer - if channel B is in Word transfer mode, or at the end of the channel B line transfer - if channel B is in Line transfer mode.
	
	Workaround:
	
	Avoid executing a DMA external access when any DMA channel should be disabled. This can be done as follows. Every time the DMA channel needs to be disabled by software, the following sequence must be used:
	
	`;; initialize an unused DMA channel "C"`
	`movep #DSR_swflag, x:M_DSRC ;; here DSR_swflag is an`
	`;; unused X, Y or P memory`
	`;; location, should`
	`;; be initialized to`
	`;; $800000`
	`;; M_DSRC - address of the`
	`;; channel C DSR register.`
		1F94R

Errata Number	Errata Description	Applies to Mask
ES115 cont.	movep #DDR_swflag, x:M_DDRC ;; DDR_swflag is an unused ;; X, Y or P memory ;; location, should be ;; initialized to $000000 ;; M_DDRC - ;; address of the channel C ;; DDR register . movep #TR_LENGTH, x:M_DCOC ;; see below the definition ;; of the TR_LENGTH value, ;; M_DCOC - address ;; of the channel C DCO register .movep #1f0240, x:M_DCRC ;; M_DCRB - address of the ;; channel C DCR register. ;; Set transfer mode - ;; block transfer, ;; triggered by ;; software highest ;; priority, continuous ;; mode on no-update ;; source and destination ;; address mode X memory ;; location for source ;; and destination (can be ;; chosen by ;; user accordingly to ;; DSR_swflag/DDR_swflag)	1F94R

Errata Number	Errata Description	Applies to Mask
ES115 cont.	;; disable DMA channel "A" ori #3, mr ;; mask all interrupts bset #23, x:M_DCRC ;; enable DMA channel C bclr #23,x:DDR_swflag,* ;; wait until DMA channel C ;; begin transfer bclr #23, x:M_DCRA ;; disable DMA channel A nop nop jclr #M_DTDA, x:M_DSTR,* ;; polling DTD bit of the DMA ;; channel A, The TR_LENGTH value can be defined as the maximum length of the external DMA transfer—from the length of the read DMA cycle and from the length of the write DMA cycle. The length of the external read/write DMA cycle can be defined as the length of the PORTA external access. The length of the internal read/write DMA cycle can be defined in the errata case as 2 DSP clock cycles. The TR_LENGTH can be found as sum of the lengths of the DMA read and DMA write cycles.	1F94R

DOCUMENTATION ERRATA

Errata Number	Errata Description	Applies to Mask

ED1	Description (revised 11/9/98):
	
	XY memory data move does not work properly if the X-memory move destination is internal I/O and the Y-memory move source is a register used as destination in the previous adjacent move from non Y-memory OR the Y-memory move destination is a register used as source in the next adjacent move to non Y-memory.
	
	Here are examples of the two cases (where x:(r1) is a peripheral):
	
	Example 1:
	
	`move #$12,y0`
	`move x0,x:(r7) y0,y:(r3) (while x:(r7) is a peripheral).`
	
	Example 2:
	
	`mac x1,y0,a x1,x:(r1)+ y:(r6)+,y0`
	`move y0,y1`
	
	This is not a bug, but a documentation update. Any of the following alternatives can be used:
	
	a. Separate these two consecutive moves by any other instruction.
	
	b. Split XY Data Move to two moves.
		1F94R

ED3	Description (added 5/7/1996): A one-word conditional branch instruction at LA-1 is not allowed. This is not a bug, but a documentation update.	1F94R
ED4	Description (added 11/11/1996): The following instructions should not start at address LA: MOVE to/from Program space {MOVEM, MOVEP (only the P space options)} This is not a bug but a documentation update (Appendix B, DSP56300 Family Manual).	1F94R

ED7	Description (added 1/27/98): When activity is passed from one DMA channel to another and the DMA interface accesses external memory (which requires one or more wait states), the DACT and DCH status bits in the DMA Status Register (DSTR) may indicate improper activity status for DMA Channel 0 (DACT = 1 and DCH[2:0] = 000). Workaround: None. This is not a bug, but a specification update.	1F94R
ED9	Description (added 1/27/98): When the SCI is configured in Synchronous mode, internal clock, and all the SCI pins are enabled simultaneously, an extra pulse of 1 DSP clock length is provided on the SCLK pin. Workaround: a. Enable an SCI pin other than SCLK. b. In the next instruction, enable the remaining SCI pins, including the SCLK pin. This is not a bug, but a specification update.	1F94R
ED15	Description (added 7/21/98): The DRAM Control Register (DCR) should not be changed while refresh is enabled. If refresh is enabled only a write operation that disables refresh is allowed. Workaround: First disable refresh by clearing the BREN bit, than change other bits in the DCR register, and finally enable refresh by setting the BREN bit.	1F94R
ED17	Description (added 9/28/98): In all DSP563xx technical datasheets, a note is to be added under "AC Electrical Characteristics" that although the minimum value for "Frequency of Extal" is 0MHz, the device AC test conditions are 15MHz and rated speed. Workaround: N/A	1F94R

ED20	Description (added 11/24/98): In the Technical Datasheet Voh-TTL should be listed at 2.4 Volts, not as: `TTL = Vcc-0.4` Workaround: This is a documentation update.	1F94R
ED21	Description (added 11/24/98): In the Technical Datasheet Iol should be listed as 1.6 mA, not as 3.0 mA. Workaround: This is a documentation update.	1F94R
ED24	Description (added 11/24/98): The technical datasheet supplies a maximum value for internal supply current in Normal, Wait, and Stop modes. These values will be removed because we will specify only a "Typical" current. Workaround: This is a documentation update.	1F94R
ED26	Description (added 1/6/99): The specification DMA Chapter is wrong. “Due to the DSP56300 Core pipeline, after DE bit in DCRx is set, the corresponding DTDx bit in DSTR will be cleared only after two instruction cycles.” Should be replaced with: “Due to the DSP56300 Core pipeline, after DE bit in DCRx is set, the corresponding DTDx bit in DSTR will be cleared only after three instruction cycles.”	1F94R

ED28	Description (added 1/7/1997; identified as Documentation Errata 2/1/99):
	
	When two consecutive LAs have a conditional branch instruction at LA-1 of the internal loop, the part does not operate properly. For example, the following sequence may generate incorrect results:
	
	`DO #5, LABEL1`
	`NOP`
	`DO #4, LABEL2`
	`NOP`
	`MOVE (R0) +`
	`BSCC _DEST ; conditional branch at LA-1 of internal loop`
	`NOP ; internal LA`
	`LABEL2`
	`NOP ; external LA`
	`LABEL1`
	`NOP`
	`NOP`
	`_DEST NOP`
	`NOP`
	`RTS`
	
	Workaround: Put an additional NOP between LABEL2 and LABEL1.
	
	Pertains to: DSP56300 Family Manual, Appendix B, Section B-4.1.3, "At LA-1."
		1F94R

ED29	Description (added 9/12/1997; identified as a Documentation errata 2/1/99): When the ESSI transmits data with the CRA Word Length Control bits (WL[2:0]) = 100, the ESSI is designed to duplicate the last bit of the 24-bit transmission eight times to fill the 32-bit shifter. Instead, after shifting the 24-bit word correctly, eight 0s are being shifted. Workaround: None at this time. **Pertains to:** UM, Section 7.4.1.7, "CRA Word Length Control." The table number is 7-2.	1F94R

ED30	Description (added 9/12/1997; identified as a Documentation errata 2/1/99): When the ESSI transmits data in the On-Demand mode (i.e., MOD = 1 in CRB and DC[4:0] = $00000 in CRA) with WL[2:0] = 100, the transmission does not work properly. Workaround: To ensure correct operation, do not use the On-Demand mode with the WL[2:0] = 100 32-bit Word-Length mode. **Pertains to:** UM, Section 7.5.4.1, "Normal/On-Demand Mode Selection."	1F94R
ED31	Description (added 9/12/1997; modified 9/15/1997; identified as a Documentation errata 2/1/99): Programming the ESSI to use an internal frame sync (i.e., SCD2 = 1 in CRB) causes the SC2 and SC1 signals to be programmed as outputs. If however, the corresponding multiplexed pins are programmed by the Port Control Register (PCR) to be GPIOs, then the GPIO Port Direction Register (PRR) chooses their direction, but this causes the ESSI to use an external frame sync if GPIO is selected. **Note:** This errata and workaround apply to both ESSI0 and ESSI1. Workaround: To assure correct operation, either program the GPIO pins as outputs or configure the pins in the PCR as ESSI signals. **Note:** The default selection for these signals after reset is GPIO. **Pertains to:** UM, Section 7.4.2.4, "CRB Serial Control Direction 2 (SCD2) Bit 4"	1F94R

ED32	Description (added 11/9/98; identified as a Documentation errata 2/1/99):
	
	When returning from a long interrupt (by RTI instruction), and the first instruction after the RTI is a move to a DALU register (A, B, X, Y), the move may not be correct, if the 16-bit arithmetic mode bit (bit 17 of SR) is changed due to the restoring of SR after RTI.
	
	Workaround:
	
	Replace the RTI with the following sequence:
	
	`movec ssl,sr`
	`nop`
	`rti`
	
	Pertains to: DSP56300 Family Manual. Add a new section to Appendix B that is entitled “Sixteen-Bit Compatibility Mode Restrictions.”
		1F94R

ED33	Description (added 12/16/98; identified as a Documentation errata 2/1/99):
	
	When Stack Extension mode is enabled, a use of the instructions BRKcc or ENDDO inside do loops might cause an improper operation.
	
	If the loop is non nested and has no nested loop inside it, the erratais relevant only if LA or LC values are being used outside the loop.
	
	Workaround:
	
	If Stack Extension is used, emulate the BRKcc or ENDDO as in the following examples. We split between two cases, finite loops and do forever loops.
	
	1) Finite DO loops (i.e. not DO FOREVER loops)
	
	==========
	
	BRKcc
	
	Original code:
	
	`do #N,label1`
	`.....`
	`.....`
	`do #M,label2`
	`.....`
	`.....`
	`BRKcc`
	`.....`
	`.....`
	`label2`
	`.....`
	`.....`
	`label1`
	
	Will be replaced by:
	
	`do #N, label1`
	`.....`
	`.....`
	`do #M, label2`
	`.....`
	`.....`
	`Jcc fix_brk_routine`
	`.....`
	`.....`
		1F94R

ED33 cont.	nop_before_label2 nop ; This instruction must be NOP. label2 .... label1 .... fix_brk_routine move #1,lc jmp nop_before_label2 ENDDO ------ Original code: do #M,label1 .... do #N,label2 .... ENDDO .... label2 .... label1 Will be replaced by: do #M, label1 .... do #N, label2 .... JMP fix_enddo_routine	1F94R

ED33 cont.	nop_after_jmp NOP ; This instruction must be NOP. .... label2 .... label1 .... fix_enddo_routine move #1,lc move #nop_after_jmp,la jmp nop_after_jmp 2) DO FOREVER loops ========== BRKcc ----- Original code: do #M,label1 .... do forever,label2 .... BRKcc .... label2 .... label1	1F94R

ED33 cont.	Will be replaced by: do #M,label1 .... do forever,label2 .... JScc fix_brk_forever_routine ; <--- note: JScc and not Jcc .... nop_before_label2 nop ; This instruction must be NOP. label2 .... label1 .... fix_brk_forever_routine move ssh,x:<..> ; <..> is some reserved not used address (for temporary data) move #nop_before_label2,ssh bclr #16,ssl ; move #1,lc rti ; <---- note: "rti" and not "rts" ! ENDDO ------ Original code: do #M,label1	1F94R

	do forever,label2 .... ENDDO .... label2 .... label1 Will be replaced by: do #M,label1 .... do forever,label2 .... JSR fix_enddo_routine ; <--- note: JSR and not JMP nop_after_jmp NOP ; This instruction should be NOP .... label2 .... label1 .... fix_enddo_routine nop move #1,lc bclr #16,ssl move #nop_after_jmp,la rti ; <--- note: "rti" and not "rts" **Pertains to:** DSP56300 Family Manual, Section B-4.2, “General Do Restrictions.”	1F94R

ED34	Description (added 1/5/99; identified as a Documentation errata 2/1/99): When stack extansion is enabled, the read result from stack may be improper if two previous executed instructions cause sequential read and write operations with SSH. Two cases are possible: Case 1: For the first executed instruction: move from SSH or bit manipulation on SSH (i.e. jclr, brclr, jset, brset, btst, bsset, jsset, bsclr, jsclr). For the second executed instruction: move to SSH or bit manipulation on SSH (i.e. jsr, bsr, jscc, bscc). For the third executed instruction: an SSL or SSH read from the stack result may be improper - move from SSH or SSL or bit manipulation on SSH or SSL (i.e., bset, bclr, bchg, jclr, brclr, jset, brset, btst, bsset, jsset, bsclr, jsclr). Workaround: Add two NOP instructions before the third executed instruction. Case 2: For the first executed instruction: bit manipulation on SSH (i.e. bset, bclr, bchg). For the second executed instruction: an SSL or SSH read from the stack result may be improper - move from SSH or SSL or bit manipulation on SSH or SSL (i.e., bset, bclr, bchg, jclr, brclr, jset, brset, btst, bsset, jsset, bsclr, jsclr). Workaround: Add two NOP instructions before the second executed instruction. **Pertains to:** DSP56300 Family Manual, Appendix B, add a new section called “Stack Extension Enable Restrictions.” Cover all cases. Also, in Section 6.3.11.15, add a cross reference to this new section.	1F94R

ED38	Description (added 7/14/99): If Port A is used for external accesses, the BAT bits in the AAR3-0 registers must be initialized to the SRAM access type (i.e. BAT = 01) or to the DRAM access type (i.e. BAT = 10). To ensure proper operation of Port A, this initialization must occur even for an AAR register that is not used during any Port A access. Note that at reset, the BAT bits are initialized to 00. **Pertains to:** *DSP56300 Family Manual*, Port A Chapter (Chapter 9 in Revision 2), description of the BAT[1 –0] bits in the AAR3 - AAR0 registers. Also pertains to the core chapter in device-specific user's manuals that include a description of the AAR3 - AAR0 registers with bit definitions (usually Chapter 4).	1F94R

ED40	Description (added 11/11/99):
	When an instruction with all the following conditions follows a repeat instruction, then the last move will be corrupted.:
	1. The repeated instruction is from external memory.
	2. The repeated instruction is a DALU instruction that includes 2 DAL registers, one as a source, and one as destination (e.g. tfr, add).
	3. The repeated instruction has a double move in parallel to the DALU instruction: one move's source is the destination of the DALU instruction (causing a DALU interlock); the other move's destination is the source of the DALU instruction.
	Example:
	rep #number
	tfr x0,a x(r0)+,x0 a,y0 ; This instruction is from external memory
	|__|_____|------|----------> This is condition 3 second part.
	|_____|----------> This is condition 3, first part - DALU interlock
	In this example, the second iteration before the last, the "x(r0)+,x0" doesn't happen. On the first iteration before the last, the X0 register is fixed with the "x(r0)+,x0", but the "tfr x0,a" gets the wrong value from the previous iteration's X0. Thus, at the last iteration the A register is fixed with "tfr x0,a", but the "a,y0" transfers the wrong value from the previous iteration's A register to Y0.
	Workaround:
	1. Use the DO instruction instead; mask any necessary interrupts before the DO.
	2. Run the REP instructions from internal memory.
	3. Don't make DALU interlocks in the repeated instruction. After the repeat make the move. In the example above, all the "move a,y0" are redundant so it can be done in the next instruction:
	`rep #number`
	`tfr x0,a x(r0)+,x0`
	`move a,y0`
	If no interrupts before the move is a must, mask the interrupts before the REP. **Pertains to:** *DSP56300 Family Manual*, Rev. 2, Section A.3, "Instruction Sequence Restrictions."
		1F94R

ED42	Description (added on 3/22/2000) The DMA End-of-Block-Transfer interrupt cannot be used if DMA is operating in the mode in which DE is not cleared at the end of the block transfer (DTM = 100 or 101). **Pertains to:** *DSP56300 Family Manual*, Rev. 2, Section 10.4.1.2, "End-of-Block-Transfer Interrupt." Also, Section 10.5.3.5, "DMA Control Registers (DCR[5–0]," discussion of bits 21 – 19 (DTM bits).	1F94R
ED50	Description (added 9/10/1996 as ES29; reclassified as a documentation erratum on 8/2/2002): When the SCI transmitter is used in Synchronous mode, the last bit of the transmitted byte might be truncated to the half of the serial cycle. Workaround: Not available.	1F94R

NOTES

1. An over-bar (i.e., $\overline{xxxx}$) indicates an active-low signal.
2. The letters seen to the right of the errata tell which DSP56303 mask numbers apply.
3. The Motorola DSP website has additional documentation updates that can be accessed at the following URL:

   http://www.mot.com/SPS/DSP/home/eng/tec/doc_update.html

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