MOTOROLA

Chip Errata
DSP56002 Digital Signal Processor
Mask: D41G

ERRATA

	Errata Description	Applies to Mask
1.	Timing 170 is not guaranteed for a period of 1000 ETc after PLOCK assertion following the events listed below: a. When enabling the PLL operation by software. b. When changing the multiplication factor. c. When recovering from the STOP state if the PLL was turned off and it is supposed to turn-on when exiting the STOP state.	D41G
2.	The timing of the acknowledge pulse (timing 240 in the data sheet) on the OnCE DSO line is too short by 3Tc. The correct timing should be 4Tc+Th-3ns (min) and 5Tc+7ns (max).	D41G
3.	If the CKP pin is connected to GND and the PLL is disabled and the PSTP bit in the PLL control register is set and the CKOUT clock output is enabled, then when recovering from the STOP state, a negative-going spike may occur in the CKOUT pin. Workaround: disable CKOUT before entering the STOP state. After exiting the STOP state, enable CKOUT.	D41G
4.	If the PLL is enabled and DF>1 and CKOS≠CSRC then when enabling or disabling CKOUT, a spike may occur on CKOUT.	D41G
5.	If the PLL is enabled and DF>1 and CKOS≠CSRC then when entering the STOP state, a spike may occur on CKOUT.	D41G

	Errata Description	Applies to Mask
6.	If CKOUT is enabled when the chip enters the STOP state, CKOUT is held high instead of being held constant at the same logic level which was true at the moment the clocks were frozen in the DSP.	D41G
7.	Disabling CKOUT will set it high immediately even if the CKOUT clock level was low at this moment, instead of completing the “low” cycle and then be disabled high.	D41G

NOTES

1. An over-bar (i.e. $\overline{xxxx}$) indicates an active-low signal.
2. The letters seen to the right of the errata tell which DSP56002 mask numbers apply.

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