Mask Set Errata for Mask 0N27B

Introduction

This report applies to mask 0N27B for these products:

- COLDFIREPLUS

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e4395: ADC: ADC input channel 27 is connected to bandgap instead of VREF_OUT

Errata type: Errata

Description: ADC input channel 27 is connected to the internal bandgap voltage (1 V), not VREF_OUT as is documented in the Reference Manual's ADC channel assignments table.

Workaround: If a measurement of VREF_OUT is needed, route the VREF_OUT signal to any other ADC input channel that has an external connection.

e3367: Debug: BKGD pin has low drive strength enabled by default

Errata type: Errata
Description: The BKGD pin has low drive strength and pin filtering enabled by default, which can cause lost or erratic communication with the debugger.

Workaround: The default settings of the BKGD pin are sufficient for reset clock frequencies. If higher frequency operation is required,

1) enable the high drive strength of the pin by setting the PTDS bit to 1 in the PCTLn_DS register and

2) disable the pin filter by writing a 0 to bit 4 of the PCTLB_PFE register corresponding to the BKGD port pin,

3) or add an external pullup resistor on the BKGD pin.

e2792: EzPort: COP is enabled in EzPort mode, leading to system resets

Errata type: Errata
Description: When EzPort mode is entered, the COP watchdog is not disabled and continues counting. After the COP times out, a system reset is generated.

Workaround: Do not use EzPort mode. If EzPort mode must be used, all command execution times must be shorter than the COP timeout period.

e3374: FTFL: Erase operation is not reliable if VDD is approximately 1.9 V or less

Errata type: Errata
Description: Insufficient high voltage charge pump capacity causes an unreliable flash-memory erase capability over temperature if VDD is approximately 1.9 V or less.

Workaround: Maintain VDD above 1.9 V for proper flash-memory erase operations.

e3372: FTFL: Reset during an EEE program operation may result in an invalid EEE read access

Errata type: Errata
Description: In rare occurrences, a reset during an EEE program operation may result in invalid EEE read access.

Workaround: Avoid a reset during EEE programming.

e2793: I2C: MCU does not wake from stop mode on subsequent address matches if previous address is mismatched

Errata type: Errata
Description: The I2C module, acting as a slave on the I2C bus, does not wake from normal stop mode on a valid address match if the previous address was not a match.

When the external I2C master sends a nonmatching address, the I2C slave state machine does not correctly idle the I2C module. Subsequent transmissions by the I2C master with a matching address do not wake the MCU from stop mode via the I2C interrupt.

Workaround: There are multiple workarounds:

(1) When the MCU, operating as an I2C slave, is in stop mode: Ensure that the external I2C master sends a matching address to wake the slave MCU before it sends any transaction to other I2C slaves.

(2) When the MCU, operating as an I2C slave, is in stop mode: If a mismatched slave address is sent by the external I2C master, which puts the slave I2C module into the invalid I2C state, disable and then re-enable the slave I2C to reset the I2C state machine.

(3) To bypass the stop mode wakeup issue: Enable the port interrupt function, which shares the pin function with the SDA input, to cause an interrupt on the falling edge of the SDA input signal {start}. This approach puts the MCU in run mode for the address match comparison.

e3528: LVD reset in stop mode

Errata type: Errata
Description: When the MCU is in stop mode, if a low voltage detect (LVD) event occurs and the LVD is configured to generate a reset (the PMC_LVDSC1[LVDRE] bit is 1), the reset does not occur to wake the MCU from stop mode.

Workaround: Disable LVD reset in stop mode and enable the LVD interrupt. In this case, if a low-voltage event occurs in stop mode, the event generates an interrupt. In the LVD interrupt service routine, a software reset can be generated.

e3353: MCG: Slow IRC does not achieve specified range

Errata type: Errata
Description: The operating range of the slow internal reference clock (slow IRC) does not achieve the Data Sheet specification of 39.0625 kHz. The maximum frequency of the slow IRC is less than 34.2 kHz. When using the MCG FLL with the slow IRC as the source clock, only the range of 31.25 kHz to 34.153 kHz should be used.

Workaround: For most desired end frequency ranges, the slow IRC range of 31.25 kHz to 34.153 kHz is sufficient if you set the MCG module's C4[DMX32] bit for a larger multiplier value. For example, using 34.153 kHz and setting the DMX32 bit to 1 can achieve an end frequency of 25 MHz or 50 MHz.

e3384: Mini-FlexBus: False bus error on back-to-back writes when flash memory is secure

Errata type: Errata
Description: During back-to-back writes, the Mini-FlexBus incorrectly responds with a bus error on the second write when both of these conditions apply: the flash memory is secure (per the value of the FTFL module's FSEC[SEC] field), and the SIM's SOPT6[MBSL] field is 10b. This setting of the SOPT6[MBSL] field disallows instruction accesses but allows data accesses on the Mini-FlexBus interface when the flash memory is secure.

Workaround: When the flash memory is secure and Mini-FlexBus instruction accesses are inhibited but data accesses are allowed, do not use back-to-back writes. Insert a delay or NOP instruction between the write operations.

e2783: Mini-FlexBus: Operation fails under conditions when flash memory is secure

Errata type: Errata

Description: The Mini-FlexBus module stops operating under specific conditions when the flash memory is secure. The secure state depends on the value of the FTFL module's FSEC[SEC] field.

When the flash memory is secure and the SIM's SOPT6[MBSL] field is 00b or 01b, the Mini-FlexBus module stops operating upon any attempted data or instruction access using the Mini-FlexBus interface.

When the flash memory is secure and the SIM's SOPT6[MBSL] field is 10b, the Mini-FlexBus module stops operating upon any attempted instruction fetch using the Mini-FlexBus interface.

Workaround: When the flash memory is secure, accesses on the Mini-FlexBus interface cannot be restricted. Accesses on the Mini-FlexBus interface can occur when the flash memory is unsecure, or when the flash memory is secure but the SIM's SOPT6[MBSL] field is 11b to allow all instruction and data accesses.

e2801: POR flag in SRS0 register might not set for a POR

Errata type: Errata

Description: When a power-on reset (POR) occurs, the POR flag in the System Reset Status Register 0 (SRS0) might not set as expected. Instead, the result of the POR might be to set only the LVD flag in SRS0.

Workaround: If a POR must be detected, software can be used to read a register that is reset by the POR Only reset type, such as the System Register File registers or the PMC module's LVDSC1[LVDV] and LVDSC2[LVWV] bitfields. If these registers or bitfields are in their reset state, then a POR has occurred.

e2584: UART: Possible conflicts between UART interrupt service routines and DMA requests

Errata type: Errata

Description: If the UARTn_S1[RDRF] and/or UARTn_S1[TDRE] flags are being used to generate DMA requests, there is a possible conflict that could occur if an interrupt service routine (ISR) or other code is used to clear any of the other flags in the UARTn_S1 register. The flags in the UARTn_S1 register use a side effect clearing mechanism where the procedure is to read the status register and then perform a read or write of the data register to clear the flag. If a DMA request for a flag bit is asserted while an ISR for another flag bit is executing, then in the process of clearing the ISR's flag bit, the ISR can also clear the flag bit for the DMA request, thereby negating the DMA request before the DMA responds to it. This could potentially cause servicing of the DMA event to be missed.

For example, assume a DMA request is being asserted for the RDRF flag. At the same time, the parity error flag (PF) sets and triggers an ISR. To clear the PF flag bit, the ISR must read the status register and read the data register. In the process, the RDRF flag would also be

cleared, causing the DMA request to negate. If the DMA request asserts after the DMA has already prepared its next transfer, then it might still read from the data register, potentially causing an underflow.

Workaround: When possible, avoid enabling the UART for DMA requests and interrupts simultaneously. If error interrupts are needed while DMA requests are active, then the error ISR can be used to abort the current DMA transfer (by disabling the DMA request inside the UART and/or disabling the external request for the DMA channel) before clearing any error flags in the UARTn_S1 register.

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