Mask Set Errata 3
68HC705SR3 8-Bit Microcontroller Unit

INTRODUCTION

This mask set errata provides information pertaining to the analog-to-digital converter, IRQ2 and timer interrupts applicable to this 68HC705SR3 MCU mask set device:

- 1F10W

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0XJ66D. Slight variations to the mask set identification code may result in an altered version number, for example 1XJ66D.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "9115" indicates the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC or XC prefix. An SC prefix denotes special/custom device. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

When contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

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PD6 and PD7 During ADC Operation

Port pins PD6 and PD7 are disabled when the ADC is in use, i.e. ADON=1. In this case PD6 and PD7 data register bits will always read as 0 (zero).

$\overline{\text{IRQ2}}$ and Timer Interrupts

If an $\overline{\text{IRQ2}}$ interrupt arrives just after a latched timer interrupt, the CPU may load an incorrect interrupt vector. Instead of loading the timer interrupt vector at $1FF6–$1FF7, the CPU may load the incorrect vector at $1FF0–$1FF1. The $1FF0–$1FF1 are reserved vector locations.

To work around this abnormally, program the location $1FF0 with the same value as $1FF6, and $1FF1 with the same value as $1FF7.

This abnormally does not occur if $\overline{\text{IRQ2}}$ interrupt is disabled (IRQ2E=0).

Additional mask set erratas can be found on the World Wide Web at http://www.motorola.com/semiconductors/