PC68HC16Z3 DEVICE INFORMATION
(Issue 1 - 15 June, 1995)
Rev. A
1G26C Mask Set

The following information and errata pertain to Revision 0 samples of the MC68HC16Z1 microcontroller. This revision contains the following module versions: CPU16V9, SIMV14, GPTV2, QSMV11, ADCV11, SRAMV6, ROMV7.

The phrase "This is an erratum" following each item below identifies characteristics of the current silicon which are expected to be improved. "This is information only" refers to enhancements, clarifications, and changes to the documented descriptions of the microcontroller and the modules within.

MODULE DETAILS:

ADC:050

ADC: ADC 10 bit absolute accuracy is tested to +/- 2.5 counts with a 1.05 MHz ADC clock, 2 ADC clock sample period, single-channel conversions, Vrh/Vdd at 5.0 Volts, and Vrl/Vss at 0 Volts. This is information only.

ADC:050

CPU16:064

CPU16: If the SHEN bits in the integration module are set to %11, and if the external bus is arbitrated away (external BR asserted) during an IACK cycle, then the CPU will vector to an incorrect address and become lost.

CPU16:064

Workaround:

1. Set the integration module SHEN bits to any combination except %11, if bus arbitration is used.

2. Do not assert BR during an IACK cycle, if the integration module SHEN bits are set to %11.

CPU16:065

CPU16: If the AVEC and DSACK signals are asserted simultaneously to terminate an IACK cycle, then the AVEC signal has higher priority. This is information only.

CPU16:065

HC16Z3:004

INTEGRATION: After power-up (Vdd Vdd min.) of the MCU, input/output and output-only port pins on the CPU16 module and the output only PWM pins (PWMA, PWMB) on the GPT module may be in an indeterminate state for up to 15 ms (depends on ramp up conditions). Input/output pins may be in output mode (instead of high impedance) for this time, which may create a conflict with external drive logic. Output only pins may not be in the defined reset state during this time. This is information only.

HC16Z3:004

WORKAROUND: If a known state is required on these pins, before the 15 ms port initialization period, external reset control logic must condition these lines.

IM:077

INTEGRATION: The loss of clock reference feature is not supported. Disregard bit position 4 in the SYNCR register (previously the SLIMP bit), this bit is now reserved. Insure that the bit position 2 in the SYNCR register is always written to it’s RESET state of %0 (previously the RSTEN bit). This is information only.

IM:077

IM:086

INTEGRATION: At power-up, integration module I/O pins should initialize to the high impedance state. The following pins may, however, drive as outputs until the first CLKOUT edge occurs to initialize the internal logic into the high impedance state. Port E, D[15:0] and HALT (open Drain). This is an erratum.

IM:086

WORKAROUND: If external conflicts result in system problems on these pins, isolate these pins from external devices using a series resistor or buffer on the offending pin.

IM:092

Integration: Unusual system operation may occur when bus arbitration is used in combination with additional system configuration settings and timing. As an example of the behavior, chip selects may assert while the external bus is granted away (if they are programmed to respond to the interrupt stack addresses) and interrupt stack may get corrupted. Reset is the only way to recover once this occurs.

Conditions to initiate:

1. SHEN bits of MCR set to %00 or %10.

and

2. BR is asserted coincident with the AS of an IACK cycle. (BR assertion is within the range of before and after 1 clock relative to the falling edge of CLKOUT when AS asserts.)

and

3. IACK cycle is terminated with external AVEC.

This is an erratum.

IM:092

WORKAROUND:

1. Use SHEN=%11 to prevent the IMB from running cycles while the external bus is granted away.

or

2. Do not assert BR coincident with AS of an IACK.

or

3. Do not use external AVEC. Use a chip select to assert internal AVEC for external nterrupts.

IM:095

INTEGRATION: Under certain conditions a masked interrupt may occur with an incorrect level. The conditions are: an external unmasked interrupt must occur coincident with an internal masked periodic interrupt (PIT). Also, previous to the above interrupts, an external interrupt line at the same level as the masked PIT interrupt must have been asserted and remain asserted. Example sequence to cause problem:

1. Set CPU interrupt mask to 5;
2. Set PIT to level 2;
3. Hold IRQ2 line low.
4. Assert valid IRQ interrupts (asserting IRQ 6 or IRQ7) the PIT exception is taken if pending.

This is an erratum.

IM:095

WORKAROUND: Do not allow matching levels on PIT and external pin.

IM:097

INTEGRATION: Several conditions combined may introduce apparent Periodic Interrupt Timer (PIT) clock errors. The clock error occurs if LPSTOP mode is entered and exited periodically using the PIT, and the system clock is set to minimum (131 KHz) prior to entry of LPSTOP mode and set to maximum at LPSTOP exit (PLL must re-lock). Also, on exiting from LPSTOP, the CPU will be held off of the bus until the PLL is re-locked. Variations in the PIT clock period may appear as the PIT counter missing clocks (the PIT is clocked by the EXTAL reference clock in LPSTOP, if STSIM = 0). During normal operation (not in LPSTOP) the PIT counter clock source (EXTAL) is synchronized by logic to the system clock (CLKOUT). The combination of PLL re-lock time, low frequency (131 KHz) clock source (too near 32 KHz reference), and the synchronization result in this behavior. This is information only.

IM:097

WORKAROUND: Use a minimum PLL frequency of 8 times the reference frequency (262 KHz for a 32 KHz reference) or higher if the system clock is toggled from a low frequency prior to LPSTOP entry (if STSIM = 0) and back to maximum on exit of LPSTOP periodically using the PIT as the controlling source. The problem is only seen when switching the PLL clock to a frequency that is too close to the reference (EXTAL) clock frequency.

IM:139

INTEGRATION: The RESET assertion time specification (#77) is 4 clocks (tcyc) minimum. However, the current version of this module requires RESET to be asserted until the current bus cycle in progress completes. This is an erratum

IM:139

WORKAROUND :

Assert the RESET pin for 2 clock cycles longer than the present timeout period of the bus monitor (BMT field in SYPCR register). This will result in an internal reset, independent of other system conditions (Bus Monitor does not need to be enabled).

IM:176

INTEGRATION: The CPU16 IPIPE0/IPIPE1 signals may appear corrupted whenever an access to on chip modules occurs during show cycles. This only occurs if module accesses are more than 2 clock. There are modules that can have access times of more than 2 clocks under normal operation. For example, some modules have a fixed access time of 3 clocks. In other modules a contention may occur when both the module control logic and the CPU attempt to access a common resource, typically resulting in wait states for the CPU. Please refer to the specific module reference manuals for this device for details. This is information only.

IM:176

WORKAROUND: Special external decode logic is required for the CPU16 IPIPE0/IPIPE1 signals in case this should occur.

VCO:051

INTEGRATION: In some Phase Lock Loop (PLL) documentation a three component filter from XFC to VDDSYNis recommended (18K resistor in series with 0.01 uF capacitor between VDDSYN and XFC, the series combination in parallel with a 3300 pF capacitor for a loop multiplier of N = 512). It has been determined with this three component filter, in the presence of external leakage (in excess of that provided by ~50 M Ohm) on the XFC pin, may result in the MCU not exiting RESET at power up. During this condition, the output frequency on CLKOUT is at the target value, but the PLL lock detect logic does not detect lock and continues to cause RESET assert ion. Versions of the integration module that are configured for either a slow or fast (Typ. 32.768 kHz or 4.194 MHz) crystal source use the same filter component values, since the internal reference frequency is always slow (32.768 kHz). Also, leakage from the XFC pin must not be in excess of thst provided by a 15 M Ohm resistor to meet PLL jitter specifications (with 0.1 uF XFC filter, refer to Electrical Characteristics section of Users manual). If the PLL is not enabled (MODCK=0 at RESET) then the XFC filter is not required and the pin may be left unconnected but VDDSYN must be connected to VDD (This item was previously IM:179). This is information only.

VCO:051

WORKAROUND: Do not use the three component filter on XFC. Use the originally documented filter (single 0.1 uF capacitor from the XFC pin to the VDDSYN supply pin).

VCO:059

INTEGRATION: The PLL Lock time (tlpll) specification of 20 ms at warm startup (VDD power up with VDDSYN applied) may not be met under some conditions. The internal PLL lock detection logic holds off assertion of the SLOCK bit in the SYNCR register during the PLL re-lock time and may result in a time longer than the specification in increments of 10 msec (20, 30 or 40 msec). (This was previously IM:098). This is an erratum.

VCO:059

WORKAROUND: Allow additional lock time (50 ms total lock time) under warm startup conditions.

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