56F8013

Preliminary Chip Errata

56F8013 Digital Signal Controller

Errata numbers are in the form n.m, where n is the number of the errata item and m identifies the document revision number.

Note: **Differences between Chip Revisions are listed on page 5** and errata information for chip revisions prior to revision A1 have been archived and can be requested from Freescale Sales.

Chip Errata Information:

The following errata items apply to 56F8013 devices with revisions and/or date codes as specified in the "Affected Chips" column. The date codes are located on the bottom line of the marking.

Errata Number	Affected Chips	Description	Impact and Workaround
1.0	Revision A1 (date code 0535 or greater)	Software breakpoint in uninterruptable code can cause the debugger to execute instructions in the wrong order.	Impact: If a sequence of code includes a conditional branch (i.e. Bcc) followed by two single word instructions and a breakpoint is set on the first single word instruction, the incorrect code execution will occur when the conditional branch is not taken Workaround: CodeWarrior has implemented a workaround that inserts a NOP after all conditional branches. The breakpoint will be located in the second single word instruction after the NOP, so execution will be correct. This workaround can be enabled or disabled by the user. Disabling the workaround will generate smaller code.
2.0	Revision A1 (date code 0535 or greater)	I^2C fails to meet data hold spec under various frequency/divider configurations	Impact: Same as description Workaround: User must use only supported configurations per spec. Table 4-5 of the 56F8000 Peripheral Reference Manual has been updated to include a list of supported configurations which do satisfy hold requirements. No hardware changes are planned.

Chip Errata Information: (Continued)

The following errata items apply to 56F8013 devices with revisions and/or date codes as specified in the “Affected Chips” column. The date codes are located on the bottom line of the marking.

Errata Number	Affected Chips	Description	Impact and Workaround
3.0	Revision A1 (date code 0535 or greater)	With the Quad Timer, when using Count Mode (CM) 0b110 “edge of secondary source triggers primary count till compare” and the Output Mode (OM) is 0b111 “enable gated clock output while counter is active”, the OFLAG will incorrectly output clock pulses prior to the secondary input edge if the primary count source is not an IPBus clock/N.	Impact: Typically this will arise when an application is trying to output a finite number of 50% duty cycle clock pulses triggered by the output of another timer. Timer 1 creates an infinite pulse train which is fed into the primary input of Timer 2. Timer 2's secondary input is the triggering signal. Timer 2's job is to wait until the trigger and then count out the correct number of clock pulses. Workaround: The workaround is to rearrange functionality. Timer 1 uses an IPBus/N to generate a pulse train at 2x the desired clock rate. It uses CM = 0b110 and OM = 0b111 correctly. Then Timer 2's job is to simply convert the 2x pulse stream into a clock pulse stream at 1x frequency and 50% duty cycle. It does this by CM = 0b001 (count rising edges of primary input) and OM = 0b011 (toggle OFLAG on successful compare) with a compare value of zero.
4.0	Revision A1 (date code 0535 or greater)	GPIO interrupts on the SAME port will not be detected if the edge of an input interrupt signal occurs in the same clock cycle that the IESR is written.	Impact: Hardware designs that have asynchronous interruptable inputs on the same GPIO port cannot rely on the device to generate the interrupt. Workarounds: 1. Use different ports for these two interrupts, or 2. After writing to the IESR, read the RAW_DATA register to determine if any other input transitions have occurred at this exact instant.
5.0	Revision A1 (date code 0535 or greater)	The “calculate data signature” command in the Flash Module cannot be run on protected flash memory Attempts to do so will produce a protection violation.	Impact: The calculate data signature command will not run on protected memory. Workaround: You must clear the protection bit for the section containing the start address of the calculate data signature command.
6.1	Revision A1 (date code 0535 or greater)	Documentation on recommended setting CHPMPTRI if a loss of reference clock occurs in the PLL. Setting CHPMPTRI, however, can cause the VCO frequency to increase out of spec.	Impact: Same as description Work Around: Function of this bit was misdocumented. The desired function was to permit safe continued use of the PLL output (though at a reduced frequency) if the reference clock stops working. This desired behavior in fact happens if CHPMPTRI is left in its default off setting.

Chip Errata Information: (Continued)

The following errata items apply to 56F8013 devices with revisions and/or date codes as specified in the "Affected Chips" column. The date codes are located on the bottom line of the marking.

Errata Number	Affected Chips	Description	Impact and Workaround
7.1	Revision A1 (date code 0535 or greater)	Step counter, ISC field in EOnCE Control Register (OCR), does not work correctly in several modes	Impact: Same as description Workaround: Users requiring functionality associated with this field should contact the factory for further information before using the field.
8.1	Revision A1 (date code 0535 or greater)	EN bit in the EOnCE Breakpoint Control Register (OCBR) register is not writeable.	Impact: Same as description Workaround(s): Users requiring functionality associated with this field should contact the factory for further information before using the field.
9.1	Revision A1 (date code 0535 or greater)	ASB mode does not automatically powerdown a converter when none of its inputs are referenced for use by a scan.	Impact: Same as description Workaround: User must use only supported configurations per spec. See ADC chapter in the 56F8000 Peripheral Reference Manual for clarification in Section 2.4.6.1, Manual Power Down of Unused Converters. No hardware changes are planned.
10.1	Revision A1 (date code 0535 or greater)	The Serial Bootloader application consistently aborts the download process when attempting to read in a valid S-record file.	Impact: 56F8013 devices with the data code of 0534 or earlier, are programmed with Serial Bootloader versions prior to 1.3 and do not correctly implement software flow control (Xon/Xoff). Workarounds: 1.Configure your PC serial application to include a delay of at least 2ms between each line of data transmitted. Also, be sure the serial application is sending "\r" (carriage return character) followed by "\n" (line feed character) to terminate each line of data. 2.Use components with date codes of 0535 or after, which are programmed with Serial Bootloader version 1.3 or greater. Versions 1.3 and beyond correctly implement Xon/Xoff flow control, so line delays are not needed. Note: The "\n" character is not needed for line endings with versions 1.3 and greater.

Chip Errata Information: (Continued)

The following errata items apply to 56F8013 devices with revisions and/or date codes as specified in the "Affected Chips" column. The date codes are located on the bottom line of the marking.

Errata Number	Affected Chips	Description	Impact and Workaround
11.1	Revision A1 (date code 0535 or greater)	The Serial Bootloader application freezes while downloading an S-record file.	Impact: 56F8013 devices with Serial Bootloader versions 1.3 or earlier do not support an odd number of bytes in the data field for S3 records. Workarounds: 1.A PERL script is available in FAQ# 25759 that can modify S-record files to ensure an even number of data field bytes are used for each S3 record. Use this script prior to S-record download. OR 2.Use 56F801x Serial Bootloader version 1.5 which is available for download on the Freescale website. Versions 1.5 and beyond are capable of processing S3 records containing an odd number of data field bytes. Note: Download, from the Freescale website (http://www.freescale.com), 1. PERL script - search for FAQ# 25759 2. the latest Serial Bootloader version for this device: Freecale.com/ Products / Digital Signal Processors and Controllers / 56800/E / 56F8013 / Design Tools /Software / Application Software/ Bootloader code, file "56F801XBOOTLOADER".
12.2	Revision A2 (date code 0704 or greater)	The ADC may drop conversions if powered down for extended periods of time.	Impact: If the ADC is powered down for an extended amount of time (e.g., days) and then powered back up, the ADC result may randomly drop to 0 or jump to 4095 (2^{12}-1). Periodic powering down does not cause this problem. However, extended periods in a continuous powered-down state may result in invalid conversions. Also, shutting the power off to the entire device for an extended amount of time does not cause this problem. The issue has only been observed when the device is powered up while the ADC is powered down (in software). Workaround: If the device is to operate and the application requires the use of the ADC, keep the ADC powered up during normal operation. Do not power down the ADC, even if it is not in use at that time. Powering the ADC up or down is controlled by the APD, PD0, and PD1 bits in the ADC's POWER register.
13.3	Revision A2 (date code 0704 or greater)	The ADC may not maintain accuracy of conversions if operated for extended periods of time, and at certain voltages below nominal voltage.	Impact: Same as description. Workaround: Maintain the VDDA and VREF inputs at a minimum of 3.1 V.

Chip Errata Information: (Continued)

The following errata items apply to 56F8013 devices with revisions and/or date codes as specified in the "Affected Chips" column. The date codes are located on the bottom line of the marking.

Errata Number	Affected Chips	Description	Impact and Workaround
14.3	Revision A2 (date code 0704 or greater)	The flash security backdoor key is not recognized.	Impact: The backdoor key cannot be used to unlock the flash at runtime. Workaround: None available.

Differences between Chip Revisions

Errata Title	Chip Rev. A1 *Date Code ≥ 0535*	Chip Rev. A2 *Date Code ≥ 0704*
Software breakpoint in uninterruptable code can cause the debugger to execute instructions in the wrong order. *See errata item 1 for clarification.*	Same as A	Same as A
I^2C fails to meet data hold spec under various frequency/divider configurations. *See errata item 2 for clarification.*	Same as A	Same as A
When assigning new timer compare values, the current output level can be cut short or inappropriately extended.	**Corrected**	**Corrected**
With the Quad Timer, when using Count Mode (CM) 0b110 "edge of secondary source triggers primary count till compare" and the Output Mode (OM) is 0b111 "enable gated clock output while counter is active", the OFLAG will incorrectly output clock pulses prior to the secondary input edge if the primary count source is not an IPBus clock/N. *See errata item 3 for clarification.*	Same as A	Same as A
When the ADC starts, its clock is resynchronized to align with the system clock. This resync event can corrupt the first ADC's sample.	**Corrected**	**Corrected**
When using APD, program the PUDELAY field to 18 before starting the ADC.	**Corrected**	**Corrected**
GPIO interrupts on the SAME port will not be detected if the edge of an input interrupt signal occurs in the same clock cycle that the IESR is written. *See errata item 4 for clarification.*	Same as A	Same as A
The "calculate data signature" command in the Flash Module cannot be run on protected flash memory Attempts to do so will produce a protection violation. *See errata item 5 for clarification.*	Same as A	Same as A
Documentation recommended setting CHPMPTRI if a loss of reference clock occurs in the PLL. Setting CHPMPTRI, however, can cause the VCO frequency to increase out of spec. *See errata item 6 for clarification.*	Same as A	Same as A
Step counter (ISC field in OCR) does not work correctly in several modes. *See errata item 7 for clarification.*	Same as A	Same as A

Differences between Chip Revisions (Continued)

Errata Title	Chip Rev. A1 *Date Code ≥ 0535*	Chip Rev. A2 *Date Code ≥ 0704*
EN bit in OCBR register is not writeable. *See errata item 8 for clarification.*	Same as A	Same as A
ASB mode does not automatically powerdown a converter when none of its inputs are referenced for use by a scan. *See errata item 9 for clarification.*	Same as A	Same as A
The Serial Bootloader application consistently aborts the download process when attempting to read in a valid S-record file. *See errata item 10 for clarification.*	**Corrected** in rev A1, use components with date codes of 0535 or after which are programmed with Serial Bootloader version 1.3 or greater.	**Corrected**
The Serial Bootloader application freezes while downloading an S-record file. *See errata item 11 for clarification.*	Download fix from Freescale Web site	Download fix from Freescale Web site
The ADC may drop conversions if powered down for extended periods of time. *See errata item 12 for clarification.*	—	Same as A1
The ADC may not maintain accuracy of conversions if operated for extended periods of time, and at certain voltages below nominal voltage. *See errata item 13 for clarification.*	—	Same as A1
The flash security backdoor key is not recognized. *See errata item 14 for clarification.*	—	Same as A1

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