Freescale Semiconductor
Engineering Bulletin

Document Number: EB736
Rev. 0, 9/2010

Limitations of the PDI Module on the MPC560xS

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1 Introduction

The MPC560xS device has the ability to interface with an external video source using its Parallel Data Interface (PDI) module, this stream can then be fed directly to the Display Control Unit (DCU) for display on a TFT LCD display.

The PDI module has certain restrictions on the incoming stream format and errata PS8790 that affects streams in internal sync mode. This engineering bulletin shows how to interface a video source to the PDI module on the MPC560xS. It should be used in conjunction with the DCU and PDI sections of the reference manual titled *MPC5606S Reference Manual* (document MPC5606SRM) .

The MPC5645S contains two PDI modules that are similar to the MPC560xS, however it also includes a Video Interface Unit (VIU) that has an additional function included, de-interlacing and scaling. It also has full support for ITU656 timing, therefore it is anticipated that the VIU will be the preferred module for interfacing with an external video source on the MPC5645S.

2 Overview of PDI Module

The PDI module accepts a video stream complete with data and timing from an external source. It sends the stream directly to the DCU module where it replaces the background layer. The PDI does not process the incoming stream in any way, nor does it store it to the memory for any processing to take place in the software. Therefore, to “ lock ” the PDI onto the video stream,

all timing information must exactly match the chosen TFT panel. The PDI contains a state machine that monitors the external stream and locks only under the correct conditions.

- The resolution of the stream must be the same as the TFT panel.
- The stream must be de-interlaced. Interlaced streams are not supported. It is not possible to ignore every odd frame.
- The HSYNC and VSYNC blanking signals must be the same length as those defined in the DCU. The DCU values are defined in the HSYN_PARA and VSYN_PARA registers. The front and back porch values must also match (see Figure 1). Any variation—even by just a single clock—prevents a lock.
- The pixel clock frequency does not have to match the TFT to achieve lock. Although, this becomes the timing signal that drives the TFT it must be within the spec of the TFT.
- The PDI allows for the polarity of the incoming timing signals to be altered. The active level of the HSYNC, VSYNC, and DE signals can be selected just as the pixel clock edge upon which the data is sampled.

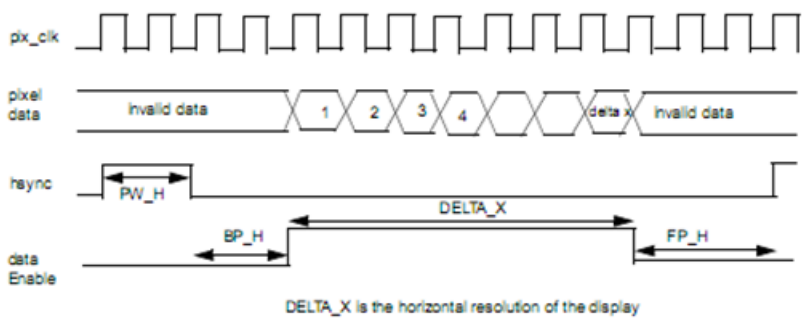

Figure 1. Horizontal timing—back porch (BP_H), front porch (FP_H), and pulse width (PW_H)

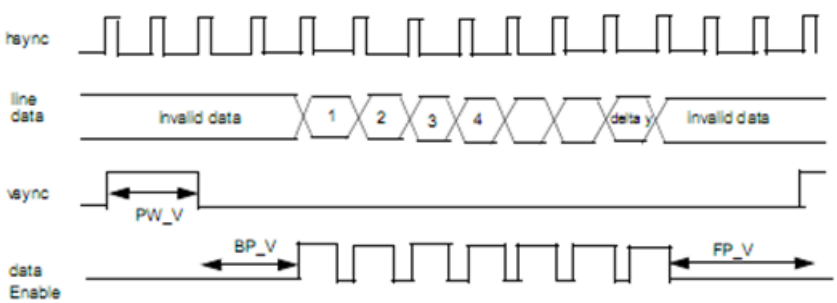

Figure 2. Vertical timing—back porch (BP_V), front porch (FP_V) and pulse width (PW_V)

After “lock” has been achieved, the timing signals sent to the DCU match the incoming stream, that is, if the pixel clock of the incoming stream differs from the output by the DCU, then upon lock the DCU uses the frequency of the PCLK from the video source.

The PDI can be configured to select one of two different synchronisation methods:

- External sync—This is similar to the way the DCU drives a TFT. There are numerous data pins. The exact number is based on the colour encryption method being used, for example, 8-bit mono, RGB565, or RGB666. Each of the timing signals has its own pin: HSYNC, VSYNC, PCLK, and DataEnable. The data enable signal is optional, the PDI can be configured to ignore it (in which case it does not have to be included in the incoming stream).
- Internal Sync—As a means of reducing the pin count in the video to PDI interface, the timing signals are encoded with the data. The way timing signals are encoded is defined by the ITU656 recommendation.

NOTE

Due to an errata, the PDI does not fully follow the ITU656 recommendation and an incoming ITU656 stream requires alterations if it is used. See Errata PS8790 for full details.

3 PDI Interfacing Methods

There are two common methods for generating a video stream for the PDI.

3.1 Analog Source

Figure 3. Connecting an analog source

In this case a low cost camera with an analog output is used as a source. These typically offer PAL and NTSC standard outputs. Some cameras may also offer the option of outputting in a progressive scan mode, this means that the stream does not require to be de-interlaced at a later stage. To interface these with the PDI, the signal has to be converted to a digital format and processed to match the resolution and timing requirements of the TFT panel used. This can be done by a decoder or FPGA.

A decoder or FPGA has to be carefully selected and programmed to carry out the following tasks:

- De-interlace the incoming stream
- Scale the stream to match the TFT panel resolution
- Ensure the timing exactly matches the TFT panel. All aspects of the blanking period (length as well as front and back porch) must match.

The digital output of the decoder and FPGA can then be fed to the PDI module.

The decision of whether to use a decoder or an FPGA depends on the availability of a decoder that supports the required features at the resolution of the TFT being used. If such a device is not available then an FPGA must be used.

3.2 Digital Source

Figure 4. Connecting a digital source

Several manufacturers produce cameras with integrated decoders. Depending on the flexibility these offer, they could be used to output the required signal without any additional hardware. As per the decoder/FPGA in the analog case, the integrated decoder must support progressive scan mode, must allow for the selection of a resolution matching that of the TFT, and must have flexibility in configuring the blanking period.

Care must be taken to ensure when downscaling the resolution the decoder re-encodes the entire stream. Certain decoders keep the same frame length and pixel clock for both VGA and QVGA streams, but do not output anything on the data pins for every second pixel. The PDI is not able to lock onto this stream.

If the integrated decoder cannot output the required stream at the required resolution then an additional FPGA may be required to carry out further processing on the stream to ensure compatibility with the PDI.

4 Errata PS8790

The PDI contains an errata pertaining to the use of the internal synchronization mode. The PDI does not lock onto a correct ITU656 stream even if the timing matches. The easiest workaround for this issue is to use external synchronization, but if this is not possible (perhaps due to the need to minimize the pins used by the PDI), then it is possible to use an external FPGA to alter the internal sync stream to a form that the PDI accepts. The FPGA can also carry out scaling and de-interlacing of the incoming stream, allowing otherwise incompatible cameras to be used as a source for the PDI.

This section assumes the reader is familiar with the timing aspects of the ITU-R BT.656 Recommendation http://www.itu.int/rec/R-REC-BT.656/en.

NOTE

The PDI uses only the timing aspects of the recommendation. The resolution and interlacing aspects are not required.

In the ITU656 recommendation, it states that:

" F and V fields are only allowed to change as part of EAV sequences i.e transition from H=0 to H=1. "

The F field is not supported by the PDI and is ignored, it is therefore of no importance. The internal sync stream is built as follows:

Full frame:

FULL_FRAME = FULL_LINE * y_res // V_BLANK_LINE * V_blanking
y_res is the Y-resolution of the TFT and V_blanking is the vertical blanking period.

Where:

FULL_LINE = EAV(H=1, V=0) // H_blanking // SAV(H=0, V=0) // Active_Data
V_BLANK_LINE = EAV(H=1, V=1) // H_blanking // SAV(H=0, V=1) // V_blanking

The unencoded VSYNC and HSYNC timing signals defined by the recommendation are shown in Figure 5:

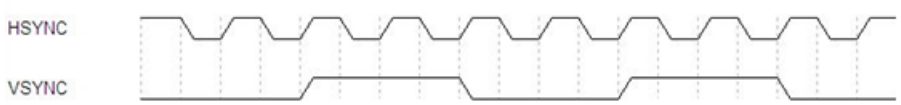

Figure 5. Unencoded HSYNC and VSYNC signals as per ITU656 Recommendation

Notice that the VSYNC signal only changes on the rising edge of the HSYNC signal. Due to errata PS8790, the PDI does not lock onto this signal.

The PDI does however lock onto the following stream:

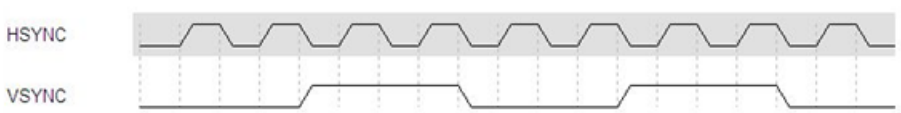

Figure 6. Unencoded HSYNC and VSYNC signals for successful PDI lock

Notice that in this instance the VSYNC signals only change on falling HYSNC edges.

The stream in Figure 6 is created as follows:

Full frame:

FULL_FRAME = FULL_LINE * y_res // V_BLANK_LINE * V_blanking
y_res is the Y-resolution of the TFT and V_blanking is the vertical blanking period.

Where:

FULL_LINE = SAV(H=0, V=0) // Active_Data // EAV(H=1, V=0) // H_blanking
V_BLANK_LINE = SAV(H=0, V=1) // V_blanking // EAV(H=1, V=1) //H_blanking
By using an FPGA any incoming signal (even NTSC/PAL) can be encoded into an internal sync stream that is compatible with the PDI.

5 Initialize PDI

After a compatible stream has been identified, the PDI is straight forward to configure. The key configuration steps for an external sync stream are shown below. It is assumed that the DCU has already been configured correctly.

1. Setup the pins the PDI will use in the SIU module
2. Configure the DCUMODE register to identify the format of the incoming stream:
   - PDI_SYNC_LOCK selects the number of full error-free frames to receive before the PDI sets the lock bit
   - If a Data Enable input is used, then set the PDI_NARROW_MODE bit
   - Use PDI_MODE to select the color encryption method (for example, RGB565)
   - Set PDI_SYNC to 0 to select external synchronization mode (timing signals are supplied on their relevant pins)
3. Configure the polarity of the incoming stream using the SYN_POL register. This allows the active edge of all the timing signals to be defined.
4. Enable the PDI by setting the PDI_EN in DCUMODE register.

Prior to the lock bit being set, the background of the display is set to the colour configured in the BGND register. After the number of error-free frames defined in PDI_SYNC_LOCK has been received, the lock bit is set and the background is replaced by the incoming video stream.

If lock is not achieved, the PDI_STATUS register can be consulted to help debug the issue. This shows which timing signals have been detected. The blanking flag shows if the H/VSYNC values of the stream match those in the H/VSYN_PARA registers.

6 Conclusion

- The incoming stream must be the correct resolution and the timing must exactly match the DCU values.
- A decoder can be used only if it supports the resolution of the TFT being used, otherwise an FPGA is required.
- The Decoder cannot be used for Internal Sync mode. The FPGA is required for this.

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Document Number: EB736
Rev. 0, 9/2010