Freescale Semiconductor
Engineering Bulletin

EB701
Rev. 1.0, 1/2009

MC33937 Double RESET Timing Considerations

Introduction

The 33937 high side pre-driver latches may begin in an indeterminate state, which draws more current than normal (about 5.0 mA more per phase), when first powered up. This state will also result in a reduced charge on the bootstrap capacitor and elevated initial voltage on the high side source. Note that even in the indeterminate state, the 33937 will not turn ON the high side output MOSFET until after the initialization sequence.

The double reset strategy for the 33937 is intended to insure that the high side pre-driver latches begin in a defined, low current state. As a result, the pre-initialization charge on the bootstrap capacitor will be full and the high side source will be near 0 V.

The timing requirements will be treated in three stages:

1. The length of time required between the first RESET going high and the second RESET going low.
2. How long the second RESET needs to stay low.
3. The wait time after the second RESET goes high before initialization.

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How long does the first RESET remain high?

The first RESET must remain high long enough for VDD and VLS to reach the full regulated voltage. The normal time for this to occur is specified as 2.0 ms maximum. If there is more capacitance on VLS or VDD than the nominal values given in the specification, this time may need to be increased. In general, the time may be safely scaled linearly with the capacitance. If the charge pump is used, it may also increase this time. An estimate of increased time due to charge pump would be to add 25%. For example, the nominal VLS capacitance is 2.2 μF on both VLS and VLS_CAP. If that value is doubled to 4.4 μF on each pin, the power up time should be increased to 4.0 ms; 5.0 ms if using the charge pump.

How long does the second RESET remain low?

The second RESET must remain low long enough for VDD to decay below the POR threshold as a minimum. The POR threshold is specified as 4.5 V max and 3.4 V min. (MC33937 data sheet. Look for V_{THRST} in the Static Electrical Characteristics table). The load on VDD may be treated as a resistive load of 570 Ω ±25% on 5.0 V (variations in VDD have already been taken into consideration in the equivalent resistance calculation). Minimum time to guarantee reaching POR is:

$$t_{POR} = 570\Omega \bullet (1.25) \bullet C_{VDD} \bullet \ln(5/3.4)$$
$$= 275\Omega \bullet C_{VDD}$$

So if the capacitance used on VDD is 1.0 μF ±20%, the minimum time for t_{POR} would be

$$t_{POR} = 275\Omega \bullet 1.0\mu F \bullet 1.2$$
$$= 330\mu s$$

The second RESET must not last so long that VLS decays below the threshold to operate the high side pre-driver latches. Since under the worst case conditions the high side latches act like a 3.0 V clamp with a 270 ohm series resistance, VLS needs to be greater than 3.0 V plus three diode drops, or approximately 5.1 V ±0.6 V. If VLS decays below this voltage, there will no longer be sufficient bias to prevent bleeding critical charge from the bootstrap capacitor. Analysis of the current paths and measurements of current-voltage characteristics shows that the high side latch behaves like a 3.0 V clamp with a 270 ohm series resistance. The path to ground from HS_S is 40 kohm ±20%, in parallel with 1750 ohm in series with two diodes, until VDD reaches 1.0 V ±30%, at which time it becomes 40 kohm in parallel with 100 μA maximum in series with a diode.

VLS will not begin to decay until after POR has occurred.

The time for VDD to decay to 0.7 V is given by:

$$t_{HOLD} = 570\Omega \bullet (1.25) \bullet C_{VDD} \bullet \ln(5/0.7)$$
$$= 1401\Omega \bullet C_{VDD}$$

Using our 1.0 μF example:

$$t_{HOLD} = 1401\Omega \bullet 1.0\mu F \bullet 1.2$$
$$= 1.68ms$$

The voltage on VLS at t_{HOLD} is given by:

$$VLS(t_{HOLD}) = (VLS - V_{OS}) \bullet \exp(-t_{HOLD}/(C_{VLS} \bullet (R_{LATCH} + R_{PD})/3)) + V_{OS}$$

Where:

$$V_{OS} = 3V \bullet (1.20) + 3 \bullet 0.7V$$
$$= 5.7V$$
$$R_{LATCH} = 270\Omega \bullet (0.80)$$
$$R_{PD} = 1750\Omega \bullet (0.80)$$
$$(R_{LATCH} + R_{PD})/3 = (270\Omega + 1750\Omega) \bullet 0.8/3$$
$$= 538.7\Omega$$
$$VLS(t_{HOLD}) = (VLS - 5.7V) \bullet \exp(-t_{HOLD}/(C_{VLS} \bullet 538.7\Omega)) + 5.7V$$

If VLS is assumed to be 13 V (a low charge pump voltage at low battery condition) and using 2.2 μF ±20% on each VLS and VLS_CAP (total of 4.4 μF), the VLS voltage at our example t_{HOLD} is:

$$VLS(1.68ms) = (13V - 5.7V) \bullet \exp(-1.68ms)/(4.4\mu F \bullet (0.8 \bullet 538.7\Omega)) + 5.7V$$
$$= 8.71V$$

The rate of voltage change of VLS can be approximated for time after t_{HOLD}, by assuming the average current discharging the VLS capacitors is the sum of all hold-off currents (max 100 μA per phase), plus $(VLS(t_{HOLD}) - (V_{CLAMP} + V_{DIODE}))/ R_{PULL\text{-}DOWN} / 2$ per phase. This approximation is good down to the clamp voltage of the high side latch, which is the minimum voltage for recovering the second RESET.

$$I_{VLS} = 3 \bullet (100\mu A + (VLS(t_{HOLD}) - (V_{CLAMP} + V_{DIODE}))/R_{PD}/2)$$
$$= 300\mu A + 3 \bullet (VLS(t_{HOLD}) - (3 \bullet 1.2 + 0.7))/(40k\Omega \bullet 0.8)/2$$
$$= 3 \bullet VLS(t_{HOLD})/64k\Omega + 98\mu A$$

For the example:

$$I_{VLS} = 3 \bullet 8.71V / 64k\Omega + 98\mu A$$
$$= 506\mu A$$

The rate of voltage change is:

$$\delta VLS / \delta t = I_{VLS} / C_{VLS}$$

For the example:

$$\delta VLS / \delta t = 506\mu A / (4.4\mu F \bullet 0.8)$$
$$= 144V / s$$

The time for VLS to decay to the minimum acceptable value is:

$$\Delta t = (VLS(t_{HOLD}) - (V_{CLAMP} + V_{DIODE})) / ((\delta VLS) / \delta t)$$

For the example:

$$\Delta t = (8.71V - (3.0V \bullet 1.2 + 0.7V)) / 144V / s$$
$$= 30.6ms$$

The maximum time for the second RESET pulse to be low is:

$$t_{2ND} = t_{POR} + t_{HOLD} + \Delta t$$

For the example:

$$t_{2ND} = 0.33ms + 1.68ms + 30.6ms$$
$$= 32.6ms$$

How long after second RESET before device can be initialized?

As soon as VDD and VLS have recovered the device can continue the normal initialization sequence. This recovery time will be less than the initial power up time, so it is always safe to use that time as the settling time for the second RESET recovery.

Double RESET timing calculator

Here is a handy calculator to compute a good set of timing parameters for the double RESET. These calculations have been designed to yeild results that are valid over the full temperature range for the production version of the 33937. Modify the values highlighted in yellow in the DATA table. The RESULTS table will automatically calculate and update the recommended limits for the double reset.

Table 1. Data

Capacitance On			Tol	
VDD	0.47	µF	20.00%	
VLS	2.20	µF	20.00%	
VLS_CAP	2.20	µF	20.00%	
VLS	13.00	V		The stable VLS voltage, also VLS at the end of t_{START}.

Table 2. Calculations

V_{DHS}	5.70	V	3.0 V clamp + 20% + 3 * 0.7 V diode drops
$t_{3.4}$	0.000155	s	Maximum time for VDD to decay to 3.4 V (Latest POR, t_{START})
t_{HOLD}	0.000790	s	Maximum time for VDD to decay to 0.7 V (Latest transistion to constant current drain)
V_{LS2}	10.51	V	VLS when transistion to constant current drain
δVLS/δt	167.96	V/s	3*(100µA + Iave_phasecomp)/CVLS Rate of decay with maximum constant current drain.
Δt	0.036988	s	Time to decay from V_{LS2} to V_{DHS}.
t_{2ND_MAX}	37.93	ms	

Table 3. Results

	Min	Max	
t_{START}	2.00	-	ms
t_{2ND}	0.16	37.93	ms
t_{END}	2.00	-	ms

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Rev. 1.0, 1/2009

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