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MFR4310 and MFR4300 Differences

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1 Introduction

This document highlights differences between the MFR4310 and MFR4300 devices. Information about fixed bugs and issues reported for the MFR4300 is outside of the scope of this document. However, this document shows the MFR4310 differences in contrast to the MFR4300 including the following:

- New features implemented
- Features removed
- Changes introduced

See the MFR4310 Data Sheet and Product Brief, the MFR4300 Data Sheet and Product Brief, and MFR4300 Errata documents for more details.

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NOTE

The MFR4310 has the same pinout as the MFR4300 device. Therefore, the MFR4300 can be replaced by the MFR4310 without modifying the PCB application.

2 EBI and Interface Signals

2.1 Added New MPC EBI Mode

A new MPC EBI mode was added to interface with Freescale's MPC5xx/MPC55xx family of devices without glue-logic. In contrast to the AMI interface mode, WE is not used in the MPC EBI mode. Therefore, read/write transactions are performed by MFR4310 EBI based on BSEL0 and BSEL1 signals. Figure 1 depicts an example of the MPC interface with the MPC5xx and MPC55xx devices.

NOTE

The AMI and S12 EBI modes functionality and selections remained unchanged.

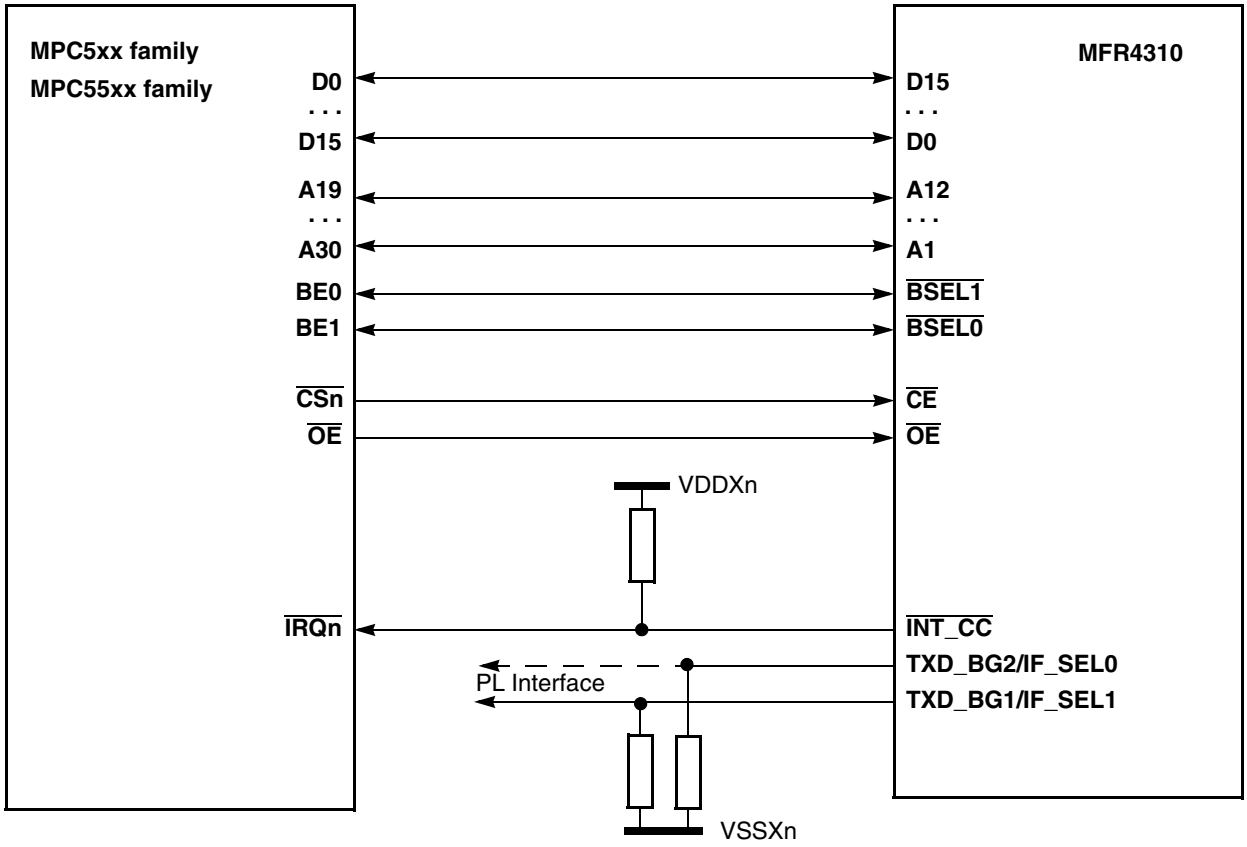

Figure 1. Example of MPC Interface with MPC5xx and MPC55xx Families

2.2 Changed IF_SEL = 00 Function and EBI Clock Source Indication

The interface selection is made on the levels of the IF_SEL[1:0] pins while a power-on, low voltage, clock monitor (if enabled), or external reset process is ongoing. The CRG latches the IF_SEL[1:0] during the latching window and sets the EBI mode according to Table 1.

Table 1. EBI Mode Selection

IF_SEL[0]	IF_SEL[1]	EBI Mode
0	0	MPC Interface
0	1	HCS12 Synchronous Interface
1	0	Asynchronous Memory Interface
1	1	Asynchronous Memory Interface

The CRG latches the EBI clock source according to Table 2 and indicates the latched state in the CRSR.ECS bit.

Table 2. EBI Clock Source Selection and Indication

IF_SEL[0]	IF_SEL[1]	EBI Clock Source	CRSR.ECS
0	0	CHICLK_CC	1
0	1	CLK_CC	0
1	0	CLK_CC	0
1	1	CHICLK_CC	1

NOTE

Only the rows marked in gray (IF_SEL[0] = 0 and IF_SEL[1] = 0) changed for the MFR4310 in contrast to the MFR4300 device. The rest of the rows remained unchanged.

After the evaluation, if both IF_SEL[1:0] signals are high or low, the CRG sets to the CRSR.ECS bit to one. Otherwise, the CRG clears that bit.

2.3 Changed IF_SEL[0] Internal Pulldown to Pullup

The IF_SEL[0] pin has an internal pullup during reset. Therefore, if there are no external pullup/down resistors connected to the IF_SEL[1:0] pins, the asynchronous memory interface with CLK_CC is selected for the EBI.

NOTE

In contrast to the MFR43100, the MFR4300 has pulldowns on the IF_SEL[1:0] pins during reset. Therefore, if there are no external pullup/down resistors connected to the MFR4300's IF_SEL[1:0] pins, no interface is selected for the EBI.

NOTE

For MFR4300 and MFR4310, the IF_SEL[1:0] pullups/downs are enabled only during reset. These pullups/downs are disabled after the reset operation is complete.

2.4 Added $\overline{\text{RESET}}$ Internal Pulldown

The $\overline{\text{RESET}}$ pin in the MFR4310 has a permanent internal pulldown. This is done to avoid device misbehavior in case the $\overline{\text{RESET}}$ pin loses connection to the board trace due to unforeseen reasons by ensuring the device remains in the reset state.

2.5 Added $\overline{\text{RESET}}$ Glitch Filter

MFR4310 has a built-in $\overline{\text{RESET}}$ glitch filter to avoid device reset caused by glitches on the $\overline{\text{RESET}}$ line. Table 3 depicts glitch filter characteristics.

Table 3. $\overline{\text{RESET}}$ Glitch Filter Characteristics

Parameter	Min	Max	Unit
$\overline{\text{RESET}}$ assertion time	14	—	ns
Filtered glitch duration	—	3	ns

Figure 2 illustrates an external reset sequence.

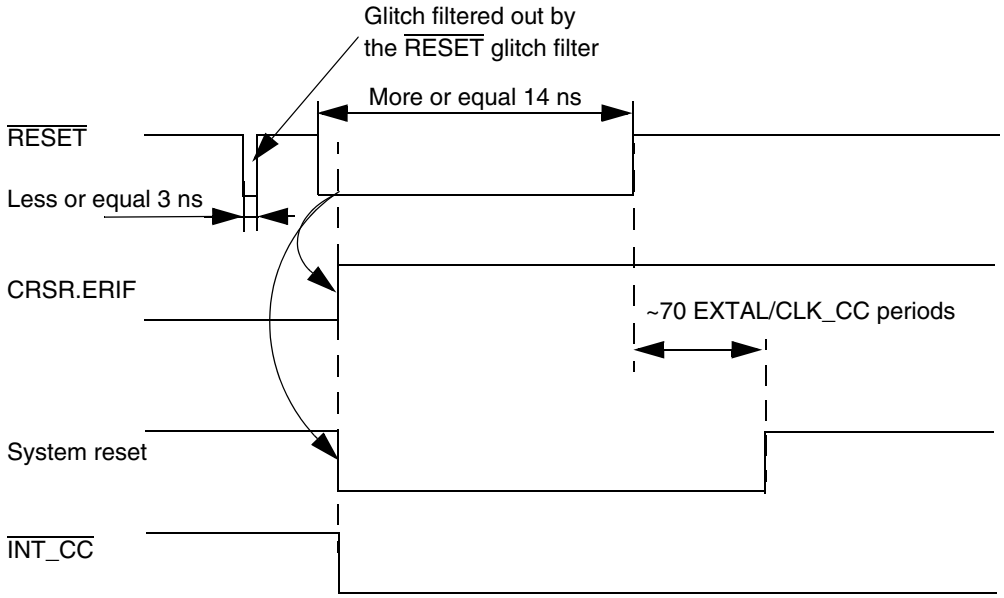

Figure 2. External Reset

2.6 Maximum CHICLK_CC frequency

Table 4 represents maximum CHICLK_CC frequency parameters for MFR4310 and MFR4300 devices.

Table 4. Maximum CHICLK_CC Frequency Parameters

Device	Maximum CHICLK_CC Frequency (MHz)
MFR4310	76
MFR4300	80

The reduction of the maximum CHICLK_CC frequency from 80 MHz (MFR4300) to 76 MHz (MFR4310) has the following consequences:

- Shortest possible maximum AMI read access time increased from 54 ns (MFR4300) to 56 ns (MFR4310)
- Minimum AMI read and write cycle times scale similarly (see EBI Timing Parameters sections in MFR4310 Product Brief and MFR4310 Data Sheet documents for minimum AMI read and write cycle times calculations)

The reduction of the maximum CHICLK_CC frequency from 80 MHz (MFR4300) to 76 MHz (MFR4310) has no impact on the following:

- EBI S12 mode timing
- Maximum number of message buffers supported with minimum minislot configuration
- FlexRay bus timing

3 PIM PIDR Register Change

The PIM part ID register (PIDR) provides the part ID 4310 in binary coded decimal.

Address offset = 0x0000; Address in MFR4300 = 0x00F0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	1	0	0	0	0	1	1	0	0	0	1	0	0	0	0
W																
Reset	0	1	0	0	0	0	1	1	0	0	0	1	0	0	0	0

Figure 3. Part ID Register (PIDR)

This register provides the part ID (4310) in binary coded decimal.

4 FlexRay IPI Block Changes

4.1 FlexRay Bus Lower Bit Rates Support

Besides the 10 Mbit/sec rate, support of lower FlexRay channel bit rates was added: 8, 5, 2.5 Mbit/sec.

4.2 FlexRay IPI Register Changes

4.2.1 Module Version Register (MVR)

Reason: module updated, therefore, the module version number changed.

MFR4300: 0x3535

MFR4310: 0x8566

0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CHIVER								PEVER							
W																
Reset	1	0	0	0	0	1	1	0	0	1	1	0	0	1	1	0

Figure 4. Module Version Register (MVR)

This register provides the FlexRay module version number. The module version number is derived from the CHI version number and the PE version number.

Table 5. MVR Field Descriptions

Field	Description
15–8 CHIVER	CHI Version Number. This field provides the version number of the controller host interface.
7–0 PEVER	PE Version Number. This field provides the version number of the protocol engine.

4.2.2 Module Configuration Register (MCR)

Reason: support of lower FlexRay channel bitrate added (8, 5, 2.5 Mbit/sec).

MFR4300: MCR[3:1] reserved

MFR4310: MCR[3:1] — BITRATE, controls FlexRay channel bit rate

0x0002

Write: MEN, SCM, CHB, CHA, BITRATE: Disabled Mode
SFFE: Disabled Mode or *POC:config*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MEN	0	SCM	CHB	CHA	SFFE	0	R*	0	0	0	R*	BITRATE			0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5. Module Configuration Register (MCR)

This register defines the global configuration of the FlexRay module.

Table 6. MCR Field Descriptions

Field	Description
15 MEN	Module Enable. This bit indicates whether the FlexRay module is in the disabled mode. The application requests the FlexRay module to leave the disabled mode by writing 1 to this bit. Before leaving the disabled mode, the application must configure the SCM, CHB, CHA, TMODE, and BITRATE values. 0 Write: Ignored, FlexRay module disable not possible Read: FlexRay module disabled 1 Write: Enable FlexRay module Read: FlexRay module enabled **Note:** If the FlexRay module is enabled, it can not be disabled.
13 SCM	Single Channel Device Mode. This control bit defines the channel device mode of the FlexRay module. 0 FlexRay module works in dual channel device mode 1 FlexRay module works in single channel device mode
12–11 CHB CHA	Channel Enable. Protocol related parameter: pChannels The semantic of these control bits depends on the channel device mode controlled by the SCM bit and is given Table 7.
10 SFFE	Synchronization Frame Filter Enable. This bit controls the filtering for received synchronization frames. 0 Synchronization frame filtering disabled 1 Synchronization frame filtering enabled
8 R*	Reserved. This bit is reserved. It is read as 0. Application must not write 1 to this bit.
4 R*	Reserved. This bit is reserved. It is read as 0. Application must not write 1 to this bit.
3–1 BITRATE	FlexRay Bus Bit Rate. This bit field defines the bit rate of the FlexRay channels according to Table 7.

Table 7. FlexRay Channel Selection

SCM	CHB	CHA	Description
Dual Channel Device Modes			
0	0	0	Ports RXD_BG1, TXD_BG1, and $\overline{\text{TXEN1}}$ not driven by FlexRay module. Ports RXD_BG2, TXD_BG2, and $\overline{\text{TXEN1}}$ not driven by FlexRay module. PE channel 0 idle PE channel 1 idle
	0	1	Ports RXD_BG1, TXD_BG1, and $\overline{\text{TXEN1}}$ driven by FlexRay module. Ports RXD_BG2, TXD_BG2, and $\overline{\text{TXEN1}}$ not driven by FlexRay module. PE channel 0 active PE channel 1 idle
	1	0	Ports RXD_BG1, TXD_BG1, and $\overline{\text{TXEN1}}$ not driven by FlexRay module. Ports RXD_BG2, TXD_BG2, and $\overline{\text{TXEN1}}$ driven by FlexRay module. PE channel 0 idle PE channel 1 active
	1	1	Ports RXD_BG1, TXD_BG1, and $\overline{\text{TXEN1}}$ driven by FlexRay module. Ports RXD_BG2, TXD_BG2, and $\overline{\text{TXEN1}}$ driven by FlexRay module. PE channel 0 active PE channel 1 active

Table 7. FlexRay Channel Selection (continued)

SCM	CHB	CHA	Description
Single Channel Device Mode			
1	0	0	Ports RXD_BG1, TXD_BG1, and $\overline{\text{TXEN1}}$ not driven by FlexRay module. Ports RXD_BG2, TXD_BG2, and $\overline{\text{TXEN1}}$ not driven by FlexRay module. PE channel 0 idle PE channel 1 idle
	0	1	Ports RXD_BG1, TXD_BG1, and $\overline{\text{TXEN1}}$ driven by FlexRay module. Ports RXD_BG2, TXD_BG2, and $\overline{\text{TXEN1}}$ not driven by FlexRay module. PE channel 0 active PE channel 1 idle
	1	0	Ports RXD_BG1, TXD_BG1, and $\overline{\text{TXEN1}}$ driven by FlexRay module. Ports RXD_BG2, TXD_BG2, and $\overline{\text{TXEN1}}$ not driven by FlexRay module. PE channel 0 active, uses cCrcInit[B] PE channel 1 idle
	1	1	Reserved

Table 8. FlexRay Channel Bit Rate Selection

MCR[BITRATE]	FlexRay Channel Bit Rate [Mbit/s]
000	10.0
001	5.0
010	2.5
011	8.0
100	Reserved
101	Reserved
110	Reserved
111	Reserved

4.2.3 Protocol Operation Control Register (POCR)

Reason: customer requirement.

MFR4300: EOC_AP / ERC_AP write only, read returns 0

MFR4310: EOC_AP / ERC_AP read/write, read returns written value

0x0014 Write: Normal Mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	EOC_AP		ERC_AP		BSY	0	0	0	POCCMD			
W	WME								WMC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6. Protocol Operation Control Register (POCR)

The application uses this register to issue protocol control commands and external clock correction commands. External clock correction commands are issued by writing to the EOC_AP and ERC_AP fields. Protocol control commands are issued by writing to the POCCMD field. For more information on protocol control commands and external clock correction commands, see the the MFR4310 Data Sheet.

Table 9. POCR Field Descriptions

Field	Description
15 WME	Write Mode External Correction. This bit controls the write mode of the EOC_AP and ERC_AP fields. 0 Write to EOC_AP and ERC_AP fields on register write 1 No write to EOC_AP and ERC_AP fields on register write
11–10 EOC_AP	External Offset Correction Application. This field is used to trigger the application of the external offset correction value defined in the protocol configuration register (PCR29). 00 Do not apply external offset correction value 01 Reserved 10 Subtract external offset correction value 11 Add external offset correction value
9–8 ERC_AP	External Rate Correction Application. This field is used to trigger application of the external rate correction value defined in the protocol configuration register (PCR21). 00 Do not apply external rate correction value 01 Reserved 10 Subtract external rate correction value 11 Add external rate correction value
7 BSY WMC	Protocol Control Command Write Busy. This status bit indicates the acceptance of the protocol control command issued by the application via the POCCMD field. The FlexRay module sets this status bit when the application has issued a protocol control command via the POCCMD field. The FlexRay module clears this status bit when protocol control command was accepted by the PE. When the application issues a protocol control command while the BSY bit is asserted, the FlexRay module ignores this command, sets the protocol command ignored error flag PCMI_EF in the CHI Error Flag Register (CHIERFR), and does not change the value of the POCCMD field. 0 Command write idle, command accepted and ready to receive new protocol command. 1 Command write busy, command not yet accepted, and not ready to receive new protocol command. Write Mode Command. This bit controls the write mode of the POCCMD field. 0 Write to POCCMD field on register write. 1 Do not write to POCCMD field on register write.
3–0 POCCMD	Protocol Control Command. The application writes to this field to issue a protocol control command to the PE. The FlexRay module sends the protocol command to the PE immediately. While the transfer is running, the BSY bit is set. 0000 ALLOW_COLDSTART — Immediately activate capability of node to cold start cluster. 0001 ALL_SLOTS — Delayed[1] transition to the all slots transmission mode. 0010 CONFIG — Immediately transition to the POC:config state. 0011 FREEZE — Immediately transition to the POC:halt state. 0100 READY, CONFIG_COMPLETE — Immediately transition to the POC:ready state. 0101 RUN — Immediately transition to the POC:startup start state. 0110 DEFAULT_CONFIG — Immediately transition to the POC:default config state. 0111 HALT — Delayed transition to the POC:halt state 1000 WAKEUP — Immediately initiate the wakeup procedure. 1001 Reserved 1010 Reserved 1011 Reserved 1100 RESET[2] — Immediately reset the Protocol Engine. 1101 Reserved 1110 Reserved 1111 Reserved

[1] Delayed means on completion of current communication cycle.

[2] Additional to Flexray Communications System Protocol Specification, Version 2.1 Rev A

4.2.4 Protocol Configuration Register 1 (PCR1)

Reason: additional FlexRay receive filter not implemented.

MFR4300: PCR1[14]: filter_bypass (was not implemented)

MFR4310: PCR1[14]: 0 (read only)

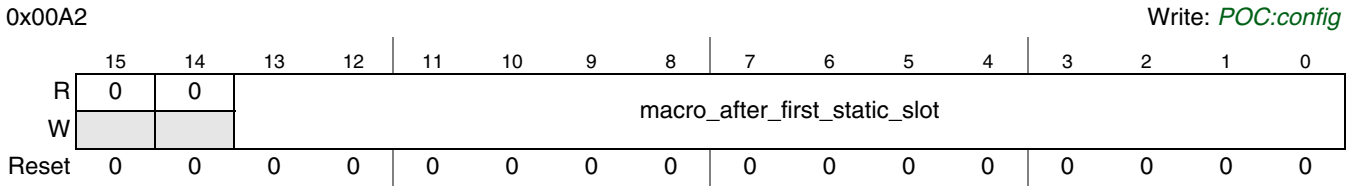

Figure 7. Protocol Configuration Register 1 (PCR1)

4.2.5 Protocol Configuration Register 22 (PCR22)

Reason: implemented undocumented test feature.

MFR4300: PCR22[15]: 0 (read only)

MFR4310: PCR22[15]: reserved (write 0 only for correct operation)

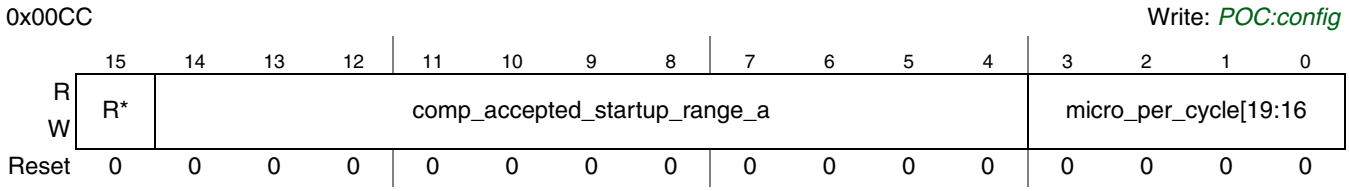

Figure 8. Protocol Configuration Register 22 (PCR22)

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