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Differences Between 908EY16A and 908EY16

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Introduction

The 908EY16A is a new revision of the existing 908EY16. The 908EY16A was designed using the latest HC08 design technology. Emphasis was placed on maintaining compatibility with the existing 908EY16 during the design stage. While this was largely realized, there are a few differences introduced by customer requested improvements and by the use of the latest, enhanced modules. The purpose of this document is to point out the differences between the two versions of the part.

Configuration

A CONFIG3 register has been added to allow for new configuration features of the ESCI, SPI, and ICG. This replaces a reserved register location at address $0009.

Address: $0009

	Bit 7	6	5	4	3	2	1	Bit 0
908EY16:	R	R	R	R	R	R	R	R
908EY16A:	NA	RNGSEL	ESCISRE	SPISRE	MCLKSRE	PORTSRE	ESCISEL	SPISEL
Reset:	0	1	0	0	0	0	0	0

R = Reserved

Figure 1. Configuration Register 3 (CONFIG3)

Enhanced Serial Communications Interface Module (ESCI)

Enhanced transmitter functions are available for the local interconnect network (LIN). The LINT bit has been added to ESCI Baud Rate register. (The bit location was previously reserved.)

Address: $0016

	Bit 7	6	5	4	3	2	1	Bit 0
908EY16:	R	LINR	SCP1	SCP0	R	SCR2	SCR1	SCR0
908EY16A:	LINT	LINR	SCP1	SCP0	R	SCR2	SCR1	SCR0
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 2. ESCI Baud Rate Register (SCBR)

The transmit and receive pins can be remapped to the PTA2 and PTA3 pins. This is selected in the CONFIG3 register. The reset state of these bits maps the ESCI transmit and receive to the same pins as on the 908EY16.

Serial Peripheral Interface Module (SPI)

The four pins associated with the SPI can be remapped to alternate assignments on PTB and PTC. The alternated assignment is selected in the CONFIG3 register. The reset state of these bits maps the SPI functions to the same pins as on the 908EY16.

Internal Clock Generator Module (ICG)

An option to allow the use of high frequency (8 – 32 MHz) crystals for the external oscillator has been added. There is now a range select bit in the CONFIG3 register to select this high frequency range.

Keyboard Interface Module (KBI)

The ability to select whether a keyboard interrupt is triggered by a rising or falling edge has been added. A reserved register has been replaced with the Keyboard Polarity register (KBIPR) at address $000C. While the falling edge trigger was the only mode available on the 908EY16, with the 908EY16A you can set either rising or falling edge and the reset state of the polarity bits will match the original state.

Address: $000C

	Bit 7	6	5	4	3	2	1	Bit 0
908EY16:	R	R	R	R	R	R	R	R
908EY16A:	0/NA	0/NA	0/NA	KBIP4	KBIP3	KBIP2	KBIP1	KBIP0
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 3. Keyboard Interrupt Polarity Register (KBIPR)

Analog-to-Digital Converter Module (ADC)

The original ADC module has been replaced with the improved ADC10 module. While the modules are extremely similar, there are some differences that need to be evaluated for impact on existing software.

- The conversion complete (COCO) bit now functions slightly differently. COCO is now always a read-only bit and will get set regardless of the state of the AIEN bit.
- The divide-by-6 clock selection has been removed. (ADIV2 bit replaced by ADLPC)
- The two left-justified modes for the ADC data format are no longer available.
- A long sample time option has been added to conserve power at the expense of longer conversion times. This option is selected using the new ADLSMP bit in the ADCLK register. (The bit location was previously reserved.)
- The ADC10 will now run in stop mode if the ACLKEN bit is set to enable the asynchronous clock inside the ADC10 module. Utilizing stop mode for an ADC conversion gives the quietest operating mode to get extremely accurate ADC readings. (The bit location now used by ACLKEN was unimplemented — it always read as a 0 and writes to that location had no affect.)
- The ADC10 conversion time is now anywhere from 21 ADC clock cycles to 44 ADC clock cycles depending on ACLKEN. The original ADC module in the 908EY16 had a conversion time of 16 to 17 ADC clock cycles. The bits that control these clocking operations are in the ADCLK register. These changes are shown in Figure 4.

Address: $003F

	Bit 7	6	5	4	3	2	1	Bit 0
908EY16:	ADIV2	ADIV1	ADIV0	ADICLK	MODE1	MODE0	R	0/NA
908EY16A:	ADLPC	ADIV1	ADIV0	ADICLK	MODE1	MODE0	ADLSMP	ACLKEN
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 4. ADC10 Clock Register (ADCLK)

- Enabling an ADC channel no longer overrides the digital I/O function of the associated pin. To prevent the digital I/O from interfering with the ADC read of the pin, the data direction bit associated with the port pin must be set as input.

Monitor Mode

Monitor Extended Security

An extended security feature has been added to the 908EY16 monitor operation. When the extended security location is programmed with zero and all 8 byte security matches, the monitor is terminated in an infinite loop automatically. To unlock extended security, the part must enter monitor mode with failed security and then the FLASH must be mass-erased to erase the whole FLASH. The extended security location in the 908EY16A is located at address $FDFF. The user should check this location in their software to ensure that it will not cause unexpected operation.

Zeroes in Security Bytes

An additional check has been added to the verification of the security bytes. The number of zero bytes used for the security bytes is limited to 5. More than 5 bytes of zero out of the 8 security bytes will cause the security check to fail. The user should check the values programmed into locations $FFF6–$FFFD to ensure that this requirement is not violated.

Forced Monitor Mode Baud Rate

The baud rate used for the 908EY16 Forced Monitor Mode was set at ~6300 baud. In the 908EY16A, this has been changed to 9600 baud. In addition, the trim value stored in FLASH is used in this mode to ensure that the tolerance required for communicating at this rate is met.

Monitor ROM FLASH Programming Routines

Erase

The existing 908EY16 call for erase uses a RAM variable called CTRLBYT to determine whether the call is for page or mass erase. The 908EY16A routine uses the address passed to determine the page to be erased. (If ADDR = FLBPR, then a mass erase is performed.) If the parameters for the current 908EY16 routine are passed to the new 908EY16A routine for a page erase, it would work correctly. Using an existing 908EY16 call to mass erase the 908EY16A will not work.

A minor difference is that the new 908EY16A routine preserves the original state of the I bit while the existing 908EY16 erase routine sets the I bit and leaves it set on exit.

Program

The existing 908EY16 routine uses the row programming method to program any range of addresses (starting address in H:X and ending address in RAM at LADDR, data to be programmed is in RAM starting after LADDR). This routine is interrupted every 6 bytes to service the COP.

The 908EY16A routine uses the same variables, so the call setup would be the same. In the 908EY16A, the COPD bit is checked. If COP servicing is required, then a byte-by-byte algorithm is used to program the range. If no COP servicing is required, then a combination of byte-by-byte and row programming is used for a faster algorithm. (In fact, the fastest programming would occur if the start address is the start of a row and the end address is the end of the same row. Then only the faster row programming method would be used.) To this point, the routines are compatible. However, there is a range limitation on this second algorithm. If a range is passed that crosses an xxFF to xx00 boundary, then it will fail. The byte-by-byte algorithm does not have this limitation.

Table 1. Programming Routine Comparison

Routine	908EY16	908EY16A
Page erase	I bit set on exit	I bit restored to value at time of call
Mass erase	Selected with CTRBYT	Selected with ADDR = FLBPR
Program	No restrictions on range to be programmed	If COPD = 1, range cannot include xxFF/xx00 boundary

The maximum number of bytes required for the stack for all FLASH programming routines is now 13 bytes. In the 908EY16, the maximum number of stack locations was 12 bytes. The user should check to verify that enough stack space is set aside to accommodate this one byte increase.

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