Engineering Bulletin

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Differences Between the HC908GZ60 and HC908GZ16

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Introduction

This engineering bulletin discusses the main differences between the HC908GZ60 and the HC908GZ16. It should be used in conjunction with the most up to date specification for each device, to ensure that all differences have been captured.

The HC908GZ16 and the HC908GZ60 are both available in 32-pin LQFP and 48-pin LQFP packages, and are pin-for-pin compatible. The HC908GZ60 is also available in 64-pin QFP package; the additional features available on the HC908GZ60 in this package type are summarized at the end of this document.

Main Device Differences

Memory Map

FLASH and RAM sizes are different. The HC908GZ16 has 16K of on-chip FLASH memory; the HC908GZ60 has 60K of on-chip FLASH. The HC908GZ16 has 1K of on-chip random access memory (RAM); the HC908GZ60 has 2K of RAM. **Table 1** shows the location of FLASH and RAM for both devices.

The HC908GZ16 contains on-chip FLASH support routines residing in ROM (read-only-memory) that can be used to program, erase and verify FLASH. The HC908GZ60 does not contain these routines.

Table 1. Memory Addresses

Device	FLASH	RAM
HC908GZ16	$C000-FDFF	$0040-043F
HC908GZ60	$0462-04FF	$0040-043F
	$0980-1B7F	$0580-097F
	$1E20-7FFF	
	$8000-FDFF	

Configuration Registers

Both devices contain two configuration registers, CONFIG1 and CONFIG2. These registers are located at the same address with identical bit polarities; however, the HC908GZ60 has three extra bits in CONFIG2 that are used to control MCLK. MCLK is a clock signal that, when enabled, is output from the HC908GZ60 on PTD0. It can be used to clock other devices in the system. The MCLK signal can be generated from the crystal or from the bus clock. The MCLKSEL bit is used to determine which one will be the source. The other two bits associated with MCLK select the divider value or switch off the MCLK. The availability of MCLK on PTD0 allows the MCU to clock external devices at various frequencies. It can also prove useful when developing code: for example, to check that the PLL has been programmed to the correct frequency. This can be done by setting up the PLL, waiting for it to lock, switching the bus clock to the PLL clock, then selecting the bus clock with no divide as the source for MCLK. An oscilloscope can be connected to PTD0 and used to confirm that the frequency of MCLK matches the desired PLL frequency.

The MCLK options are set up using bits [6:4] in CONFIG2. Bit 6 is the MCLK Source Select Bit, MCLKSEL. When this bit is set, the crystal frequency is selected as the MCLK source; when it is clear, the bus frequency is the MCLK source. MCLKSEL is used in conjunction with MCLK [1:0] (bit 5 and bit 4 of CONFIG2. MCLK [1:0] are the MCLK Output Select Bits. Setting MCLK1 and/or MCLK0 enables the PTD0/$\overline{SS}$ pin to be used as a MCLK output clock, provided the DDR0 bit in register DDRD is set. **Table 2** shows the possible options.

Table 2. MCLK Output Select

MCLK1	MCLK0	MCLK Frequency
0	0	MCLK not enabled
0	1	Clock
1	0	Clock divided by 2
1	1	Clock divided by 4

The MCLK option is not available on the HC908GZ16.

The following differences vary slightly depending on the package type (32-pin LQFP or 48-pin LQFP).

Keyboard Interrupt

On the HC908GZ16 and the HC908GZ60, four keyboard interrupt pins are available on the 32-pin LQFP package; eight are available on the 48-pin LQFP package.

For both devices, interrupts can be programmed to be edge-only or edge-and-level interrupt sensitive. On the HC908GZ16, keyboard interrupts can be triggered on a falling edge and/or a low level. The HC908GZ60 offers greater flexibility in that interrupts can be triggered on a falling edge and/or a low level or on a rising edge and/or a high level. To select the desired trigger polarity the user should write a 0 or a 1 to the relevant KBIP[7:0] bit in the Keyboard Interrupt Polarity Register located at $0448. Writing a 1 enables the corresponding keyboard interrupt pin to latch an interrupt request when a rising edge and/or a high level is detected. Conversely, writing a 0 enables the corresponding keyboard interrupt pin to latch an interrupt request when a falling edge and/or a low level is detected.

(The 64-pin QFP HC908GZ60 also has eight keyboard interrupt pins.)

Analog to Digital Converter

Both devices have a 10-bit ADC; however, the HC908GZ60 has extra ADC channels available. The extra ADC channels on the HC908GZ60 are available on Port A. On the HC908GZ60, each port pin on Port A can serve as general purpose I/O, a keyboard interrupt; or an ADC channel. On the HC908GZ16, each port pin on Port A can serve as either a general purpose I/O pin or a keyboard interrupt pin. **Table 3** shows the number of ADC channels available for each device when assembled in 32-pin LQFP or 48-pin LQFP packages.

Table 3. ADC Channels Available versus Package Type

Device	Package	No. of ADC channels
HC908GZ16	32-pin LQFP	6 channels on PTB
HC908GZ16	48-pin LQFP	8 channels on PTB
HC908GZ60	32-pin LQFP	6 channels on PTB and 4 channels on PTA
HC908GZ60	48-pin LQFP	8 channels on PTB and 8 channels on PTA

(Twenty-four ADC channels are available on the 64-pin QFP HC908GZ60: eight on Port A, eight on Port B and eight on Port G. Port A is also multiplexed with keyboard interrupts.)

64-pin QFP HC908GZ60 Only

As previously stated, the HC908GZ60 is also available in a 64-pin QFP package. This package option of the HC908GZ60 offers all the features as the other package options, plus the following:

- Extra I/O ports:
  - Port F (with higher current drive on PTF[3:0])
  - Port G
- Extra ADC channels
- A 6-channel timer, TIM2 (and, consequently, additional interrupt vectors).

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