Functional Differences Between Masks 0H82G and 4J22A of the DSP56303

This document describes the differences between two masks of the DSP56303: the newer mask 0H82G and mask immediately preceding it 4J22A.

CONTENTS

1 CDR II Process

The 0H82G mask is the first mask of the DSP56303 to use the communications design rules (CDRII) process. It also has new IO and a new PLL, with the requisite change in the PLL capacitor equation (PCAP).

2 PLL Input Capacitor

The process change results in a changed requirement for computing the size of C_{PCAP}, the capacitor used with the PCAP input. 1 lists the new formulas for computing the value of this input capacitor for the DSP

3 Differences Overview

The primary functional differences between the two mask sets are due to inherent differences between the two design technologies. **Table 1** compares the mask sets.

Table 1. Functional Comparison of 0H82G and 4J22A

Feature	4J22A			0H82G		
	Recommended	Min	Max	Recommended	Min	Max
Technology	0.5 micron	—	—	Sub 0.4 micron	—	—
PLL input capacitor (C_{PCAP})	Uses the following rules: For MF ≤ 4: C_{PCAP} = [(500 × MF) – 150] pF For MF > 4: C_{PCAP} = (690 × MF) pF	(MF × 425) – 125 MF × 520	(MF × 590) – 175 MF × 920	Use the following rules: For MF ≤ 4: C_{PCAP} = [(680 × MF) – 120] pF For MF > 4: C_{PCAP} = (1100 × MF) pF	(MF × 580) – 100 MF × 830	(MF × 780) – 140 MF × 1470

4 Asynchronous Bus Arbitration

In the Operating Mode Register (OMR) of the 0H82G is a new Asynchronous Bus Arbitration (ABE) bit to support external access at high frequencies. As **Figure 1** shows, bit 13 in the OMR enables Asynchronous Bus Arbitration. For convenience, **Table 2** defines all the OMR bits available in the 0H82G mask set of the DSP56303. The new ABE bit is highlighted in a bold red font.

SCS								EOM								COM							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			SEN	WRP	EOV	EUN	XYS	ATE	APD	ABE	BRT	TAS	BE	CDP1:0		MS	SD		EBD	MD	MC	MB	MA

ATE—Address Trace Enable
APD—Address Attribution Priority Disable
ABE—Async. Bus Arbitration Enable
BRT—Bus Release Timing
TAS—$\overline{TA}$ Synchronize Select
BE—Burst Mode Enable
CDP1—Core-DMA Priority 1
CDP0—Core-DMA Priority 0
MS—Memory Switch Mode
SD—Stop Delay
EBD—External Bus Disable
MD—Operating Mode D
MC—Operating Mode C
MB—Operating Mode B
MA—Operating Mode A
SEN—Stack Extension Enable
WRP—Extended Stack Wrap Flag
EOV—Extended Stack Overflow Flag
EUN—Extended Stack Underflow Flag
XYS—Stack Extension Space Select

— Reserved bit; read as zero; should be written with zero for future compatibility

Figure 1. Operating Mode Register (OMR)

Table 2. Operating Mode Register (OMR) Bit Definitions

Bit Number	Bit Name	Reset Value	Description
23 – 21		0	Reserved. Set to 0 for future compatibility.
20	SEN	0	**Stack Extension Enable** Enables/disables the stack extension in data memory. If the SEN bit is set, the extension is enabled. Hardware reset clears this bit, so the default out of reset is a disabled stack extension.
19	WRP	0	**Stack Extension Wrap Flag** Set when copying from the on-chip hardware stack (System Stack Register file) to the stack extension memory begins. You can use this flag during the debugging phase of the software development to evaluate and increase the speed of software-implemented algorithms. The WRP flag is a *sticky bit* (that is, cleared only by hardware reset or by an explicit MOVE operation to the OMR).
18	EOV	0	**Stack Extension Overflow Flag** Set when a stack overflow occurs in Stack Extended mode. Extended stack overflow is recognized when a push operation is requested while SP = SZ (Stack Size register), and the Extended mode is enabled by the SEN bit. The EOV flag is a *sticky bit* (that is, cleared only by hardware reset or by an explicit MOVE operation to the OMR). The transition of the EOV flag from zero to one causes a Priority Level 3 (Non-maskable) stack error exception.
17	EUN	0	**Stack Extension Underflow Flag** Set when a stack underflow occurs in Extended Stack mode. Extended stack underflow is recognized when a pull operation is requested, SP = 0, and the SEN bit enables Extended mode. The EUN flag is a *sticky bit* (that is, cleared only by hardware reset or by an explicit MOVE operation to the OMR). Transition of the EUN flag from zero to one causes a Priority Level 3 (Non-maskable) stack error exception. NOTE: While the chip is in Extended Stack mode, the UF bit in the SP acts like a normal counter bit.
16	XYS	0	**Stack Extension XY Select** Determines whether the stack extension is mapped onto X or Y memory space. If the bit is clear, then the stack extension is mapped onto the X memory space. If the XYS bit is set, the stack extension is mapped to the Y memory space.
15	ATE	0	**Address Trace Enable** When set, the Address Trace Enable (ATE) bit enables Address Trace mode. The Address Trace mode is a debugging tool that reflects internal memory accesses at the external address lines.
14	APD	0	**Address Attribution Priority Disable** Disables the priority assigned to the Address Attribute signals (AA0-AA3). When APD = 0 (default setting), the four Address Attribute signals each have a certain priority: AA3 has the highest priority, AA0 has the lowest priority. Therefore, only one AA signal can be active at one time. This allows continuous partitioning of external memory; however, certain functions, such as using the AA signals as additional address lines, require the use of additional interface hardware. When APD is set, the priority mechanism is disabled, allowing more than one AA signal to be active simultaneously. Therefore, the AA signals can be used as additional address lines without the need for additional interface hardware.

Table 2. Operating Mode Register (OMR) Bit Definitions (Continued)

Bit Number	Bit Name	Reset Value	Description
13	ABE	0	**Asynchronous Bus Arbitration Enable** Eliminates the setup and hold time requirements (with respect to CLKOUT) for BB and BG, and substitutes a required non-overlap interval between the deassertion of one BG input to a DSP56300 family device and the assertion of a second BG input to a second DSP56300 family device on the same bus. When the ABE bit is set, the BG and BB inputs are synchronized. This synchronization causes a delay between a change in BG or BB until this change is actually accepted by the receiving device.
12	BRT	0	**Bus Release Timing** Selects between fast or slow bus release. If BRT is cleared, a Fast Bus Release mode is selected (that is, no additional cycles are added to the access and BB is not guaranteed to be the last Port A pin that is tri-stated at the end of the access). If BRT is set, a Slow Bus Release mode is selected (that is, an additional cycle is added to the access, and BB is the last Port A pin that is tri-stated at the end of the access).
11	TAS		**TA Synchronize Select** Selects the synchronization method for the input Port A pin—TA (Transfer Acknowledge). If TAS is cleared, you are responsible for asserting the TA pin in synchrony with the chip clock, as described in the technical data sheet. If TAS is set, the TA input pin is synchronized inside the chip, thus eliminating the need for an off-chip synchronizer. Note that the TAS bit has no effect when the TA pin is deasserted: you are responsible for deasserting the **TA** pin in synchrony with the chip clock, regardless of the value of TAS.
10	BE	0	**Cache Burst Mode Enable** Enables/disables Burst mode in the memory expansion port during an instruction cache miss. If the bit is cleared, Burst mode is disabled and only one program word is fetched from the external memory when an instruction cache miss condition is detected. If the bit is set, Burst mode is enabled, and up to four program words are fetched from the external memory when an instruction cache miss is detected.
9–8	CPD	1	**Core-DMA Priority** Specify the priority of core and DMA accesses to the external bus. 00 — Determined by comparing status register CP[1:0] to the active DMA channel priority 01 — DMA accesses have higher priority than core accesses 10 — DMA accesses have the same priority as the core accesses 11 — DMA accesses have lower priority than the core accesses
7	MS	0	**Memory Switch Mode** Allows some internal data memory (X, Y, or both) to become part of the chip internal Program RAM. **Notes:** **1.** Program data placed in the Program RAM/Instruction Cache area changes its placement after the MS bit is set (that is, the Instruction Cache always uses the highest internal Program RAM addresses). **2.** To ensure proper operation, place six NOP instructions after the instruction that changes the MS bit. **3.** To ensure proper operation, do not set the MS bit while the Instruction Cache is enabled (CE bit is set in SR).

Table 2. Operating Mode Register (OMR) Bit Definitions (Continued)

Bit Number	Bit Name	Reset Value	Description
6	SD	0	**Stop Delay Mode** Determines the length of the delay invoked when the core exits the Stop state. The STOP instruction suspends core processing indefinitely until a defined event occurs to restart it. If SD is cleared, a 128K clock cycle delay is invoked before a STOP instruction cycle continues. However, if SD, the delay before the instruction cycle continues is 16 clock cycles. The long delay allows a clock stabilization period for the internal clock to begin oscillating and to stabilize. When a stable external clock is used, the shorter delay allows faster start-up of the DSP56300 core.
5		0	Reserved. Set to 0 for future compatibility.
4	EBD	0	**External Bus Disable** Disables the external bus controller to reduce power consumption when external memories are not used. When EBD is set, the external bus controller is disabled and external memory cannot be accessed. When EBD is cleared, the external bus controller is enabled and external access can be performed. Hardware reset clears the EBD bit.
3–0	MD–MA		**Chip Operating Mode** Indicate the operating mode of the DSP56300 core. On hardware reset, these bits are loaded from the external mode select pins, MODD, MODC, MODB, and MODA, respectively. After the DSP56300 core leaves the Reset state, MD, MC, MB, and MA can be changed under program control.

5 Errata Fixes

The specific differences in errata items between masks 4J22A and 0H82G are listed in the following tables. A detailed description of each errata item is available in the chip errata documents on the web site listed on the back cover of this document.

Following is a list of the errata items present in the 4J22A mask but not in the 0H82G mask.

Errata Number	Errata Description	Applies to Mask
ES16	Description (added 10/09/1997): When the chip is powered up with PLL enabled (PINIT = 1), the skew between EXTAL and CLKOUT after the PLL locks cannot be guaranteed at high frequency (over 50 MHz, not 100% tested). Workaround: If skew between EXTAL and CLKOUT is needed, power up with PINIT = 0, and then enable the PLL by software.	Fixed on 0H82G

ES36	Description (added 10/09/1997): If the stack extension is enabled, the instructions listed below should not be placed as the next-to-last or as the last instruction of a DO loop (i.e., should not appear at LA-1 or LA). The instructions are: XY Memory Data Move (A-6.76) X Memory Move (A-6.71) Y Memory Move (A-6.73) Long Memory Data Move (A-6.75) Immediate Short Data Move (A-6.68) Register to Register Data Move (A-6.69) Address Register Update (A-6.70) X Memory and Register Data Move (A-6.72) Y Memory and Register Data Move (A-6.74) *Arithmetic Instructions that allow Parallel Moves listed above* IFcc and IFcc.U (A-6.41) Workaround: Insert a NOP or other instruction not listed above as the next-to-last and last instructions in the DO loop.	Fixed on 0H82G

ES47	Description (added 10/09/1997):
	
	If the DMA channel and the core access the same 1/4 K internal X data, Y data, or program memory page, and the DMA interrupt is enabled, a false interrupt may occur in addition to the correct one.
	
	Workaround:
	
	Ensure that the channel's DTD status bit in the DSTR is set before jumping to the Interrupt Service Routine (i.e., the interrupt is correct only when DTD is set).
	
	Example:
	
	`ORG P:I_DMA0`
	`JSSET #M_DTD0,X:M_DSTR,ISR_ ; ISR_ is the Interrupt Service`
	`; Routine label for DMA channel 0`
		Fixed on 0H82G

ES53	Description (added 10/09/1997): Using the JTAG instruction code 1111 ($F) or 1101 ($D) for the BYPASS instruction may cause the chip to enter Debug mode (which then correctly sets the Status bits (OS[1:0]) in the OnCE Status and Control Register (OSCR[7:6]) and asserts the $\overline{DE}$ output to acknowledge the Debug mode status). Workaround: Use one of the following alternatives: a. If possible, do not use instruction code 1111 ($F) or 1101 ($D) for the BYPASS instruction. Use one of the other defined BYPASS instruction codes (i.e., any code from 1000–1100 ($8–$C) or 1110 ($E)). b. If you must use instruction code 1111 ($F) or 1101 ($D), use the following procedure: — While the $F or $D instruction code is in the Instruction Register, ensure that the JTAG Test Access Port (TAP) state machine does not pass through the JTAG Test-Logic-Reset state while accessing any JTAG registers (i.e., Instruction Register, Boundary Scan Register, or ID Register). — Before using any other JTAG instruction, load one of the other BYPASS instruction codes (i.e., any code from 1000–1100 ($8–$C) or 1110 ($E)) into the instruction register. Then, any other JTAG instruction may be used.	Fixed on 0H82G

Following is a list of the silicon errata items present in the 0H82G mask but not in the 4J22A mask.

Errata Number	Errata Description	Applies to Mask
ES33	Description (added 3/3/1997): When using the JTAG instructions SAMPLE/PRELOAD, EXTEST, and CLAMP, erroneous data may be driven out on the parallel pins and TDO. Data cannot be shifted through the Boundary Scan Register (BSR) using the SAMPLE/PRELOAD instruction. Because the BSR must be preloaded using the SAMPLE/PRELOAD instruction, the EXTEST and CLAMP instructions cannot be used for testing the board connections. Workaround: None available.	0H82G

ES94	Description (added 8/10/98):
	
	Enabling any DMA channel by software for transferring a block of data (TM=011 in the channel control register) might not work properly.
	
	Workaround:
	
	Triggering of a channel for block transfer by software can be replaced by triggering of the DMA channel for block transfer by a peripheral (that is, Timer, SCI etc.) that is not used while the block of data should be transferred by DMA. This can be done as follows:
	
	1. Set the DSR, DDR and DCO registers of the DMA channel according to the application case.
	
	2. Transfer mode of the DMA channel (in the DCR register) should be set to TM = 000 or TM = 100 (See Section 8.1.5.3, 563xx UM).
	
	3. DMA Request Source of the DMA channel should be set according to the chosen peripheral, which should trigger the DMA channel (see Section 8.1.5.6 56300 UM and "DMA Request Sources" Table in the CORE CONFIGURATION item of the 563xx UM).
	
	4. All others fields of the DCR register, except the DE bit, should be set according to the application case.
	
	5. Configure the peripheral to assert its DMA request line;
	
	6. Set DE bit of the DCR register.
	
	Example 1:
	
	Assuming that the SCI is not used while the block of #DCO3 words is transferred by DMA channel 3, the SCI Transmit Data (TDRE = 1, DRS[4:0] = 01111) trigger can be used instead of a software trigger for channel 3.
	
	1. Initialize DMA channel registers
	
	`movep #DSR3,x:M_DSR3`
	`movep #DDR3,x:M_DDR3`
	`movep #DCO3,x:M_DCO3`
	`bset  #0,x:M_PCRE`
	
	Now when the DMA channel is enabled, a transfer of the block begins.
		0H82G

ES101	Description (added 10/26/98):
	
	If the reset mode is expanded mode (for example, mode 0 or mode 8 on the DSP5630x), A MOVE (not a PROGRAM FETCH) from internal P memory to any destination may not work properly.
	
	Workaround:
	
	After each reset ($\overline{\text{RESET}}$) negation and before the first move from internal program memory, execute the following sequence:
	
	`BSET  #M_CE,sr`
	`NOP`
	`NOP`
	`NOP`
	`BCLR  #M_CE,sr`
		0H82G

ES103	Description (added 11/9/98):
	
	When returning from a long interrupt (by RTI instruction), and the first instruction after the RTI is a move to a DALU register (A, B, X, Y), the move may not be correct, if the 16-bit arithmetic mode bit (bit 17 of SR) is changed due to the restoring of SR after RTI.
	
	Workaround:
	
	Replace the RTI with the following sequence:
	
	`movec   ssl,sr`
	`nop`
	`rti`
		0H82G

Following is a list of the documentation errata items present in the 0H82G mask but not in the 4J22A mask.

Errata Number	Errata Description	Applies to Mask

ED32	Description (added 11/9/98; identified as a Documentation errata 2/1/99):
	
	When returning from a long interrupt (by RTI instruction), and the first instruction after the RTI is a move to a DALU register (A, B, X, Y), the move may not be correct, if the 16-bit arithmetic mode bit (bit 17 of SR) is changed due to the restoring of SR after RTI.
	
	Workaround:
	
	Replace the RTI with the following sequence:
	
	`movec   ssl,sr`
	`nop`
	`rti`
	
	Pertains to: DSP56300 Family Manual. Add a new section to Appendix B that is entitled “Sixteen-Bit Compatibility Mode Restrictions.”
		0H82G

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Document Order No.: EB341
Rev. 6
10/2005