NXP Semiconductors
Engineering Bulletin

Document Number: EB00856
Rev 0, 06/2017

MPC5xxx: Proper Methods for Suspending an Active DMA channel

by: NXP Semiconductors

Contents

1 Introduction

This engineering bulletin provides guidance on how to properly suspend and resume an active Direct Memory Access (DMA) channel hardware service request, when the DMA is triggered by a slave module such as the Deserial Serial Peripheral Interface (DSPI), the Sigma Delta Analog to Digital Convertor (SDADC), or other peripheral modules. The information provided here applies to MPC5xxx and S32Kxx families of devices.

2 Overview

DMA allows the user to move data from memory or a peripheral module's registers to another location of memory or another module's registers without CPU interaction. Normally, the DMA and slave module are configured and there is no reason to suspend the DMA channel. However, in some rare cases, it is desirable to suspend a peripheral's DMA hardware service request dynamically while it is in operation. In such a use case, there are certain restrictions for disabling the DMA hardware service request. For coherency, a specific procedure must be followed.

2.1 Procedure to suspend an active DMA channel

If an active DMA channel needs to be suspended, the slave trigger must be stopped first, followed by suspending the DMA. This is done by using the following sequence.

1. Disable the DMA service request at the source peripheral first. Confirm it has been disabled by reading back the appropriate register in the peripheral.
2. Check the DMA's Hardware Request Status register (DMA_HRSx) to ensure there is no pending DMA service request for the DMA channel being suspended. Then, disable the DMA hardware request by clearing the ERQ bit on the appropriate DMA channel via the DMA Channel Clear Enable Request (DMA_CERQ) register . If a service request is present, wait until the request has been processed and the HRS bit reads zero. Then disable the DMA channel hardware request by clearing the ERQ bit.

2.2 Procedure to resume the DMA channel

As with the suspend procedure, the resume sequence must also be properly performed.

1. Enable the DMA hardware service request on the appropriate channel by setting the ERQ bit via Set Enable Request Register (DMA_SERQ)

2. Enable the DMA service request at the source peripheral.

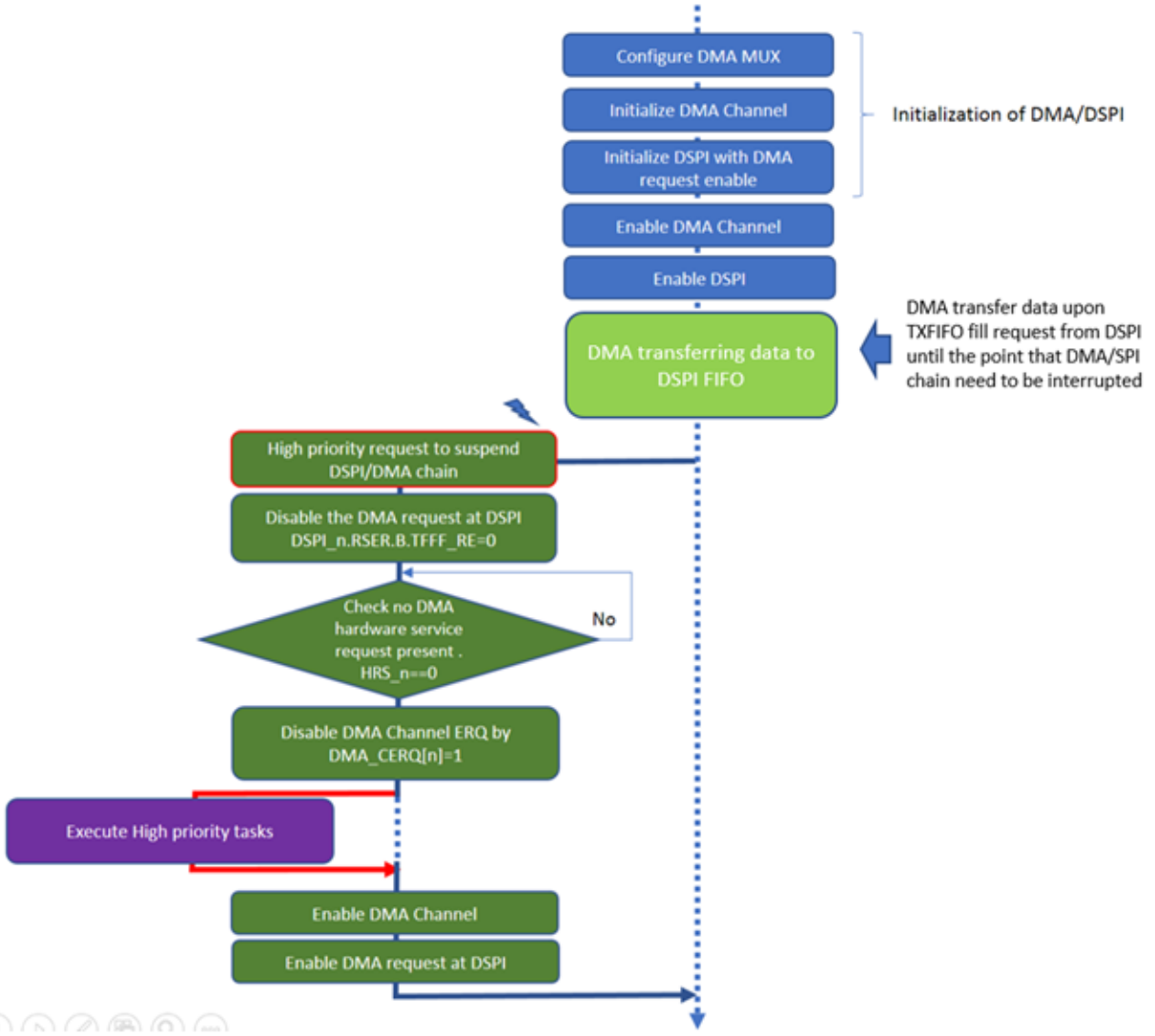
3 Use case example

One use case that could require suspending is when using the DMA with the DSPI module.

The DSPI is set as the master for transmitting data via a DMA request when the DSPI_TXFIFO has an empty slot. The TXFIFO fill DMA request enable/disable can be configured by the TFFF_RE bit of the DSPI_RESR register. The DMA will transfer the next command & data to the TXFIFO upon the request. If the DMA/DSPI transfer loop needs to be suspended, use the following steps.

1. Disable the DMA service request at the source by writing '0' to the DSPI_RSER.B.TFFF_RE bit. Confirm that DSPI_RSER.B.TFFF_RE == 0.
2. Ensure there is no DMA request from the DSPI by verifying Hardware Request Status Register (DMA_HRSx)_HRS.b.HRSn == 0 for the appropriate channel. If no service request is present (HRS_n=0), disable the DMA channel by clearing the channel's ERQ bit by DMA_x.CERQ[CH]= 1. If a service request is present, wait until the request has been processed and the HRS bit reads zero.

The following diagram illustrates the procedure described above to suspend an ongoing DSPI/DMA chain.



When a “high priority task” is executing, the user needs to ensure that the application software does not cause any FIFO overflow situation. For example, when the CPU is being used to write to the DSPI TX_FIFO/CMD_FIFO etc.

How To Reach Us

Home Page:

nxp.com

Web Support:

nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.