DATA SHEET

TZA3015HW

30 Mbit/s to 3.2 Gbit/s A-rate™ 4-bit fibre optic transceiver

Preliminary specification
Supersedes data of 2003 Oct 06

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Philips
Semiconductors

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30 Mbit/s to 3.2 Gbit/s A-rate™ 4-bit fibre optic transceiver

TZA3015HW

FEATURES

General

- A-rabitte™(1): supports any bit rate from 30 Mbit/s to 3.2 Gbit/s with one single reference frequency
- 4-bit parallel interface
- Selectable Double Data Rate (DDR, half clock rate) or Single Data Rate (SDR) clocking scheme on parallel interface, enabling easy interfacing with FPGA devices
- I²C-bus and pin programmable
- Six selectable reference frequency ranges
- Transmitter, receiver and transceiver modes
- Clean-up loop back mode
- Line loop back mode
- Diagnostic loop back mode
- Serial loop timing mode
- Single 3.3 V power supply.

Limiter

- Limiting amplifier with typical 5 mV input sensitivity
- Received Signal Strength Indicator (RSSI)
- Loss Of Signal (LOS) indicator with adjustable threshold
- Differential overvoltage protection.

Data and clock recovery and synthesizer

- Supports any bit rate from 30 Mbit/s to 3.2 Gbit/s when using I²C-bus interface
- Supports eight pre-programmed (pin selectable) bit rates:
  - SDH/SONET rates at 155.52 Mbit/s, 622.08 Mbit/s, 2488.32 Mbit/s and 2666.06 Mbit/s (STM16/OC48 + FEC)
  - Gigabit Ethernet at 1250 Mbit/s and 3125 Mbit/s
  - Fibre Channel at 1062.5 Mbit/s and 2125 Mbit/s.
- Provides stable clock signal at LOS
- Frequency lock indicator for DCR
- Loss Of Lock (LOL) indicator for synthesizer
- ITU-T compliant jitter tolerance for Data and Clock Recovery (DCR)
- ITU-T compliant jitter transfer for DCR in clean-up loop back mode
- ITU-T compliant jitter generation for synthesizer.

Multiplexer

- 4 : 1 multiplexing ratio
- Supports co-directional and contra-directional clocking
- 4-stage FIFO for wide tolerance to clock skew
- Rail-to-rail parallel inputs compliant with LVPECL, Current-Mode Logic (CML) and LVDS
- Programmable parity checking
- CML data and clock outputs.

Demultiplexer

- 1 : 4 demultiplexing ratio
- Adjustable LVDS output swing
- Frame detection for SDH/SONET and Gigabit Ethernet (GE) frames.

I²C-bus configurable options

- Programmable frequency resolution of 10 Hz
- Independent receive and transmit bit rate
- Slice level adjustment to improve Bit Error Rate (BER)
- Six reference frequency ranges
- Adjustable swing for CML serial data and clock outputs
- Programmable polarity of RF I/Os
- Clock versus data swap for optimum connectivity
- Swap of parallel bus for optimum connectivity
- Mute function for a forced logic 0 output state
- Programmable parity
- Programmable 32-bit frame detection.

(1) A-rate is a trademark of Koninklijke Philips Electronics N.V.

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TZA3015HW

APPLICATIONS

- Any optical transmission system with line rates between 30 Mbit/s and 3.2 Gbit/s
- Physical interface IC in receive and transmit channels
- Transponder applications
- Dense wavelength division multiplexing systems
- Due to DDR clocking option, the ultimate physical interface for FPGA based designs.

GENERAL DESCRIPTION

The TZA3015HW is a fully integrated optical network transceiver containing a limiter, data and clock recovery circuit, clock synthesizer, 1 : 4 demultiplexer and 4 : 1 multiplexer.

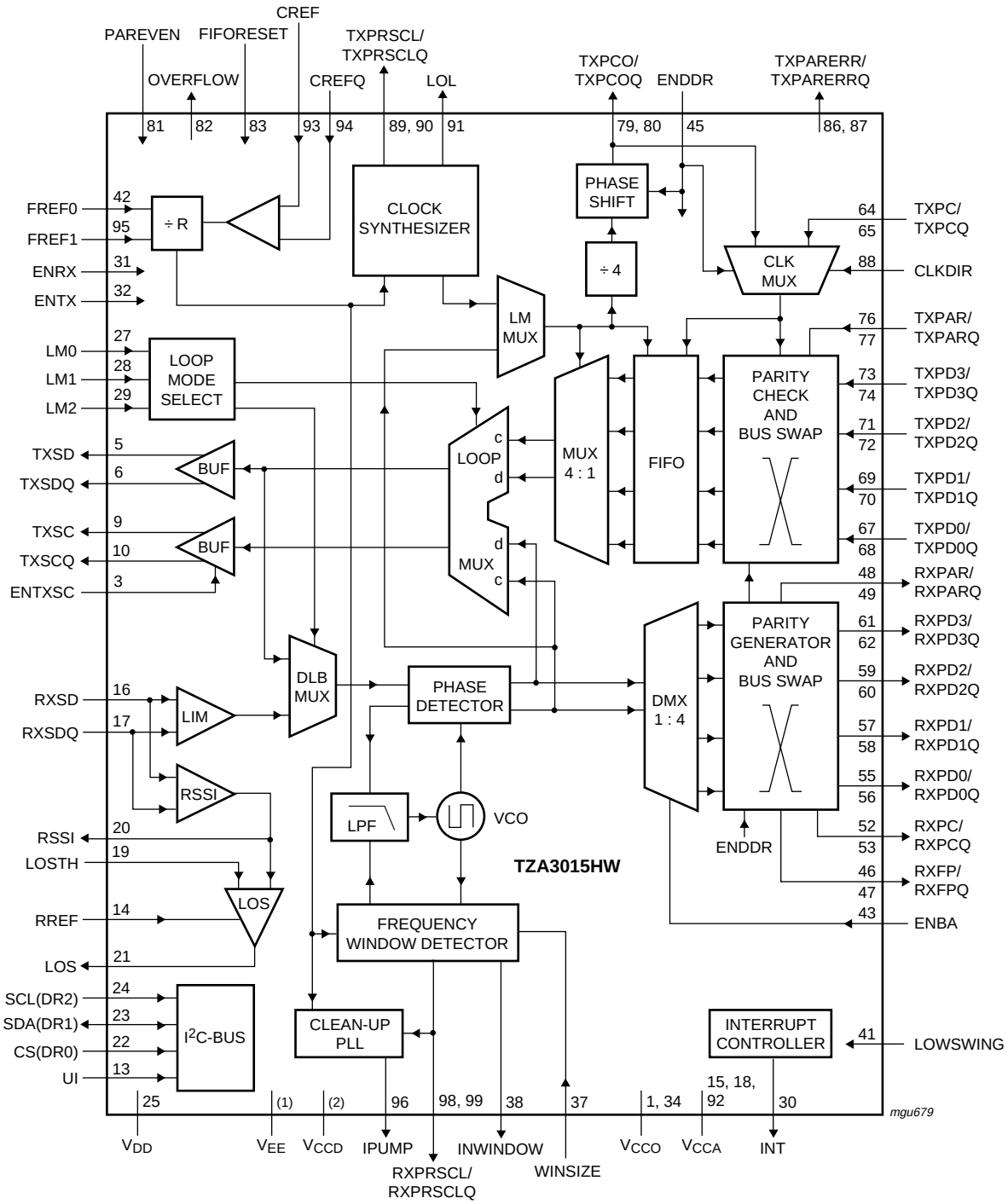
The A-rate feature allows the IC to operate at any bit rate between 30 Mbit/s and 3.2 Gbit/s with one single reference frequency.

All clock signals are generated using a fractional N synthesizer with 10 Hz resolution offering a true continuous rate operating. For full configuration flexibility the transceiver can be programmed by pin and via the I^2C-bus.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3015HW	HTQFP100	plastic thermal enhanced thin quad flat package; 100 leads; body $14 \times 14 \times 1$ mm; exposed die pad	SOT638-1

BLOCK DIAGRAM



(1) Connected to pins 2, 12, 26, 33, 35, 40, 50, 84 and 100.

(2) Connected to pins 4, 7, 8, 11, 36, 39, 44, 51, 54, 63, 66, 75, 78, 85 and 97.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{EE}	die pad	common ground plane
V_{CCO}	1	supply voltage (clock generator)
V_{EE}	2	ground
ENTXSC	3	enable serial clock
V_{CCD}	4	digital supply voltage
TXSD	5	serial data output
TXSDQ	6	serial data output inverted
V_{CCD}	7	supply voltage (digital part)
V_{CCD}	8	supply voltage (digital part)
TXSC	9	serial clock output
TXSCQ	10	serial clock output inverted
V_{CCD}	11	supply voltage (digital part)
V_{EE}	12	ground
UI	13	user interface select input
RREF	14	reference resistor input
V_{CCA}	15	supply voltage (analog part)
RXSD	16	serial data input
RXSDQ	17	serial data input inverted
V_{CCA}	18	supply voltage (analog part)
LOSTH	19	loss of signal threshold input
RSSI	20	received signal strength indicator output
LOS	21	loss of signal output
CS(DR0)	22	chip select output (data rate select input 0)
SDA(DR1)	23	I^2C-bus serial data input and output (data rate select input 1)
SCL(DR2)	24	I^2C-bus serial clock input (data rate select input 2)
V_{DD}	25	supply voltage (digital)
V_{EE}	26	ground
LM0	27	loop mode select input 0
LM1	28	loop mode select input 1
LM2	29	loop mode select input 2
INT	30	interrupt output
ENRX	31	enable receiver
ENTX	32	enable transmitter
V_{EE}	33	ground
V_{CCO}	34	supply voltage (clock generator)
V_{EE}	35	ground

SYMBOL	PIN	DESCRIPTION
V_{CCD}	36	supply voltage (digital part)
WINSIZE	37	wide and narrow frequency detect window select input
INWINDOW	38	frequency window detector output
V_{CCD}	39	supply voltage (digital part)
V_{EE}	40	ground
LOWSWING	41	enable low LVDS swing
FREF0	42	reference frequency select input 0
ENBA	43	enable byte alignment
V_{CCD}	44	supply voltage (digital part)
ENDDR	45	enable DDR
RXFP	46	frame pulse output
RXFPQ	47	frame pulse output inverted
RXPAR	48	parity output
RXPARQ	49	parity output inverted
V_{EE}	50	ground
V_{CCD}	51	supply voltage (digital part)
RXPC	52	parallel clock output
RXPCQ	53	parallel clock output inverted
V_{CCD}	54	digital supply voltage
RXPD0	55	parallel data output 0
RXPD0Q	56	parallel data output 0 inverted
RXPD1	57	parallel data output 1
RXPD1Q	58	parallel data output 1 inverted
RXPD2	59	parallel data output 2
RXPD2Q	60	parallel data output 2 inverted
RXPD3	61	parallel data output 3
RXPD3Q	62	parallel data output 3 inverted
V_{CCD}	63	supply voltage (digital part)
TXPC	64	parallel clock input
TXPCQ	65	parallel clock input inverted
V_{CCD}	66	supply voltage (digital part)
TXPD0	67	parallel data input 0
TXPD0Q	68	parallel data input 0 inverted
TXPD1	69	parallel data input 1
TXPD1Q	70	parallel data input 1 inverted
TXPD2	71	parallel data input 2
TXPD2Q	72	parallel data input 2 inverted
TXPD3	73	parallel data input 3
TXPD3Q	74	parallel data input 3 inverted

SYMBOL	PIN	DESCRIPTION
V_{CCD}	75	supply voltage (digital part)
TXPAR	76	parity input
TXPARQ	77	parity input inverted
V_{CCD}	78	supply voltage (digital part)
TXPCO	79	transmitter parallel clock output
TXPCOQ	80	transmitter parallel clock output inverted
PAREVEN	81	parity select input (odd or even)
OVERFLOW	82	FIFO overflow alarm output
FIFORESET	83	FIFO reset input
V_{EE}	84	ground
V_{CCD}	85	supply voltage (digital part)
TXPARERR	86	parity error output
TXPARERRQ	87	parity error output inverted
CLKDIR	88	selection input between co- and contra-directional clocking

SYMBOL	PIN	DESCRIPTION
TXPRSCL	89	prescaler synthesizer output
TXPRSCLQ	90	prescaler synthesizer output inverted
LOL	91	loss of lock output
V_{CCA}	92	supply voltage (analog part)
CREF	93	reference clock input
CREFQ	94	reference clock input inverted
FREF1	95	reference frequency select input 1
IPUMP	96	clean-up PLL charge pump output
V_{CCD}	97	supply voltage (digital part)
RXPRSCL	98	prescaler DCR output
RXPRSCLQ	99	prescaler DCR output inverted
V_{EE}	100	ground

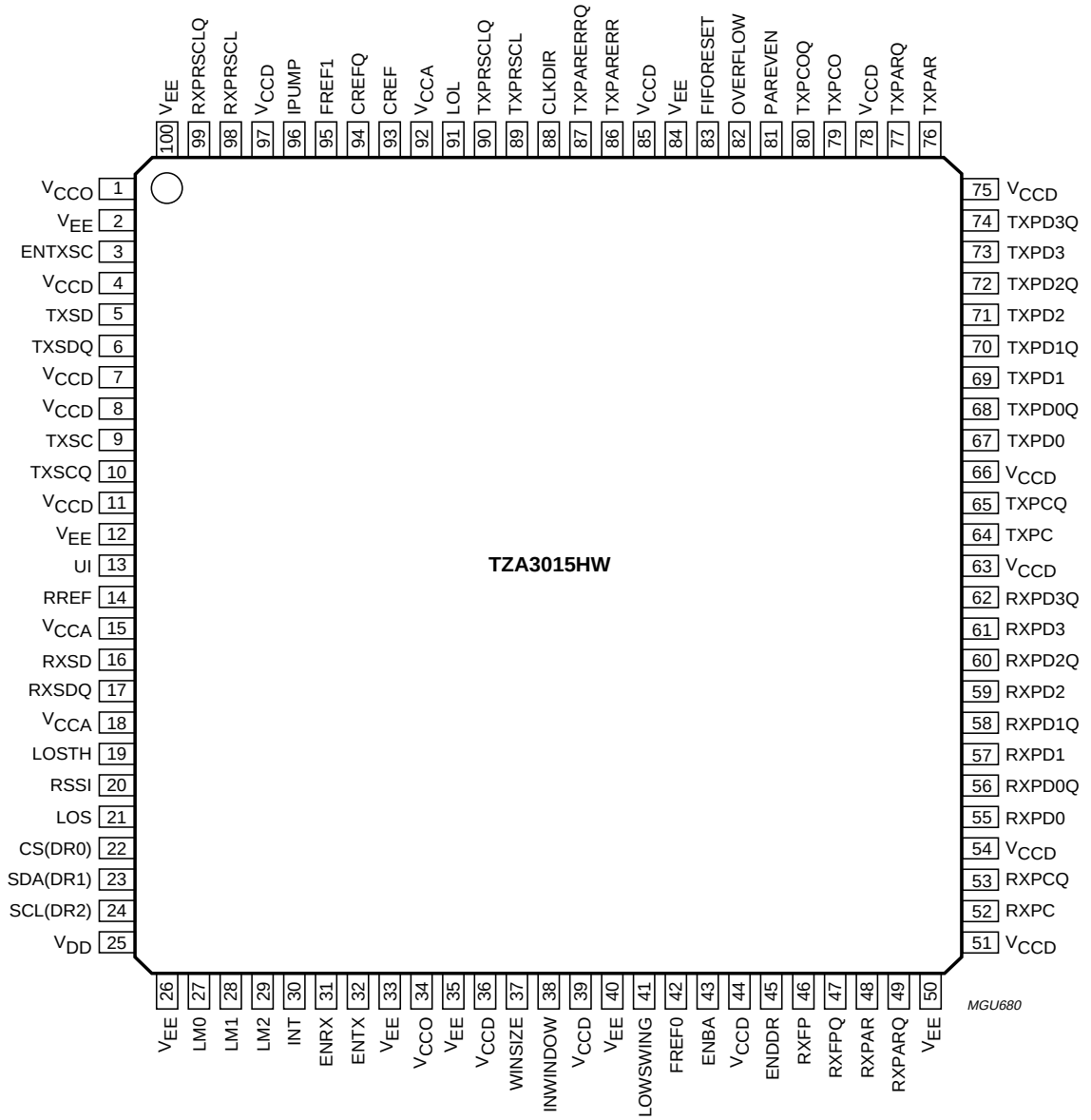


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TZA3015HW contains the following main blocks:

- General part: configuration via I²C-bus mode or pre-programmed mode
- Receiver part: limiting amplifier, data and clock recovery and demultiplexer
- Transmitter part: clock synthesizer and multiplexer.

General

CONFIGURATION

The IC features two types of user interface: I²C-bus or direct pin programming of eight predefined modes. The mode selection is set by pin UI.

The I²C-bus mode is operational and A-rate functionality is enabled if pin UI is left open-circuit or connected to V_{CC} (see Table 1). If pin UI is connected to V_{EE}, the eight pre-programmed modes can be selected with pins CS(DR0), SDA(DR1) and SCL(DR2).

Table 1 Truth table for pin UI

UI	MODE	PIN 22	PIN 23	PIN 24
LOW	pre-programmed	DR0	DR1	DR2
HIGH	I²C-bus	CS	SDA	SCL

I²C-BUS MODE

In I²C-bus mode the IC can be configured by using pins SDA and SCL. Pin CS has to be HIGH during the I²C-bus read or write actions. When pin CS is made LOW, the programmed configuration remains active, but signals SDA and SCL are ignored. In this way, all ICs in the application with the same I²C-bus address (e.g. other TZA3015HWs) are individually accessible.

The I²C-bus address is given in Table 2.

Table 2 Device address of the TZA3015HW

DEVICE ADDRESS BITS							R/$\overline{W}$
A6	A5	A4	A3	A2	A1	A0	
1	0	1	0	1	0	0	X

After power-up, the TZA3015HW initiates a Power-On Reset (POR) sequence to restore the default settings of the I²C-bus registers, regardless of the user interface. See Table 21 for the defaults and a detailed list of all I²C-bus registers and the meaning of their contents.

Some functions of the TZA3015HW can be controlled both using pre-program mode and via the I²C-bus. In these cases, an extra I²C-bus bit called I2C<pinname> is available to set the programming precedence to pre-programmed or I²C-bus bit (default is selection by pre-programmed).

PRE-PROGRAMMED MODE

The TZA3015HW is primarily intended to be programmed via the I²C-bus. If no I²C-bus control is present in the application, the TZA3015HW can be used in the pre-programmed mode (pin UI = LOW), with reduced functionality. The TZA3015HW functions that are accessible in the pre-programmed mode and their associated pins are:

- All pre-programmed modes are supported by one single reference frequency
- The redefined pins DR0 to DR2 act as standard CMOS inputs that select any of the desired data rates; see Table 3
- Transceiver mode (transceiver, transmitter, receiver, off) (ENRX and ENTX)
- Enable serial clock output (ENTXSC)
- Loss of signal threshold setting (LOSTH)
- Select loop mode (LM0 to LM2)
- Automatic byte alignment for SDH/SONET or Gigabit Ethernet (ENBA)
- Frame detection for SDH/SONET or Gigabit Ethernet
- Even parity generation (PAREVEN)
- In window detection (INWINDOW)
- Sizeable frequency window: 1000 or 0 ppm (WINSIZE)
- Temperature alarm (INT, open drain)
- Co-directional or contra-directional clocking scheme (CLKDIR)
- Enable DDR for both receiver and transmitter (ENDDR)
- CML serial RF outputs with typical 300 mV (p-p) single-ended signal (DC-coupled load)
- Loss of lock detection (LOL)
- FIFO overflow indication (OVERFLOW)
- FIFO reset (FIFORESET)
- Supported reference frequencies: 19.44, 38.88, 155.52 and 622.08 MHz.

Table 3 Truth table for pins DR2 to DR0 (pin UI = V_{EE})

DR2	DR1	DR0	PROTOCOL	BIT RATE (Mbit/s)
LOW	LOW	LOW	STM1/OC3	155.52
LOW	LOW	HIGH	STM4/OC12	622.08
LOW	HIGH	LOW	STM16/OC48	2488.32
LOW	HIGH	HIGH	STM16 + FEC	2666.06
HIGH	LOW	LOW	GE	1250.00
HIGH	LOW	HIGH	10GE	3125.00
HIGH	HIGH	LOW	Fibre Channel	1062.50
HIGH	HIGH	HIGH	Fibre Channel	2125.00

Receiver

LIMITING AMPLIFIER

The TZA3015HW contains a limiting amplifier (see Fig.3).

To achieve optimum receiver sensitivity for any bit rate, the bandwidth of the amplifier is automatically scaled with the bit rate. Wideband noise of the optical front-end (photo detector and transimpedance amplifier) is thus reduced for lower bit rates. When using the I^2C-bus, the bandwidth of the amplifier can be set independently of the bit rate with bits AMP[2:0] in register LIMCON (D3h).

The highest bandwidth is selected as default at power-up.

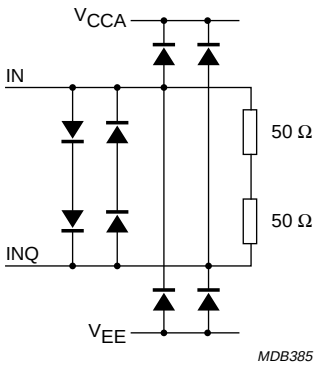


Fig.3 Limiter input termination configuration.

Received Signal Strength Indicator (RSSI)

The signal strength at the input is measured with a logarithmic detector. The logarithmic detector converts the input signal amplitude into a voltage which can be measured at pin RSSI. The RSSI reading has a dynamic range of 40 dB with a sensitivity (S_{RSSI}) of 17 mV/dB (typical) for a $V_{i(p-p)}$ range of 5 to 500 mV (see Fig.4). V_{RSSI} can be calculated using the following formula:

$$V_{RSSI} = V_{RSSI(32mV)} + S_{RSSI} \times 20\log\frac{V_{i(p-p)}}{32\ mV}$$

where: $V_{RSSI(32mV)}$ = 680 mV (typical).

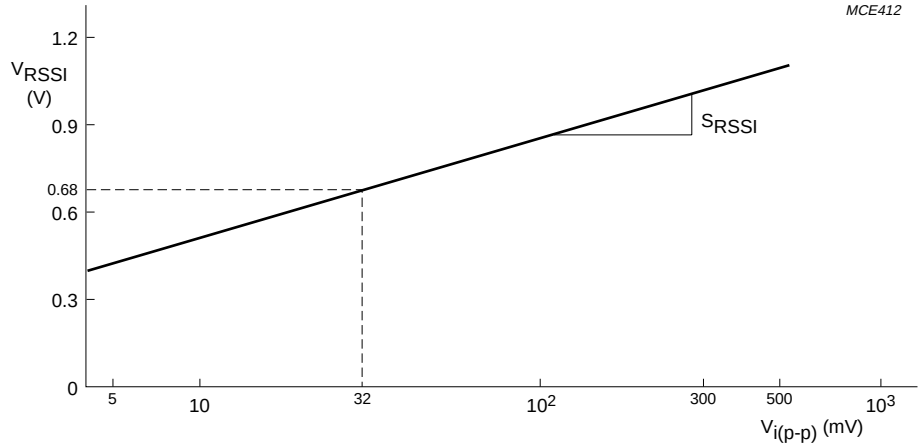


Fig.4 V_{RSSI} as a function of $V_{i(p-p)}$.

Loss Of Signal (LOS) indicator

Besides the analog RSSI output, a digital LOS indication is present on the TZA3015HW. The RSSI level is internally compared with a LOS threshold, which can be set by connecting an external resistor to pin LOSTH or by means of an internal DAC which is accessible via the I²C-bus.

Bit I2CLOSTH of register LIMLOSCON (D1h) enables the 8-bit DAC, of which the value needs to be programmed into register LIMLOSTH (D0h). The threshold level is adjustable in 256 steps from 0 to 1.2 V.

If the received signal strength is below the threshold value, pin LOS will be HIGH. A default hysteresis of 3 dB is applied in the comparator. The hysteresis can be set with bits HTLC[2:0] in register LIMLOSCON (D1h). The programmable range is 0 to 7 dB.

The polarity of the LOS output can be inverted by bit LOSPOL of register LIMLOSCON (D1h) to provide more flexibility in the application.

LOSTH reference setting by external resistor

If the built-in DAC is not used, the reference voltage level to pin LOSTH can be set by connecting an external resistor (R2) between pin LOSTH and ground. V_{LOSTH} is determined by the resistor ratio between R2 and R1 (see Fig.5). For resistor R1 a value of 10 to 20 kΩ is recommended, yielding a current of 120 to 60 μA through R1.

$$V_{LOSTH} = \frac{R2}{R1} \times V_{ref}$$

V_{ref} represents a temperature stabilized and accurate reference voltage of 1.2 V. The minimum threshold level corresponds to 0 V and the maximum to 1.2 V. Hence, the value of R2 may not be higher than R1. The accuracy of V_{LOSTH} depends mainly on the matching of the two external resistors.

Apart from using resistors (R1 and R2) to set the LOS threshold, an accurate external voltage source may also be used.

If no resistor is connected or an external voltage higher than $^2/_3 \times V_{CC}$ is applied to pin LOSTH, the LOS detection circuit (including the RSSI reading) is automatically switched off to reduce power dissipation. This 'auto power off' function only works in the pre-programmed mode. I²C-bus mode allows flexible configuration.

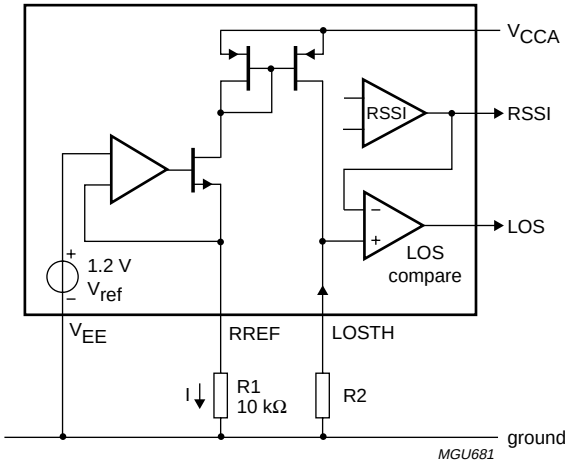


Fig.5 Setting the LOSTH reference level by external resistors.

Slice level adjustment

Due to asymmetrical noise in some optical transmission systems, a pre-detection signal-to-noise ratio improvement can be achieved by adding a DC offset to the input signal. This is done by the slice level circuit in the TZA3015HW. The required offset depends on the photo detector characteristics in the optical front-end and the amplitude of the received signal. The slice level is adjustable between –50 and +50 mV in 512 steps of 0.2 mV.

Bit SLEN of register LIMLOSCON (D1h) enables the slice function. The slice level is set by sign and magnitude convention. The polarity sign is set by bit SLSGN in register LIMLOSCON (D1h). The magnitude is set by an 8-bit DAC, accessible via register LIMSL (D2h), from 0 to 50 mV in 256 steps.

The introduced offset is not present on input pins RXSD(Q), in order not to affect the logarithmic RSSI detector, which would detect the offset as a valid input signal.

DATA AND CLOCK RECOVERY (DCR)

The TZA3015HW recovers the clock and data contents from the incoming bit stream; see Fig.6. The DCR uses a combined frequency and phase locking scheme, providing reliable and quick data acquisition on any bit rate between 30 Mbit/s and 3.2 Gbit/s.

At power-up, coarse adjustment of the free running Voltage Controlled Oscillator (VCO) frequency is required. This is achieved by the Frequency Window Detector (FWD) circuit. The FWD is a conventional frequency locked PLL. The FWD checks the VCO frequency, which has to be within a 1000 ppm window around the required frequency. The FWD then compares the divided VCO frequency, also available on pins RXPRSCL(Q), with the reference frequency on pins CREF(Q), usually 19.44 MHz. If the VCO frequency is outside this window, the FWD disables the Data Phase Detector (DPD) and forces the VCO to a frequency within the window. As soon as the 'in window' condition occurs, which is visible on pin INWINDOW, the DPD is enabled and will lock on the incoming bit stream. Since the VCO frequency is very close to the expected bit rate, the phase acquisition will be almost instantaneous, resulting in quick phase lock to the incoming data stream.

Although the VCO is now locked to the incoming bit stream, the FWD is still supervising the VCO frequency and takes over control if the VCO frequency drifts outside the predefined frequency window. This might occur during a 'loss of signal' situation. Due to the FWD, the VCO frequency is always close to the required bit rate, enabling rapid phase acquisition when the lost input signal returns.

Due to the loose coupling of 1000 ppm, the reference frequency does not need to be highly accurate or stable. Any crystal-based oscillator that generates a reasonably accurate frequency (e.g. 100 ppm) will do. This only holds if the TZA3015HW is used as a receiver since the synthesizer of the transmitter uses the same reference clock. The transmitter does need a very accurate reference frequency.

Fractional N synthesizer in the DCR

The DCR section contains a fractional N synthesizer as frequency acquisition aid for the A-rate functionality. This allows the DCR to synchronize on incoming data, regardless of the received bit rate. Any combination of bit rate and reference frequency is possible, due to the 22 bits fractional N synthesizer, allowing approximately 10 Hz frequency resolution. The LSB (bit K0) should be set to logic 1 to avoid limit cycles (cycles of less than maximum length). This leaves 21 bits (bits K[21:1]), available for free programming.

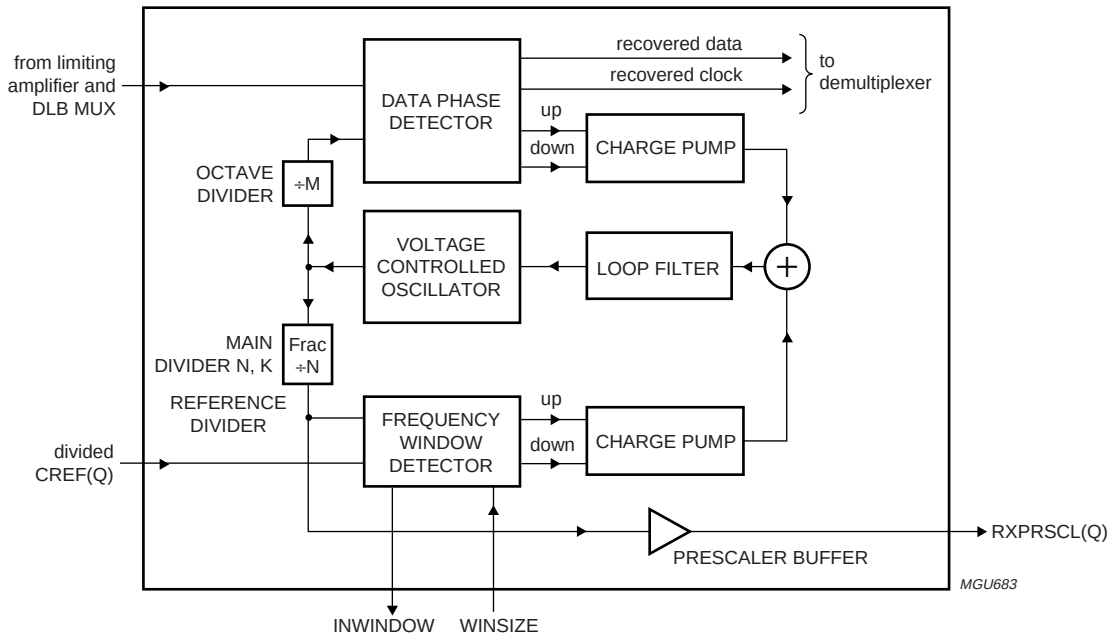


Fig.6 Functional diagram of data and clock recovery.

DCR programming

Programming the DCR involves four dividers:

- Reference divider R
- Main divider N
- Fractional divider K
- Octave divider M.

The first step is to determine in which octave the desired bit rate fits, see Fig.7 and Tables 4 and 5. Figure 7 shows the position of the most commonly used line rates in relation to the defined octaves of the TZA3015HW. Table 5 lists the most commonly used standards together with the associated line rates. Table 4 clarifies the octave definitions. This yields the value for the octave divider M. The value for R is determined by the reference frequency and the received bit rate (see Section “Reference clock programming”).

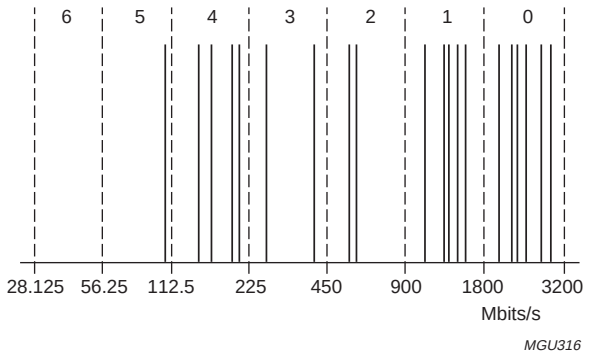


Fig.7 Commonly used line rates and allocation of octaves along a logarithmic bit rate scale.

Table 4 Octave definition

OCTAVE	M	LOWEST BIT RATE (Mbit/s)	HIGHEST BIT RATE (Mbit/s)
0	1	1800	3200
1	2	900	1800
2	4	450	900
3	8	225	450
4	16	112.5	225
5	32	56.25	112.5
6	64	28.125	56.25

Table 5 Most-common optical transmission protocols

PROTOCOL	BIT RATE (Mbit/s)	OCTAVE
10GE	3125.00	0
2xHDTV	2970.00	0
STM16/OC48 + FEC	2666.06	0
STM16/OC48	2488.32	0
DV-6000	2380.00	0
Fibre Channel	2125.00	0
HDTV	1485.00	1
D-1 video	1380.00	1
DV-6010	1300.00	1
Gigabit Ethernet	1250.00	1
Fibre Channel	1062.50	1
OptiConnect	1062.50	1
ISC	1062.50	1
STM4/OC12	622.08	2
DV-6400	595.00	2
Fibre Channel	425.00	3
OptiConnect	265.63	3
Fibre Channel	212.50	4
ESCON/SBCON	200.00	4
STM1/OC3	155.52	4
FDDI	125.00	4
Fast Ethernet	125.00	4
Fibre Channel	106.25	5
OC1	51.84	6

The values for N and K are derived from the division ratio (n.k). The division ratio (n.k) can be calculated with the following formula:

$$n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}}$$

where:

n = integer part of the division ratio

k = fractional part of the division ratio

bit rate = bit rate at serial input in Mbit/s

M = octave divider M

R = reference divider R

f_{ref} = reference frequency in MHz.

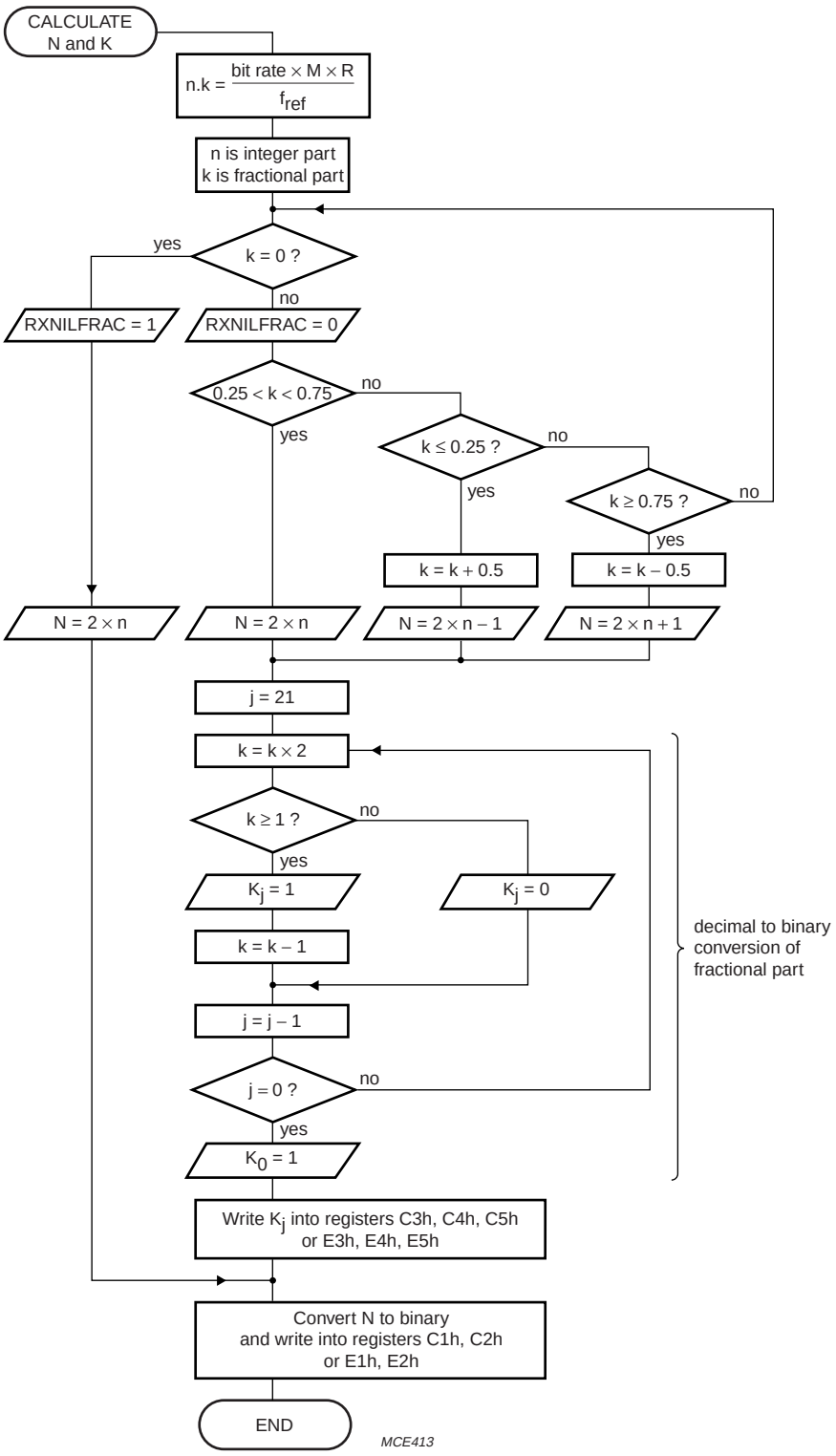


Fig.8 Flowchart for calculating N and K.

Having calculated the division factor (n.k), the values for N and K can be calculated according to the flow depicted in the flowchart of Fig.8.

The value of the octave divider M is programmed by bits RXDIV_M[2:0] in register RXOCTDIV (C0h). The value for the main divider N is programmed by bits RXN[8:0] in registers RXMAINDIV1 (C1h) and RXMAINDIV0 (C2h). The value for the fractional divider K is programmed by bits RXK[21:0] in registers RXFRACN2 to RXFRACN0 (C3h to C5h). Bit RXNILFRAC in register RXFRACN2 (C3h) must be set depending on whether there is a fractional part or not.

Example 1: An SDH or SONET link has a bit rate of 2488.32 Mbit/s (STM16/OC48) and consequently fits in octave number 0, so M = 1. Suppose the reference frequency provided at pins CREF(Q) is 77.76 MHz. This means that the reference division R needs to be 4. The values of n and k can be calculated from the flowchart:

$$n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{2488.32\ \text{Mbits} \times 1 \times 4}{77.76\ \text{MHz}} = 128$$

Since k = 0 in this example, no fractional functionality is required, bit RXNILFRAC (register C3h), should be logic 1. N = 2 × n and no correction is required. Consequently the appropriate values are: R = 4 (register A1h), M = 1 (register C0h) and N = 256 (registers C1h and C2h).

Example 2: An SDH STM16 or SONET OC48 link with FEC has a bit rate of 2666.057143 Mbit/s (15/14 × 2488.32 Mbit/s) and consequently fits in octave number 0, so M = 1. Suppose the reference frequency provided at pins CREF(Q) is 38.88 MHz. This means that the reference division R needs to be 2. The values of n and k can be calculated from the flowchart: $n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{2666.05714283\ \text{Mbits} \times 1 \times 2}{38.88\ \text{MHz}} = 137.1428571$

This means that n = 137, k = 0.1428571 and bit RXNILFRAC (register C3h) should be logic 0. Since k < 0.25, k is corrected to 0.6428571, while the corrected N becomes N = 273. Consequently the appropriate values are: R = 2 (register A1h), M = 1 (register C0h), N = 273 (registers C1h and C2h) and K = 10 1001 0010 0100 1001 0011 (registers C3h to C5h). The FEC bit rate is usually quoted to be 2666.06 Mbit/s. Due to round off errors, this leads to a slightly different value for k than in the example.

Example 3: A Fibre Channel link has a bit rate of 1062.50 Mbit/s and consequently fits in octave number 1, so M = 2. Suppose the reference frequency provided at pins CREF(Q) is 19.44 MHz. This means that the reference division R needs to be 1. The values of n and k can be calculated from the flowchart:

$$n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{1062.50\ \text{Mbits} \times 2 \times 1}{19.44\ \text{MHz}} = 109.3106996$$

This means that n = 109, k = 0.3107 and bit RXNILFRAC should be logic 0 (register C3h). Since k is between 0.25 and 0.75, k does not need to be corrected and N = 2 × n = 218. Consequently the appropriate values are: R = 1 (register A1h), M = 2 (register C0h) and N = 218 (registers C1h and C2h). K = 01 0011 1110 0010 1000 0001 (registers C3h to C5h).

Example 4: A non standard transmission link has a bit rate of 3012 Mbit/s and consequently fits in octave number 0, so M = 1. Suppose the reference frequency provided at pins CREF(Q) is 20.50 MHz. This means that the reference division R needs to be 1. The values of n and k can be calculated from the flowchart:

$$n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{3012\ \text{Mbits} \times 1 \times 1}{20.50\ \text{MHz}} = 146.9268293$$

This means that n = 146, k = 0.9268293 and bit RXNILFRAC should be logic 0 (register C3h). Since k is larger than 0.75, k needs to be corrected to 0.4268293 and N = 2 × n + 1 = 293. Consequently the appropriate values are: R = 1 (register A1h), M = 1 (register C0h) and N = 293 (registers C1h and C2h). K = 01 1011 0101 0001 0010 1011 (registers C3h to C5h).

If the I^2C-bus is not used, the DCR can be set up for the eight pre-programmed bit rates by pins DR0 to DR2 with an applied reference frequency of 19.44 MHz (see Table 3).

Reference clock programming

The reference clock, connected to pins CREF(Q), is used for both the DCR frequency window detector and the transmitter synthesizer. The reference clock is divided by divider R. Pre-programmed operating in an SDH/SONET application assumes the use of a reference clock with a frequency that is a multiple (R) of 19.44 MHz. For other applications, any reference frequency between 18 and 21 MHz may be used. If a reference frequency is selected, any bit rate between 30 Mbit/s and 3.2 Gbit/s is supported.

The division ratio and reference frequency can be programmed by the bits FREFI2C[2:0] of register REFDIV (A1h) or by pins FREF0 and FREF1. Internally, the reference frequency is always divided to the lowest frequency range between 18 and 21 MHz and for SDH/SONET applications to 19.44 MHz. This is done by divider R which is set by the described pins and bits.

In the pre-programmed mode (Table 6) four ranges of clock frequencies can be used by programming R through pins FREF0 and FREF1. In I²C-bus mode (Table 7) two additional ranges of clock frequencies can be used by programming R through bits FREFI2C[2:0].

Table 6 Truth table for reference divider R in pre-programmed mode

PIN		DIVISION FACTOR R	REFERENCE FREQUENCY	
FREF1	FREF0		SDH/SONET (MHz)	RANGE (MHz)
HIGH	HIGH	1	19.44	18 to 21
HIGH	LOW	2	38.88	36 to 42
LOW	HIGH	8	155.52	144 to 168
LOW	LOW	32	622.08	576 to 672

Table 7 Truth table for reference divider R in I²C-bus mode

BIT			DIVISION FACTOR R	REFERENCE FREQUENCY RANGE (MHz)
FREF I2C2	FREF I2C1	FREF I2C0		
0	0	0	1	18 to 21
0	0	1	2	36 to 42
0	1	0	4	72 to 84
0	1	1	8	144 to 168
1	0	0	16	288 to 336
1	0	1	32	576 to 672

Reference input

For optimum jitter performance and Power Supply Rejection Ratio (PSRR), the sensitive reference input should be driven differentially (see Fig.9). If the reference frequency source (f_{ref}) is single-ended, the unused CREF or CREFQ input should be terminated with an impedance which matches the source impedance R_{source}. The PSRR can be improved by AC coupling the reference frequency source to inputs CREF and CREFQ. Any low frequency noise injected from the f_{ref} power supply will be attenuated by the resulting high-pass filter. The low cut-off frequency of the AC coupling must be lower than the reference frequency, otherwise the reference signal will be attenuated and the signal to noise ratio will be reduced. The value of coupling capacitor C is calculated using the formula: $C > \frac{1}{2\pi R_{source} f_{ref}}$

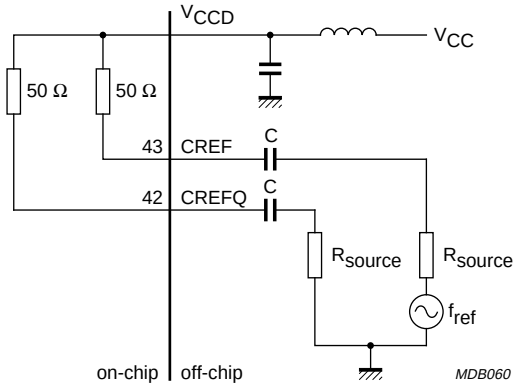


Fig.9 Reference input with single-ended clock source.

Prescaler outputs

The prescaler output RXPRSCL(Q) is the VCO frequency of the DCR divided by the main division factor N. It can be used as an accurate reference for another PLL, since it corresponds to the recovered data rate. If needed, the polarity of the prescaler outputs can be inverted by bit RXPRSCLINV of register DDR&RXPRSCL (D5h).

If no prescaler information is desired, the output can be disabled by bit RXPRSCLEN of the same register. Apart

from these settings, the signal amplitude can be set. This parameter follows the settings of the LVDS outputs. For programming details, see Section “LVDS outputs”.

FWD programming

The default width of the window for frequency acquisition is 1000 ppm around the required bit rate. This window size can be changed between 4000 and 250 ppm by bits WINSIZE[2:0] of register DCRCON (C6h). This allows for loose or tight coupling of the VCO to the applied reference clock. Another feature is to define a window width of 0 ppm, by means of pin WINSIZE, see Table 8. This effectively removes the dead zone from the FWD, rendering the FWD into a classical PLL.

The VCO will be directly locked to the reference signal instead of the incoming bit stream. Apart from pin WINSIZE, this mode can be invoked by bits I2CWINSIZE and WINSIZE of register DCRCON(C6h).

Table 8 Truth table for pin WINSIZE

WINSIZE	FREQUENCY WINDOW (ppm)
LOW	0
HIGH	1000

Accurate clock generation during loss of signal

A zero window size is especially interesting in the absence of input data, since the frequency of the ‘recovered clock’ will be equal to the programmed line clock rate.

Bit AUTOWIN of register DCRCON (C6h) (see Table 9) makes the window size dependent on the LOS status of the limiter. If the optical input signal is lost, the FWD automatically selects the 0 ppm window size; i.e. a direct lock to the reference frequency. This results in a stable and defined output clock during LOS situations, while automatically reverting back to normal DCR operating when the input signal returns.

The accuracy of the reference frequency needs to be better than 20 ppm if the application has to comply with ITU-T recommendations.

Table 9 Truth table for bit AUTOWIN

AUTOWIN	FREQUENCY WINDOW
0	FWD user defined
1	FWD dependent on LOS

INWINDOW output

The status of the FWD circuit is reflected in the state of pin INWINDOW; HIGH for an ‘in window’ situation and LOW whenever the VCO is outside the defined frequency window. Due to the fact that the device enters the frequency acquisition mode when out of window is detected, the INWINDOW pin will have an intermittent value when the input signal is not within the defined window boundary.

DEMULTIPLEXER

The demultiplexer converts the serial input bit stream to a parallel format. The output data is available on a 4-bit LVDS-bus, thus reducing the data frequency by a factor four. Apart from the de-serializing function, the demultiplexer comprises a parity calculator and a frame header detection circuit.

The calculated parity (even) is available at output pins RXPAR(Q), whereas occurrence of the frame header pattern in the data stream results in a one clock cycle (parallel clock output) wide pulse on output pins RXFP(Q).

If pin ENBA is HIGH, automatic byte (word) alignment takes place, formatting the parallel output to logical nibbles. Apart from pin ENBA, this mode can be invoked by bits I2CENBA and ENBA of register DMXCON (B8h).

To support most commonly used transmission protocols, the frame header pattern can be programmed to any 32-bit pattern (see Section “Frame detection”).

If required, the demultiplexer output can be forced into a fixed logic state by bit DMXMUTE of register DMXCON (B8h).

The highest supported parallel bus speed is 800 Mbit/s.

Frame detection

Byte alignment is enabled if the enable byte alignment input (pin ENBA) is forced HIGH. Whenever a 32-bit sequence matches the programmed header pattern, the incoming data is formatted into logical bytes (being output as nibbles) and a frame pulse is generated on differential output pins RXFP(Q). Any header pattern can be programmed through registers HEADER3 to HEADER0 (B0h to B3h). It is possible to enter a ‘don’t care’ for any bit position, e.g. to program a header pattern that is much shorter than 32 bits or to program a pattern with a gap in it.

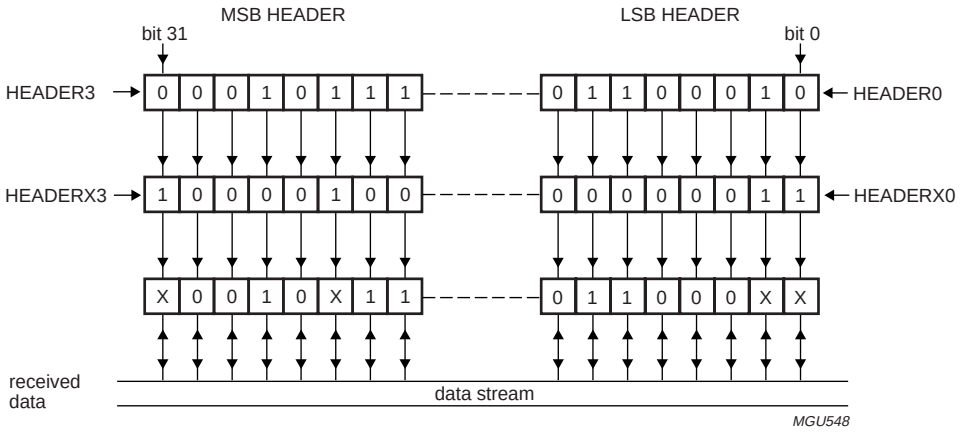


Fig.10 Example of programming the frame pattern (the symbol ‘X’ represents a don’t care).

For this, it is necessary to program registers HEADERX3 to HEADERX0 (B4h to B7h). Programming a logic 1 into the HEADERX register will turn the corresponding bit in the HEADER register into a don’t care bit, in this way the HEADER register is masked. An example of programming the framing pattern is shown in Fig.10.

The default frame header pattern is F6F62828h, corresponding to the middle section of the standard SDH/SONET frame header (the last two A1 bytes plus the first two A2 bytes).

If signal ENBA is LOW, no active alignment takes place. However, if the framing pattern happens to occur in the formatted data, a frame pulse will continue to be output on pins RXFP(Q).

Receiver framing in SDH/SONET applications

Figure 11 shows a typical SDH/SONET re-frame sequence involving byte alignment. Frame and byte boundary detection is enabled on the rising edge of ENBA and remains enabled while ENBA is HIGH. Boundaries are recognized on receipt of the second A2 byte and RXFP goes HIGH for one RXPC clock cycle.

The four most significant bits of the first A2 byte in the frame header are the first bits that appear on the outgoing data bus (RXPD0 to RXPD3) with the correct alignment.

When interfacing with a section terminating device, ENBA must remain HIGH for a full frame after the initial frame pulse. This is to allow the section terminating device to verify internally that frame and byte alignment are correct (see Fig.12). Byte boundary detection is disabled on the first RXFP pulse after ENBA has gone LOW.

Figure 13 shows frame and byte boundary detection activated on the rising edge of ENBA and deactivated by the first RXFP pulse after ENBA has gone LOW.

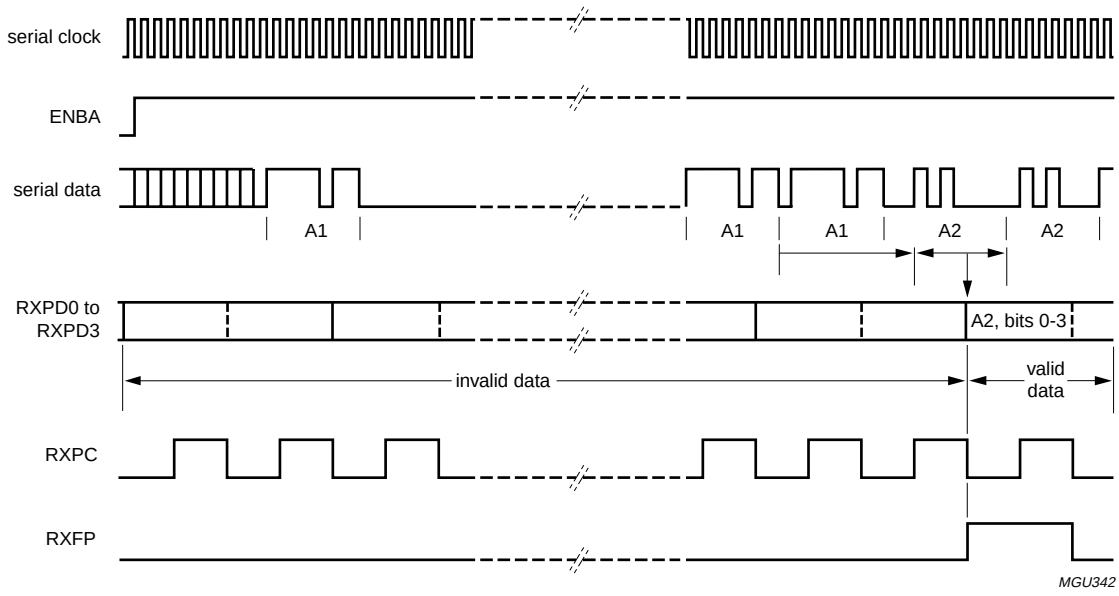


Fig.11 Frame and byte detection in SDH/SONET application.

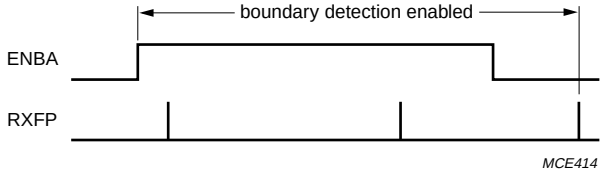


Fig.12 ENBA operating time with section terminating device.

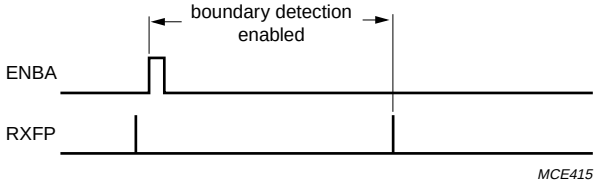


Fig.13 Alternate ENBA timing.

Receiver framing in other applications

In other applications frame headers may be used that are shorter than 32 bits, e.g. 10 bits for Gigabit Ethernet. The position of the frame header in the header register can be chosen freely, but determines the boundary of the parallel data on pins RXPD0(Q) to RXPD3(Q). After alignment, the header bits that are programmed by bits H12 to H15 of register HEADER1 (B2h), appear at the RXPD(Q) outputs. A frame pulse appears at output RXFP(Q) at the same time.

Parity generation

Outputs RXPAR(Q) provide the even parity of the nibble that is currently available on the parallel bus. With bit RXPARINV of register RXMFOUTC0 (D4h), the parity can be made odd. If no parity check is required, bit RXPAREN of register RXMFOUTC0 (D4h) can be programmed to disable this output, to reduce power dissipation.

Transmitter

CLOCK SYNTHESIZER

The transmitter frequency can be set independently of the receiver frequency. For this a clock synthesizer is provided that drives the multiplexer. Just like the DCR the clock synthesizer is built around a fractional N synthesizer offering A-rate functionality for the transmit path.

The clock synthesizer consists of a VCO, several dividers, a phase frequency detector, an integrated loop filter, a lock detection circuit and a prescaler output buffer (see Fig.14).

The internal VCO is phase-locked to the reference clock signal provided at pins CREF(Q). This frequency is internally scaled down (if necessary) to a frequency in the range of 18 to 21 MHz by divider R.

Because of the 22 bits fractional N capability, any combination of bit rate (30 Mbit/s to 3.2 Gbit/s) and reference frequency between 18 and 672 MHz is possible. The LSB (bit k0) of the fractional divider, should be set to logic 1 to avoid limit cycles. These are cycles of less than maximum length, which generate spurs in the frequency spectrum. This leaves bits k[21:1] available for programming the fraction, allowing approximately 10 Hz of frequency resolution without altering the reference frequency.

To meet most transmission standards, the reference frequency should be very accurate. In order to be able to synthesize a clean RF clock that is compliant with the most stringent jitter generation requirements, it should also be very clean in terms of phase noise.

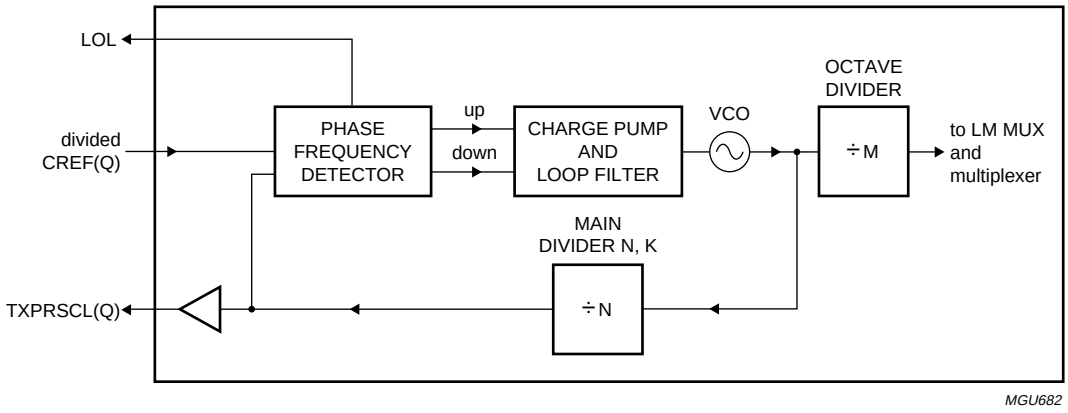


Fig.14 Schematic diagram of the clock synthesizer.

All parts of the PLL are internal; no external components are required. This allows for easy application.

Programming the clock synthesizer involves four dividers:

- Reference divider R
- Main divider N
- Fractional divider K
- Octave divider M.

This is essentially the same as for the DCR.

The first step is to determine in which octave the desired bit rate fits, see Tables 4 and 5 and Fig.7. Figure 7 shows the position of the most commonly used line rates in relation to the defined octaves of the TZA3015HW. Table 5 clarifies the octave definitions; this yields the value for the octave divider M. The value for R is determined by the reference frequency and the received bit rate (see Section “Reference clock programming”).

Prescaler output

The prescaler output TXPRSCL(Q) is the VCO frequency of the synthesizer divided by the main division factor N. If the synthesizer is in-lock, the frequency is equal to the reference frequency at CREF(Q) divided by R. It can be used as an accurate reference for another PLL. If needed, the polarity of the prescaler outputs can be inverted by bit TXPRSCLINV of register TXMFOUTC (F2h).

If no prescaler information is desired, the output can be disabled by bit TXPRSCLEN of the same register. Apart from these settings, the signal amplitude can be set. This parameter follows the settings of the LVDS outputs. For programming details, see Section “LVDS outputs”.

Loss of lock

During operating, the loss of lock output pin LOL should be LOW which means that the clock synthesizer is in-lock and the output frequency corresponds to the programmed value. If pin LOL goes HIGH, phase and/or frequency lock is lost and the output frequency may deviate from the programmed value. The LOL condition is also available in the registers INTERRUPT (00h) and STATUS (01h).

On demand (interrupt is default masked), it generates an interrupt signal at pin INT.

MULTIPLEXER

The multiplexer comprises a high-speed input register, a 4-stage First In First Out (FIFO) elastic buffer, a parity check circuit and the actual multiplexing tree.

Parallel bus clocking schemes

The TZA3015HW supports both co-directional and contra-directional clocking schemes for the parallel data bus. The clocking application can be selected by pin CLKDIR or by the bit CLKDIR of register MUXCON0 (F1h). Co-directional clocking is default.

Table 10 Truth table for clocking scheme

PIN CLKDIR	BIT CLKDIR	APPLICATION
LOW	0	contra-directional clocking
HIGH	1	co-directional clocking

In the co-directional clocking mode, the parallel clock signal is applied to pins TXPC(Q). The parallel clock signal is generated in the data processing device (e.g. a framer). The co-directional application is depicted in Fig.15. The data processing device may be clocked by an external crystal or by the parallel clock output TXPCO(Q) of the TZA3015HW. This clock output is internally derived from the synthesizer. If the parallel clock output TXPCO(Q) is not required, it can be disabled in order to save dissipation. This is done by programming bit TXPCOEN of register TXMFOUTC (F2h).

In a contra-directional clock application, no clock is provided on pin TXPC (see Fig.16). The clock that samples the input data on the parallel bus, is an internal clock derived from signal TXPCO. In this application, the part providing the parallel data has to be clocked with the clock signal TXPCO(Q). In order to alleviate timing problems, the phase of clock TXPCO(Q), with respect to the internal clock, can be shifted in 90° steps. Bit TXPCOINV (180°) of register TXMFOUTC (F2h) together with bit TXPOPHASE (90°) of register MUXCON0 (F1h) sets the phase shift (see Table 11).

Table 11 Truth table for bits TXPCINV and TXPOPHASE

TXPCOINV	TXPOPHASE	PHASE SHIFT
0	0	0°
0	1	90°
1	0	180°
1	1	270°

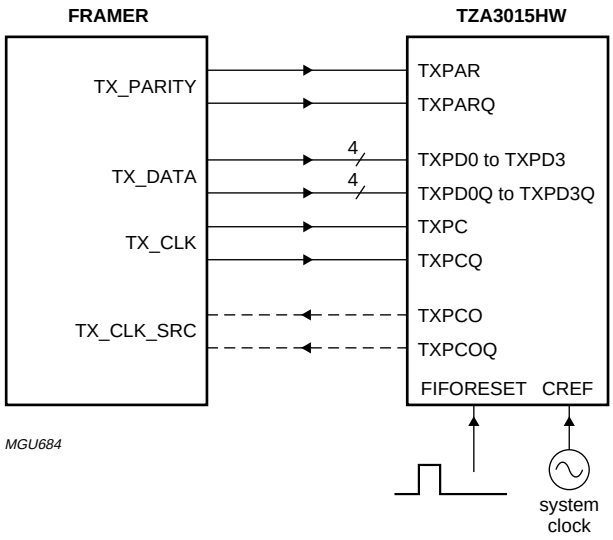


Fig.15 Co-directional clocking diagram.

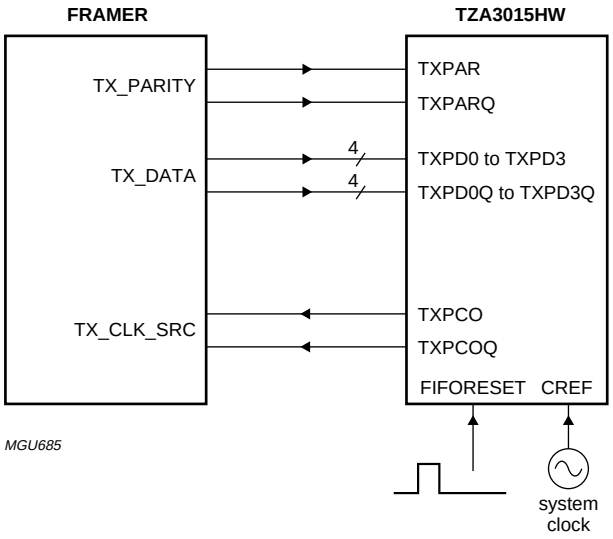


Fig.16 Contra-directional clocking diagram.

Double data rate mode

Usually the parallel clock frequency (TXPC, RXPC and TXPCO) equals the parallel data rate (for example when the serial bit rate is 2.488 Gbit/s, the parallel bit rate is 622 Mbit/s and the data is clocked with a 622 MHz clock). This is the default operating mode.

However, in some applications it is required to use a parallel clock operating at a frequency that is half of the parallel data rate. This is the DDR mode (for example when the serial bit rate is 2.488 Gbit/s, the parallel bit rate is 622 Mbit/s and the data is clocked at both the rising as well as the falling edge of the 311 MHz clock). The timing for the parallel input interface is in accordance with the SFI4 specification.

The DDR functionality can be enabled by pin ENDDR (see Table 12) or via the I^2C-bus. I^2C-bus control is enabled by setting bit I2CDDR of register DDR&RXPRSCL (D5h).

In I^2C-bus mode the three parallel clocks can be set separately in the DDR mode by bits RXPCDDREN, TXPCDDREN and TXPCODDREN of registers DDR&RXPRSCL (D5h), MUXCON0 (F1h) and TXMFOUTC (F2h) respectively (see Tables 13, 14 and 15).

The DDR mode is functional for the whole bit-rate range, so it is true A-rate.

Table 12 Truth table for pin ENDDR

ENDDR	MODE
LOW	TXPC, RXPC and TXPCO in normal mode
HIGH	TXPC, RXPC and TXPCO in DDR mode

Table 13 Truth table for bit RXPCDDREN

RXPCDDREN	MODE
1	RXPC in DDR mode
0	RXPC in normal mode

Table 14 Truth table for bit TXPCDDREN

TXPCDDREN	MODE
1	TXPC in DDR mode
0	TXPC in normal mode

Table 15 Truth table for bit TXPCODDREN

TXPCODDREN	MODE
1	TXPCO in DDR mode
0	TXPCO in normal mode

FIFO register

In the co-directional clocking scheme, the input register samples the parallel bus data on the rising edge of the clock signal TXPC(Q). The same clock writes this data into the FIFO register. Data is retrieved from the FIFO by an internal clock, derived from the clock generator of the actual multiplexing tree. This provides for large jitter tolerance on the parallel interface; the FIFO absorbs momentary phase disturbances. Excessively large phase disturbances may stretch the elastic buffer to its limits, causing a FIFO overflow or underflow. Pin OVERFLOW and the registers STATUS (01h) and INTERRUPT (00h) indicate this situation. On demand (i.e to programmed in the register INTMASK [A0h]) it generates an interrupt signal at pin INT.

The overflow alarm persists until the FIFO is reset by a HIGH-level on pin FIFORESET or by setting bit FIFORESET of register MUXCON0 (F1h) to logic 1. A FIFORESET also initializes the FIFO. I^2C-bus control of the FIFORESET function is obtained by programming bit I2CFIFORES of register MUXCON0 (F1h). To fully benefit from the FIFO, it should be reset whenever there has been a LOL condition, or when bit rates have changed.

The asynchronous signal FIFORESET is re-timed by the internal clock from the clock generator. Two clock cycles after signal FIFORESET has been made HIGH, the FIFO initializes. Two clock cycles after signal FIFORESET has been made LOW, the FIFO will be operational again. To initialize automatically, when an overflow has occurred, it is possible to connect pin OVERFLOW to pin FIFORESET directly or via a resistor.

Multiplexing bus swap

Bit TXBUSSWAP of register MUXCON1 (F0h) swaps the bus order of the parallel data input bus TXPD0(Q) to TXPD3(Q). Bit TXBUSSWAP reverses the order of bits from MSB to LSB, or vice versa, to allow for optimum connectivity on the PCB.

Parity checking

In order to check the integrity of the data provided on the parallel input bus, a parity checking function has been implemented in the TZA3015HW. The calculated parity, based on the data currently on the bus, is compared to the expected parity provided at pins TXPAR(Q). If these do not match, i.e. a parity error has occurred, the output pins TXPARERR(Q) are HIGH during the next parallel bus clock (TXPC) period.

Odd or even parity checking can be selected by pin PAREVEN or by bit TXPAREVEN of register MUXCON1 (F0h). I²C-bus control of the parity type is enabled by setting bit I2CTXPAREVEN of register MUXCON1 (F0h). A HIGH-level on pin PAREVEN corresponds with even parity (default for bit TXPAREVEN), see Table 16.

Table 16 Truth table for parity setting

PIN PAREVEN	BIT TXPAREVEN	PARITY TYPE
LOW	0	odd
HIGH	1	even

Jitter performance

The clock synthesizer has been optimized for lowest jitter generation and the data and clock recovery has been optimized for the best jitter tolerance. For all SDH/SONET line rates, the jitter tolerance and the jitter generation is compliant with ITU-T standard G.958, provided the reference clock is clean enough. For optimum jitter generation, the single-sideband phase noise of the reference frequency should be less than −140 dBc/Hz, for frequencies greater than 12 kHz from the carrier. If the reference divider R is used, this requirement elevates with approximately 20 × log R.

Configuring the main functionality

OPERATING MODES

The TZA3015HW can be configured in several operating modes. It can be configured as:

- Transceiver
- Transmitter
- Receiver
- Transponder with clean-up PLL.

The transceiver configuration is the default operating mode. The transmitter and receiver part can be enabled independently. This saves power when only one half of the functionality is needed. The TZA3015HW can also be configured as a clean-up PLL. This is described in the Section “Loop modes”. The operating modes can be selected with pins ENRX and ENTX, these pins enable the receiver and the transmitter. This also offers the possibility to power-down the complete IC. Operating (or enable) modes are listed in Table 17.

Table 17 Truth table for the operating modes

ENRX	ENTX	OPERATING MODE
LOW	LOW	power-down
LOW	HIGH	transmitter
HIGH	LOW	receiver
HIGH	HIGH	transceiver (or transponder)

LOOP MODES

The TZA3015HW supports four loop modes:

- Line loop back
- Diagnostic loop back
- Serial loop timing
- Clean-up loop back.

Selecting the loop modes

The required loop mode can be selected either by pins LM0, LM1 and LM2 or by I²C-bus control.

The pin settings for the loop mode selection can be seen in Table 18.

Table 18 Loop mode selection; note 1

LM2	LM1	LM0	MODE
LOW	LOW	LOW	normal
LOW	LOW	HIGH	line loop back
LOW	HIGH	LOW	diagnostic loop back
HIGH	LOW	HIGH	serial loop timing
HIGH	HIGH	LOW	clean-up loop back
HIGH	HIGH	HIGH	normal

Note

1. The loop mode can be also programmed by setting bits LM[2:0] in register LOOPMODE (A3h).

Line loop back mode

This mode feeds back the received serial data to the serial data output together with the recovered serial clock. This allows testing of the serial data path including the optic fibres. The received serial data that is fed back is also available in parallel format at the parallel output bus (see Fig.17).

Diagnostic loop back mode

This mode feeds back the parallel input data to the parallel outputs together with a parallel clock. The parallel data is serialized and available at the serial output. Also a serial transmit clock is generated. The parallel output clock signal is recovered from the serial output data. This loop mode is used to test the connection between the transceiver and the data processing unit and the system itself. No external fibre optic connection is needed to test the system (see Fig.18).

Serial loop timing mode

This mode feeds back the recovered clock to the clock synthesizer in order to run the receiver and transmitter at the same clock frequency (see Fig.19).

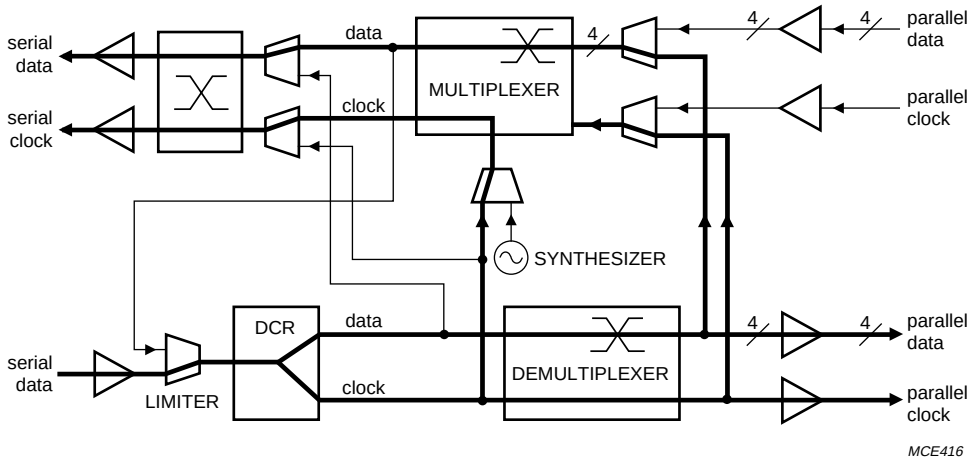


Fig.17 Line loop back mode.

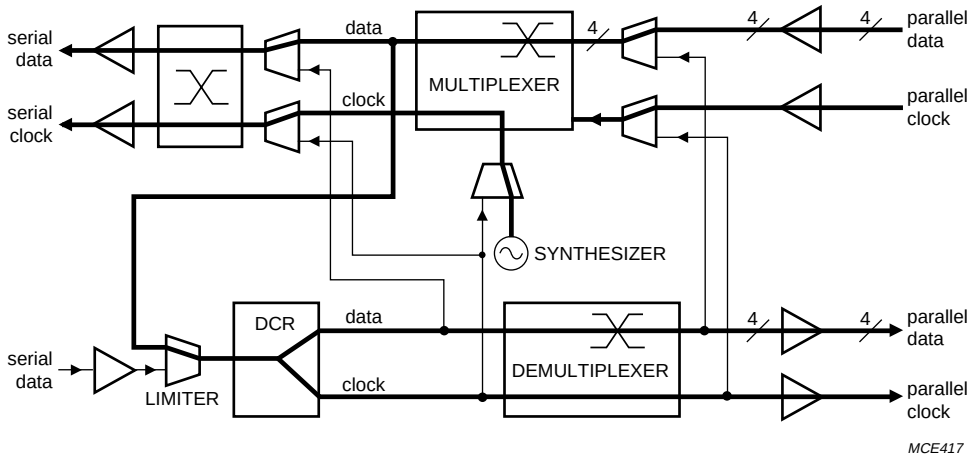


Fig.18 Diagnostic loop back mode.

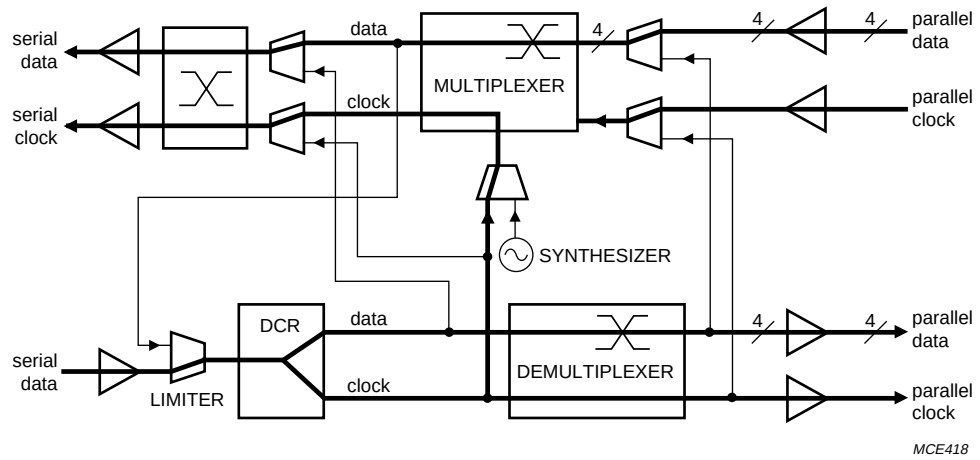


Fig.19 Serial loop timing mode.

Clean-up loop back mode

The TZA3015HW can be used in transponder applications. In this application, the transmitter is locked onto the recovered clock from the DCR (RXPRSCL). Without preparations, the jitter transfer of this application is determined by cascading the transfer functions of the DCR and the clock synthesizer. This transfer function is not well controlled and may not meet the required specification in terms of bandwidth and/or jitter peaking. A second drawback is that the jitter generation of the synthesizer is degraded because the frequency reference (i.e. the DCR) is not very clean in terms of phase-noise.

To improve both the jitter transfer and jitter generation in transponder applications, an external low-noise reference oscillator is locked onto the DCR recovered clock by means of a small band PLL, i.e. the clean-up PLL. The low-noise oscillator, e.g. a Voltage Controlled Crystal Oscillator (VCXO), acts as the reference for the clock synthesizer. If appropriately designed, the jitter will be dominated by the clean-up PLL. This PLL can be optimized for bandwidth and jitter peaking, while the jitter generation is optimized by choosing the appropriate VCXO.

Figure 20 shows a typical clean-up PLL application. For ease of use, all components are integrated in the TZA3015HW, except for the VCXO and the loop filter components. The PLL consists of a phase frequency detector, a charge pump, an external loop filter (R, C1 and C2), a VCXO and a reference divider. The combination of R and C1 is mandatory and will transform the current at the output of the charge pump into a control voltage for the VXCO. Capacitor C2 is optional.

The internal clock and data path in the TZA3015HW is clarified in Fig.21. As can be seen in the clean-up application, the received (and transmitted) data is also available in parallel format at the parallel output bus.

Two bits are available to ease the design of the clean-up PLL. The loop is designed to work with a VCXO that has a positive gain. That is an increasing voltage on the VCXO control input will increase the output frequency. By means of bit CLUPPLLINV of register REFDIV (A1h) the loop is inverted and will work with VCXOs which have a negative gain. Bit CLUPPLLHG of register REFDIV (A1h) will change the gain of the charge pump. If bit CLUPPLLHG is logic 0, the charge pump current I_{CP} is 100 μA. If bit CLUPPLLHG is logic 1, the charge pump current I_{CP} is 1 mA. This eases choosing suitable component values for R and C1.

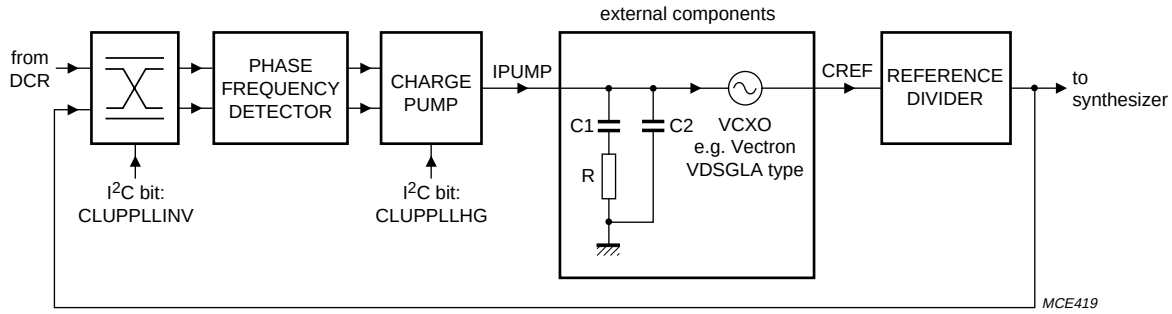


Fig.20 Clean-up PLL application with the TZA3015HW.

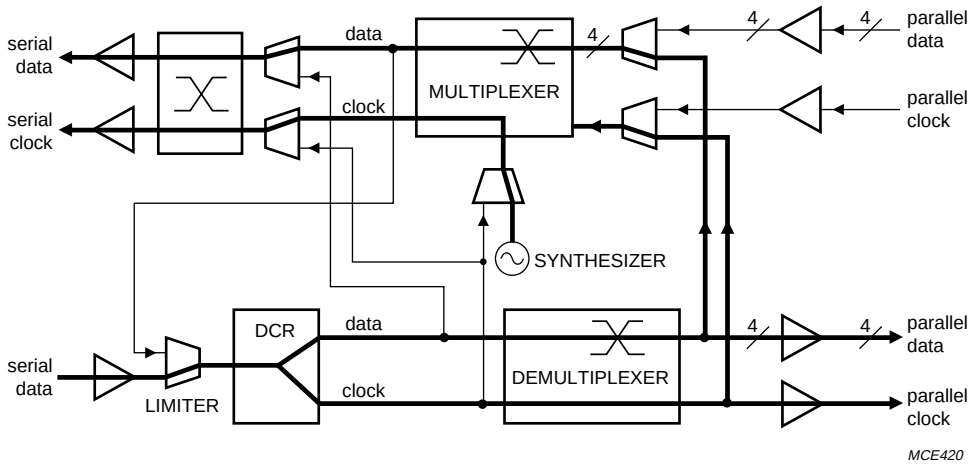


Fig.21 Clean-up loop back mode.

I/O configuration

LVDS OUTPUTS

Several options exist that allow flexible configuration of the LVDS outputs: output amplitude, signal polarity, bus order, mute and selective enable/disable of various outputs. All these options can be set in the registers MFOBCON (A4h), DMXCON (B8h), RXMFOUTC0 (D4h), DDR&RXPRSCL (D5h) and TXMFOUTC (F2h). Affected by these registers are:

- Parallel clock output; pins RXPC(Q)
- Parallel data output; pins RXPD0(Q) to RXPD3(Q)
- Frame pulse output; pins RXFP(Q)
- Parity output; pins RXPAR(Q)
- Parity error output; pins TXPARERR(Q)
- Transmitter parallel clock output; pins TXPCO(Q)
- Prescaler DCR output; pins RXPRSCL(Q)
- Prescaler synthesizer output; pins TXPRSCL(Q).

The output swing of all LVDS outputs can be set by pin LOWSWING or by programming bit LOWSWING in register MFOBCON (A4h). I²C-bus control is enabled by programming bit I2CLOWSWING in register MFOBCON (A4h). The typical voltage levels are given in Table 19. See also Figs 34 and 35.

Table 19 Truth table for pin LOWSWING

LOWSWING	LVDS OUTPUT VOLTAGE SWING
LOW	500 mV
HIGH	300 mV

Parallel clock output

Bit RXPCINV of register RXMFOUTC0 (D4h) sets the polarity of the parallel clock output RXPC(Q), effectively shifting the clock edge by half a clock cycle and changing the rising edge to a falling edge. This might resolve a parallel bus timing problem. The parallel clock output can be disabled by programming bit RXPCEN of register RXMFOUTC0 (D4h).

Parallel data output

The parallel output bus data RXPD0(Q) to RXPD3(Q) can be swapped by bit RXBUSSWAP of register DMXCON (B8h). The mute option forces the parallel output bits to a logic 0 state. This is done by programming bit DMXMUTE of register DMXCON (B8h). The polarity of the data RXPD0(Q) to RXPD3(Q) can be set by bit RXPDINV of register RXMFOUTC0 (D4h). The data outputs can be disabled by programming bit RXPDEN of register RXMFOUTC0 (D4h).

Frame pulse output

The polarity of the frame pulse output RXFP(Q) is set by bit RXFPINV of register RXMFOUTC0 (D4h). The frame pulse output can be disabled by programming bit RXFPEN of register RXMFOUTC0 (D4h).

Parity output

The polarity of the parity output RXPAR(Q) is set by bit RXPARINV of register RXMFOUTC0 (D4h). The parity output can be disabled by programming bit RXPAREN of register RXMFOUTC0 (D4h).

Parity error output

The polarity of the parity error output TXPARERR(Q) is set by bit TXPARERRINV of register TXMFOUTC (F2h). The parity error output can be disabled by programming bit TXPARERREN of register TXMFOUTC (F2h).

Transmitter parallel clock output

Bit TXPCOINV of register TXMFOUTC (F2h) sets the polarity of the parallel clock output TXPCO(Q), effectively shifting the clock edge by half a clock cycle and changing the rising edge to a falling edge. The phase of the clock can be shifted by 90° by programming bit TXPCOPHASE of register MUXCON0 (F1h). The combination of these two bits offers a phase shift range of 0 to 360°, adjustable in four steps (step size 90°). This might resolve a parallel bus timing problem. The parallel clock output can be disabled by programming bit TXPCOEN of register TXMFOUTC (F2h).

Prescaler DCR output

The polarity of the receiver prescaler output RXPRSCL(Q) is set by bit RXPRSCLINV of register DDR&RXPRSCL (D5h). The receiver prescaler output can be disabled by programming bit RXPRSCLEN of register DDR&RXPRSCL (D5h).

Prescaler synthesizer output

The polarity of the transmitter prescaler output TXPRSCL(Q) is set by bit TXPRSCLINV of register TXMFOUTC (F2h). The transmitter prescaler output can be disabled by programming bit TXPRSCLEN of register TXMFOUTC (F2h).

LVDS INPUTS

The available LVDS inputs are:

- Parallel clock input; pins TXPC(Q)
- Parallel data input; pins TXPD0(Q) to TXPD3(Q)
- Parity input; pins TXPAR(Q).

The differential LVDS inputs can handle any input swing with a minimum of 100 mV (p-p) single-ended. The inputs accept any value between V_{EE} and V_{CC}, i.e. the input buffers are true rail-to-rail. The limiting value of the LVDS input current is 25 mA. A differential hysteresis of 25 mV is implemented; see Fig.33.

Parallel clock input

Bit TXPCINV of register MUXCON1 (F0h) sets the polarity of the parallel clock input TXPC(Q), effectively shifting the clock edge by half a clock cycle and changing the rising edge to a falling edge. This could be used to resolve a parallel bus timing problem.

Parallel data input

The order of the parallel output bus data TXPD0(Q) to TXPD3(Q) can be programmed by bit TXBUSSWAP of register MUXCON1 (F0h).

Bit TXPDINV of register MUXCON1 (F0h) sets the polarity of the parallel data inputs TXPD0(Q) to TXPD3(Q).

RF OUTPUTS

The serial RF outputs are CML type outputs (see Figs 31 and 32). Several options exist that allow flexible configuration of the RF outputs: output amplitude adjustment, signal polarity, data-clock swap, output termination and selective enable/disable of the clock output. Thus, the TZA3015HW can be configured so that

connectivity problems with other ICs are avoided. Unused outputs can be disabled.

These options can be programmed in registers TXRFOUTC1 (F3h) and TXRFOUTC0 (F4h). The following RF outputs are available:

- Serial data output; pins TXSD(Q)
- Serial clock output; pins TXSC(Q).

The RF CML data and clock outputs have an adjustable signal amplitude between 70 and 1100 mV (p-p) single-ended in 16 steps. The amplitude can be programmed by setting bits RFS[3:0] of register TXRFOUTC0 (F4h). The default amplitude is 300 mV (p-p) single-ended.

The clock and data outputs can be swapped by programming bit TXSDSCSWAP of register TXRFOUTC1 (F3h). Allowing full flexibility in the PCB design.

The data and clock outputs can be DC- or AC-coupled to the laser driver. The TZA3015HW serial RF outputs can be adapted to this for optimal connectivity by appropriately setting bit RFOUTTERMAC of register TXRFOUTC0 (F4h). DC termination is default.

Serial clock output

The polarity of the serial clock output TXSC(Q) can be programmed by bit TXSCINV of register TXRFOUTC1 (F3h). The serial clock output can be disabled by setting pin ENTXSC or by programming bit TXSCEN of register TXRFOUTC1 (F3h) (see Table 20). This saves power dissipation in applications where the serial clock is not needed

Table 20 Truth table for serial clock enable

PIN ENTXSC	BIT ENTXSC	SERIAL CLOCK
LOW	0	disabled
HIGH	1	enabled

In order to control the enabling of the serial clock output by the I^2C-bus, bit I2CTXSCEN of register TXRFOUTC1 (F3h) must be programmed.

Serial data output

The polarity of the serial data output TXSD(Q) can be programmed by bit TXSDINV of register TXRFOUTC1 (F3h). The data output can be disabled by programming bit TXSDEN of register TXRFOUTC1 (F3h).

REFERENCE CLOCK INPUT

The reference clock CREF(Q) input is shown in Fig.36

RF INPUT

The serial data inputs are pins RXSD(Q). These pins are differential CML type serial RF data inputs. There are no special settings for these inputs.

CMOS OUTPUTS

The CMOS outputs are all used as logic outputs to indicate the status of the TZA3015HW.

- Loss of signal output; pin LOS
- Frequency window detector output; pin INWINDOW
- Interrupt output; pin INT
- Loss of lock output; pin LOL
- FIFO overflow alarm output; pin OVERFLOW.

A LOW state equals the ground potential and a HIGH state equals the supply voltage. The INT output can be configured as CMOS output or as open-drain output (see Sections “Open-drain output” and “Interrupt generation”). The output is configured as open-drain output by default.

CMOS INPUTS

The CMOS inputs are all used as logic inputs to configure the TZA3015HW:

- User interface selection input; pin UI
- Data rate selection inputs; pins DR0 to DR2
- Loop mode selection inputs; pins LM0 to LM2
- Enable receiver input; pin ENRX
- Enable transmitter input; pin ENTX
- Wide and narrow frequency detect window selection input; pin WINSIZE
- Enable low LVDS swing output input; pin LOWSWING
- Reference frequency selection inputs; pins FREF0 and FREF1
- Enable byte alignment input; pin ENBA
- FIFO reset input; pin FIFORESET
- Odd or even parity check input; pin PAREVEN
- Co-directional or contra-directional clocking selection input; pin CLKDIR
- Enable serial clock input; pin ENTXSC.

The CMOS inputs have an internal pull-up resistance; if the input is left open, a logic HIGH state will be forced internally. In the pre-programmed mode (UI = LOW), pins DR0 to 2 act as regular CMOS inputs. In the I²C-bus mode (UI = HIGH), pins SCL and SDA comply with the I²C-bus interface standard.

OPEN-DRAIN OUTPUT

The TZA3015HW contains one open-drain interrupt output pin INT. The output type of the interrupt controller can be configured by programming bit INTOUT of register INTCONF (A5h). The output can be configured as a push-pull CMOS output or as an open-drain output. For the open-drain configuration an external pull-up resistor of 3.3 kΩ is recommended. The polarity can be set by programming bit INTPOL of register INTCONF (A5h).

INTERRUPT GENERATION

The TZA3015HW features a fully configurable interrupt generator. An interrupt signal can be generated in the following events:

- Loss Of Signal (LOS)
- INWINDOW
- Temperature alarm
- Loss Of Lock (LOL)
- FIFO overflow or underflow.

The aforementioned events generate flags which can be read in register STATUS (01h). Each of these flags will generate an interrupt in the INTERRUPT register (00h). If programmed so in the register INTMASK (A0h) the INTERRUPT register bit(s) will generate an interrupt on pin INT. In this mask register each interrupt bit can be masked by writing a logic 0 in the corresponding bit position.

The STATUS register shows the present status of the receiver. The INTERRUPT register shows the history of the interrupts and is not affected by the INTMASK register.

Bit INTOUT of register INTCONF (A5h) determines the output type of pin INT: standard CMOS output or open-drain output. The latter is the default which provides for multiple receivers sharing a common interrupt signal wire with a 3.3 kΩ pull-up resistor (INT is active LOW in this case). The polarity can be set by programming bit INTPOL of register INTCONF (A5h).

The interrupt and status register can be polled by an I²C-bus read action. After the read action on the interrupt register the interrupt register is reset by clearing the interrupt bits where the ‘alarm’ is no longer present. If the ‘alarm’ is still set, the interrupt bit is not cleared after the read action. If an interrupt bit remains set (and if it is not masked) the INT pin will keep its interrupt condition active; it will not generate a pulse nor a spike. The I²C-bus status register is not reset since it always shows the present status of the receiver. It is important to note that the three reserved bits of the STATUS and INTERRUPT registers can take any value and that they can change during operating. These bits can not be used to obtain information on the status of the IC.

Power supply connections

Four separate supply domains (V_{DD}, V_{CCD}, V_{CCO} and V_{CCA}) provide isolation between the various functional blocks. Each supply domain should be connected to a common V_{CC} via separate filters. All supply domains should be powered synchronously.

All supply pins, including the exposed die pad, must be connected. The die pad should be connected with the lowest inductance possible. Since the die pad is also used as the main ground return of the chip, the connection should have a low DC impedance as well. The voltage supply levels should be in accordance with the values specified in Chapter “Characteristics”.

All external components should be surface mounted devices, preferably of size 0603 or smaller. The components must be mounted as closely to the IC as possible.

I²C-BUS

I²C-bus characteristics

The I²C-bus is a 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Data transfer may be initiated only when the line is not busy.

START AND STOP CONDITIONS

Figure 22 shows the definition of the start and stop conditions. Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

ACKNOWLEDGE

Figure 23 shows the definition of an acknowledgement on the I²C-bus. Only one data byte is transferred between the start and stop conditions during a write from the transmitter to the receiver. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the **last byte** that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

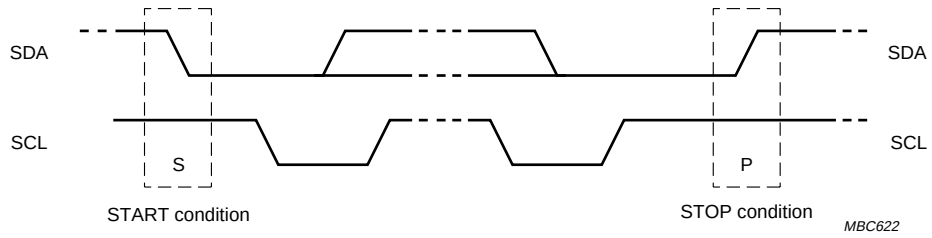


Fig.22 Start and stop conditions.

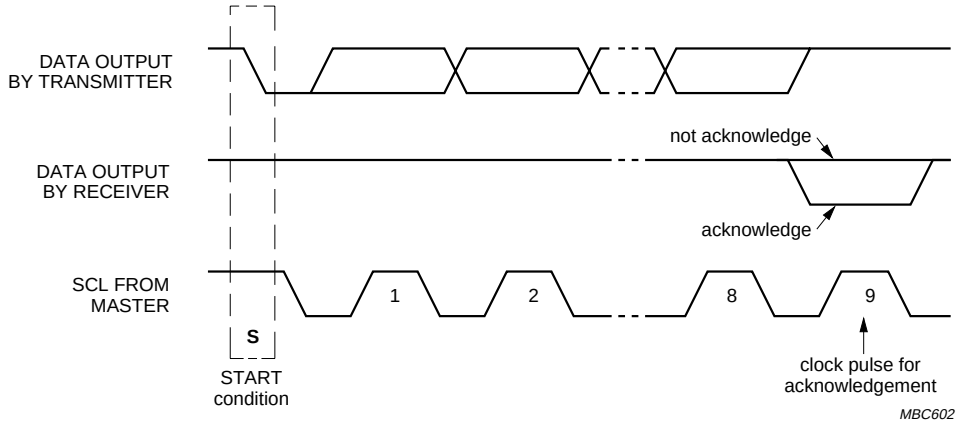


Fig.23 (Not) acknowledge condition on the I²C-bus.

I²C-bus protocol

Figure 24 shows the definition of the bytes. If bit R/$\overline{W}$ = 1 the master reads from the read register, if bit R/$\overline{W}$ = 0 the master writes to the write register. It is not possible to write and read the same register.

WRITE PROTOCOL

Figure 25 shows the protocol for writing to one single register. After the start command (S) the transmitter sends the address of the slave device, waits for an acknowledge from the slave, sends the register address, waits for an acknowledge, sends data, waits for an acknowledge from the master followed by a stop condition (P).

READ PROTOCOL

Figure 26 shows the protocol for reading from one or more registers.

After the start command (S) the receiver sends the address of the slave device, waits for an acknowledge from the transmitter slave, receives data from the slave (slave, TZA3015HW, starts sending data after generating the acknowledge), after receiving the data, the receiver (master) sends an acknowledge, or if finished a not-acknowledge followed by a stop condition (P).

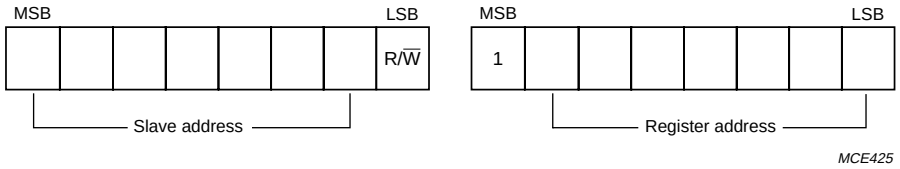


Fig.24 Definition of slave- and register address (= instruction byte); slave and register addresses are 7 bits.

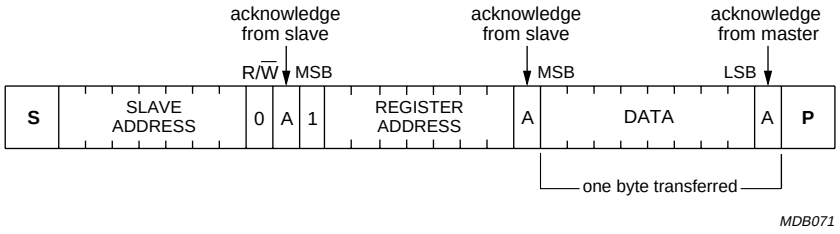
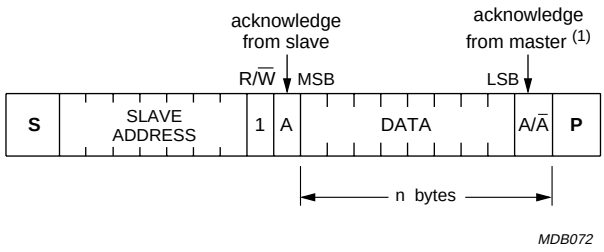


Fig.25 Write protocol.



(1) The master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave.

Fig.26 Read protocol.

I²C-BUS REGISTERS

The TZA3015HW can be programmed via the I²C-bus if pin UI = HIGH or leaving the pin open-circuit. The I²C-bus registers can be accessed via the 2-wire I²C-bus interface using pins SCL and SDA if pin CS = HIGH during read or write actions. The I²C-bus address of the TZA3015HW can be found in Table 2.

Table 21 I²C-bus registers

ADDRESS (HEX)	NAME	FUNCTION	DEFAULT	RANGE	R/W
General part					
00	INTERRUPT	interrupt register (see Table 22)	XXXX XXXX	n.a.	R
01	STATUS	status register (see Table 23)	XXXX XXXX	n.a.	R
A0	INTMASK	interrupt mask register (see Table 24)	0000 0100	n.a.	W
A1	REFDIV	reference divider and clean-up PLL (see Table 25)	0000 0000	n.a.	W
A3	LOOPMODE	loop mode and enable register (see Table 26)	0110 0111	n.a.	W
A4	MFOBCON	LVDS output buffer configuration (see Table 27)	0101 0000	n.a.	W
A5	INTCONF	interrupt output configuration (see Table 28)	0000 0001	n.a.	W
Transceiver					
B0	HEADER3	programmable header; MSB (see Table 29)	1111 0110	n.a.	W
B1	HEADER2	programmable header (see Table 30)	1111 0110	n.a.	W
B2	HEADER1	programmable header (see Table 31)	0010 1000	n.a.	W
B3	HEADER0	programmable header; LSB (see Table 32)	0010 1000	n.a.	W
B4	HEADERX3	programmable header don't care; MSB (see Table 33)	0000 0000	n.a.	W
B5	HEADERX2	programmable header don't care (see Table 34)	0000 0000	n.a.	W
B6	HEADERX1	programmable header don't care (see Table 35)	0000 0000	n.a.	W
B7	HEADERX0	programmable header don't care; LSB (see Table 36)	0000 0000	n.a.	W
B8	DMXCON	demultiplexer configuration register (see Table 37)	0000 0000	n.a.	W
C0	RXOCTDIV	DCR octave M divider (see Table 38)	0000 0000	n.a.	W
C1	RXMAINDIV1	VCO frequency N divider (see Table 39)	0000 0001	128 to 511	W
C2	RXMAINDIV0	VCO frequency N divider (see Table 40)	0000 0000	128 to 511	W
C3	RXFRACN2	fractional division (see Table 41)	1000 0000	n.a.	W
C4	RXFRACN1	fractional division (see Table 42)	0000 0000	n.a.	W
C5	RXFRACN0	fractional division (see Table 43)	0000 0000	n.a.	W
C6	DCRCON	DCR configuration register (see Table 44)	0000 1100	n.a.	W
D0	LIMLOSTH	limiter loss threshold	0000 0000	0 to 255	W
D1	LIMLOSCON	limiter loss of signal configuration register (see Table 45)	0000 1101	n.a.	W
D2	LIMSL	limiter slice level	0000 0000	0 to 255	W
D3	LIMCON	limiter amplifier configuration (see Table 46)	0000 0000	n.a.	W
D4	RXMFOUTC0	disable/invert parallel outputs (see Table 47)	1010 1010	n.a.	W

ADDRESS (HEX)	NAME	FUNCTION	DEFAULT	RANGE	R/W
D5	DDR&RXPRSCL	disable/invert parallel outputs (see Table 48)	0010 0000	n.a.	W
Transmitter part					
E0	TXOCTDIV	synthesizer octave divider (see Table 49)	0000 0000	n.a.	W
E1	TXMAINDIV1	VCO frequency (N divider) (see Table 50)	0000 0001	128 to 255	W
E2	TXMAINDIV 0	VCO frequency (N divider) (see Table 51)	0000 0000	128 to 255	W
E3	TXFRACN2	fractional division (see Table 52)	1000 0000	n.a.	W
E4	TXFRACN1	fractional division (see Table 53)	0000 0000	n.a.	W
E5	TXFRACN0	fractional division (see Table 54)	0000 0000	n.a.	W
F0	MUXCON1	multiplexer configuration byte 1 (see Table 55)	0110 0010	n.a.	W
F1	MUXCON0	multiplexer configuration byte 0 (see Table 56)	0000 0010	n.a.	W
F2	TXMFOUTC	disable/invert LVDS outputs (see Table 57)	1010 1000	n.a.	W
F3	TXRFOUTC1	disable/invert RF outputs (see Table 58)	0100 1011	n.a.	W
F4	TXRFOUTC0	RF output configuration register (see Table 59)	0000 0011	n.a.	W

Table 22 Register INTERRUPT (address: 00h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								loss of signal	LOS
							1	no signal present	
							0	signal present	
								INWINDOW	INWINDOW
						1		frequency out of window	
						0		frequency in window	
								temperature alarm	TALARM
					1			junction temperature ≥130 °C	
					0			junction temperature <130 °C	
								loss of lock	LOL
				1				synthesizer out of lock	
				0				synthesizer out of lock	
	x	x	x						reserved
								FIFO overflow or underflow	OVERFLOW
1								FIFO overflow or underflow occurred	
0								FIFO normal operating	

Table 23 Register STATUS (address: 01h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								loss of signal	LOS
							1	no signal present	
							0	signal present	
								INWINDOW	INWINDOW
						1		frequency out of window	
						0		frequency in window	
								temperature alarm	TALARM
					1			junction temperature ≥130 °C	
					0			junction temperature <130 °C	
								loss of lock	LOL
				1				synthesizer out of lock	
				0				synthesizer out of lock	
	x	x	x						reserved
								FIFO over- or underflow	OVERFLOW
1								FIFO under- or underflow occurred	
0								FIFO normal operating	

Table 24 Register INTMASK (address: A0h, default value: 04h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								mask LOS signal	MLOS
							1	not masked	
							0	masked; note 1	
								mask INWINDOW signal	MINWINDOW
						1		not masked	
						0		masked; note 1	
								mask temperature alarm	MTALARM
					1			not masked	
					0			masked; note 1	
								mask LOL signal	MLOL
				1				not masked	
				0				masked; note 1	
	x	x	x						reserved
								mask FIFO overflow or underflow	MOVERFLOW
1								not masked	
0								masked; note 1	
0	0	0	0	0	1	0	0		default value

Note to Table 24

1. Signal is not processed by the interrupt controller.

Table 25 Register REFDIV (address: A1h, default value: 00h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								reference frequency division ratio divider R; octave selection	FREFI2C[2:0]
					0	0	0	R = 1	
					0	0	1	R = 2	
					0	1	0	R = 4	
					0	1	1	R = 8	
					1	0	0	R = 16	
					1	0	1	R = 32	
								reference frequency division programming by I^2C-bus	I2CFREF
				1				enable I^2C-bus programming	
				0				enable programming by pins	
			x						reserved
								high gain clean-up PLL	CLUPPLLHG
		1						enable high gain	
		0						normal gain	
								invert charge pump currents of the clean-up PLL	CLUPPLLINV
	1							clean-up PLL inverted	
	0							clean-up PLL normal operating	
								enable clean-up PLL	CLUPPLLEN
1								clean-up PLL enabled	
0								clean-up PLL disabled (except in clean-up loop back mode)	
0	0	0	0	0	0	0	0		default value

Table 26 Register LOOPMODE (address: A3h, default value: 67h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								loop mode selection	LM[2:0]
					0	0	0	normal mode	
					0	0	1	line loop back mode	
					0	1	0	diagnostic loop back mode	
					0	1	1	reserved	
					1	0	0	reserved	
					1	0	1	serial loop timing mode	
					1	1	0	clean-up loop back mode	
					1	1	1	normal mode	

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
				1 0				loop mode programming by I²C-bus enable I²C-bus programming enable programming by pins	I2CLM
			x						reserved
		1 0						enable receiver receiver enabled receiver disabled	ENRX
	1 0							enable transmitter transmitter enabled transmitter disabled	ENTX
1 0								transmitter/receiver enable by I²C-bus enable I²C-bus programming enable programming by pins	I2CENTRX
0	1	1	0	0	1	1	1		default value

Table 27 Register MFOBCON (address: A4h, default value: 50h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
		x	x	x	x	x	x		reserved
	1 0							parallel output voltage swing low swing (300 mV) high swing (500 mV)	LOWSWING
1 0								parallel output voltage swing programming by I²C-bus enable I²C-bus programming enable programming by pins	I2CLOWSWING
0	1	0	1	0	0	0	0		default value

Table 28 Register INTCONF (address: A5h, default value: 01h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
							1 0	interrupt output polarity inverted normal operating	INTPOL
						1 0		interrupt output configuration push-pull output open drain output	INTOUT
x	x	x	x	x	x				reserved
0	0	0	0	0	0	0	1		default value

Table 29 Register HEADER3 (address: B0h, default value: F6h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
x	x	x	x	x	x	x	x	programmable header; H31 = MSB	H[31:24]
1	1	1	1	0	1	1	0		default value

Table 30 Register HEADER2 (address: B1h, default value: F6h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
x	x	x	x	x	x	x	x	programmable header	H[23:16]
1	1	1	1	0	1	1	0		default value

Table 31 Register HEADER1 (address: B2h, default value: 28h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
x	x	x	x	x	x	x	x	programmable header	H[15:08]
0	0	1	0	1	0	0	0		default value

Table 32 Register HEADER0 (address: B3h, default value: 28h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
x	x	x	x	x	x	x	x	programmable header; H00 = LSB	H[07:00]
0	0	1	0	1	0	0	0		default value

Table 33 Register HEADERX3 (address: B4h, default value: 00h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
x	x	x	x	x	x	x	x	don’t care; HX31 = MSB	HX[31:24]
0	0	0	0	0	0	0	0		default value

Table 34 Register HEADERX2 (address: B5h, default value: 00h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
x	x	x	x	x	x	x	x	don’t care	HX[23:16]
0	0	0	0	0	0	0	0		default value

Table 35 Register HEADERX1 (address: B6h, default value: 00h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
x	x	x	x	x	x	x	x	don't care	HX[15:08]
0	0	0	0	0	0	0	0		default value

Table 36 Register HEADERX0 (address: B7h, default value: 00h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
x	x	x	x	x	x	x	x	don't care; HX00 = LSB	HX[07:00]
0	0	0	0	0	0	0	0		default value

Table 37 Register DMXCON (address: B8h, default value: 00h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
				x	x	x	x		reserved
			1 0					parallel bus swapping RXPD0 = MSB; RXPD3 = LSB (swapped) RXPD3 = MSB; RXPD0 = LSB (normal)	RXBUSSWAP
		1 0						mute parallel outputs enable mute; parallel outputs forced to logic 0 disable mute	DMXMUTE
	1 0							enable byte alignment byte alignment enabled byte alignment disabled	ENBA
1 0								ENBA programming by I^2C-bus enable I^2C-bus programming enable programming by pins	I2CENBA
0	0	0	0	0	0	0	0		default value

Table 38 Register RXOCTDIV (address: C0h, default value: 00h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								division ratio octave divider M; octave selection	RXDIV_M[2:0]
					0	0	0	M = 1; octave number 0	
					0	0	1	M = 2; octave number 1	
					0	1	0	M = 4; octave number 2	
					0	1	1	M = 8; octave number 3	
					1	0	0	M = 16; octave number 4	
					1	0	1	M = 32; octave number 5	
					1	1	0	M = 64; octave number 6	
x	x	x	x	x					reserved
0	0	0	0	0	0	0	0		default value

Table 39 Register RXMAINDIV1 (address: C1h, default value: 01h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
							x	division ratio divider N; RXN8 = MSB	RXN8
x	x	x	x	x	x	x			reserved
0	0	0	0	0	0	0	1		default value

Table 40 Register RXMAINDIV0 (address: C2h, default value: 00h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
x	x	x	x	x	x	x	x	division ratio divider N; RXN0 = LSB	RXN[7:0]
0	0	0	0	0	0	0	0		default value

Table 41 Register RXFRACN2 (address: C3h, default value: 80h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
		x	x	x	x	x	x	fractional divider; RXK21 = MSB	RXK[21:16]
	x								reserved
1 0								RXNILFRAC control bit (NF) no fractional N functionality fractional N functionality	RXNILFRAC
1	0	0	0	0	0	0	0		default value

Table 42 Register RXFRACN1 (address: C4h, default value: 00h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
x	x	x	x	x	x	x	x	fractional divider	RXK[15:8]
0	0	0	0	0	0	0	0		default value

Table 43 Register RXFRACN0 (address: C5h, default value: 00h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
x	x	x	x	x	x	x	x	fractional divider; RXK0 = LSB	RXK[7:0]
0	0	0	0	0	0	0	0		default value

Table 44 Register DCRCON (address: C6h, default value: 0Ch)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								frequency window size; relative to bit rate	WINSIZE[2:0]
					0	1	1	2000 ppm	
					1	0	0	1000 ppm	
					1	0	1	500 ppm	
					1	1	0	250 ppm	
								manual frequency window size selection	WINSIZE
				1				window size according to bits WINSIZE[2:0] (default value 1000 ppm); PLL frequency loosely coupled to reference crystal	
				0				window size is 0 ppm; PLL frequency directly synthesized from reference crystal	
								WINSIZE control bit	I2CWINSIZE
			1					through I^2C-bus interface	
			0					through external pin WINSIZE	
								automatic frequency window size selection	AUTOWIN
		1						enabled	
		0						disabled	
x	x								reserved
0	0	0	0	1	1	0	0		default value

Table 45 Register LIMLOSCON (address: D1h, default value: 0Dh)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								enable loss of signal detection	LOSEN
							1	LOS detection enabled	
							0	LOS detection disabled	

BIT								PARAMETER	
7	6	5	4	3	2	1	0	DESCRIPTION	NAME
								LOS threshold level programming by I²C-bus	I2CLOSTH
						1		enable I²C-bus programming; set level by register D0h	
						0		set level by applying analog reference voltage on pin LOSTH	
								loss of signal detection hysteresis	HTLCB[2:0]
			0	0	0			0 dB	
			0	0	1			1 dB	
			0	1	0			2 dB	
			0	1	1			3 dB	
			1	0	0			4 dB	
			1	0	1			5 dB	
			1	1	0			6 dB	
			1	1	1			7 dB	
								enable slice level	SLEN
		1						slice level enabled	
		0						slice level disabled	
								slice level sign	SLSGN
	1							positive slice level	
	0							negative slice level	
								LOS level polarity	LOSPOL
1								inverted polarity	
0								normal polarity	
0	0	0	0	1	1	0	1		default value

Table 46 Register LIMCON (address: D3h, default value: 00h)

BIT								PARAMETER	
7	6	5	4	3	2	1	0	DESCRIPTION	NAME
								amplifier octave selection	AMP[2:0]
					0	0	0	octave number 0; 1800 to 3200 Mbit/s	
					0	0	1	octave number 1; 900 to 1800 Mbit/s	
					0	1	0	octave number 2; 450 to 900 Mbit/s	
					0	1	1	octave number 3; 225 to 450 Mbit/s	
					1	X	X	octave number 4; 30 to 225 Mbit/s	
x	x	x	x	x					reserved
0	0	0	0	0	0	0	0		default value

Table 47 Register RXMFOUTC0 (address: D4h, default value: AAh)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								parallel data output polarity	RXPDINV
							1	inverted	
							0	normal	
								parallel data output enable	RXPDEN
						1		enabled	
						0		disabled	
								parallel clock output polarity	RXPCINV
					1			inverted	
					0			normal	
								parallel clock output enable	RXPCEN
				1				enabled	
				0				disabled	
								parity output polarity	RXPARINV
			1					inverted	
			0					normal	
								parity output enable	RXPAREN
		1						enabled	
		0						disabled	
								frame pulse output polarity	RXFPINV
	1							inverted	
	0							normal	
								frame pulse output enable	RXFPEN
1								enabled	
0								disabled	
1	0	1	0	1	0	1	0		default value

Table 48 Register DDR&RXPRSCL (address: D5h, default value: 20h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
				x	x	x	x		reserved
								invert RX prescaler output	RXPRSCLINV
			1					inverted	
			0					normal	
								enable RX prescaler output	RXPRSCLEN
		1						enabled	
		0						disabled	

BIT								PARAMETER	
7	6	5	4	3	2	1	0	DESCRIPTION	NAME
								DDR clock frequency mode for RXPC	RXPCDDREN
	1							DDR mode enabled	
	0							normal operating mode	
								DDR programming by I2C-bus	I2CDDR
1								enable I2C-bus programming	
0								enable programming by pin ENDDR	
0	0	1	0	0	0	0	0		default value

Table 49 Register TXOCTDIV (address: E0h, default value: 00h)

BIT								PARAMETER	
7	6	5	4	3	2	1	0	DESCRIPTION	NAME
								division ratio octave divider M; octave selection	TXDIV_M[2:0]
					0	0	0	M = 1; octave number 0	
					0	0	1	M = 2; octave number 1	
					0	1	0	M = 4; octave number 2	
					0	1	1	M = 8; octave number 3	
					1	0	0	M = 16; octave number 4	
					1	0	1	M = 32; octave number 5	
					1	1	0	M = 64; octave number 6	
x	x	x	x	x					reserved
0	0	0	0	0	0	0	0		default value

Table 50 Register TXMAINDIV1 (address: E1h, default value: 01h)

BIT								PARAMETER	
7	6	5	4	3	2	1	0	DESCRIPTION	NAME
							x	division ratio divider N; TXN8 = MSB	TXN8
x	x	x	x	x	x	x			reserved
0	0	0	0	0	0	0	1		default value

Table 51 Register TXMAINDIV0 (address: E2h, default value: 00h)

BIT								PARAMETER	
7	6	5	4	3	2	1	0	DESCRIPTION	NAME
x	x	x	x	x	x	x	x	division ratio divider N; TXN0 = LSB	TXN[7:0]
0	0	0	0	0	0	0	0		default value

Table 52 Register TXFRACN2 (address: E3h, default value: 80h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
		x	x	x	x	x	x	fractional divider: TXK21 = MSB	TXK[21:16]
	x								reserved
1 0								TXNILFRAC control bit (NF) no fractional N functionality fractional N functionality	TXNILFRAC
1	0	0	0	0	0	0	0		default value

Table 53 Register TXFRACN1 (address: E4h, default value: 00h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
x	x	x	x	x	x	x	x	fractional divider	TXK[15:8]
0	0	0	0	0	0	0	0		default value

Table 54 Register TXFRACN0 (address: E5h, default value: 00h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
x	x	x	x	x	x	x	x	fractional divider; TXK0 = LSB	TXK[7:0]
0	0	0	0	0	0	0	0		default value

Table 55 Register MUXCON1 (address: F0h, default value: 62h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
							1 0	parallel INPUT bus swapping TXPD0 = MSB; TXPD3 = LSB (swapped) TXPD3 = MSB; TXPD0 = LSB (normal)	TXBUSSWAP
						1 0		parity polarity even parity odd parity	TXPAREVEN
					1 0			parity programming by I^2C-bus by I^2C-bus interface by external pin PAREVEN	I2CTXPAREVEN
				1 0				parallel clock input polarity inverted normal	TXPCINV

BIT								PARAMETER	
7	6	5	4	3	2	1	0	DESCRIPTION	NAME
			1 0					parallel data input polarity inverted normal	TXPDINV
x	x	x							reserved
0	1	1	0	0	0	1	0		default value

Table 56 Register MUXCON0 (address: F1h, default value: 02h)

BIT								PARAMETER	
7	6	5	4	3	2	1	0	DESCRIPTION	NAME
							1 0	parallel clock output phase 90° phase shift 0° phase shift	TXPCOPHASE
						1 0		parallel clock direction co-directional clocking contra-directional clocking	CLKDIR
					1 0			parallel clock direction programming I^2C-bus by I^2C-bus interface by external pin CLKDIR	I2CLKDIR
				1 0				FIFO reset reset FIFO normal mode	FIFORESET
			1 0					FIFO reset programming by I^2C-bus by I^2C-bus interface by external pin FIFORESET	I2CFIFORES
		1 0						DDR clock frequency mode for TXPC DDR mode enabled normal mode	TXPCDDREN
x	x								reserved
0	0	0	0	0	0	1	0		default value

Table 57 Register TXMFOUTC (address: F2h, default value: A8h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
							x		reserved
						1 0		DDR clock frequency mode for TXPCO DDR mode enabled normal mode	TXPCODDREN
					1 0			parallel clock output polarity inverted normal	TXPCOINV
				1 0				parallel clock output enable enabled disabled	TXPCOEN
			1 0					prescaler output polarity inverted normal	TXPRSCLINV
		1 0						prescaler output enable enabled disabled	TXPRSCLEN
	1 0							parity error output polarity inverted normal	TXPARERRINV
1 0								parity error output enable enabled disabled	TXPARERREN
1	0	1	0	1	0	0	0		default value

Table 58 Register TXRFOUTC1 (address: F3h, default value: 4Bh)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
						x	x		reserved
					1 0			serial output data polarity inverted normal	TXSDINV
				1 0				enable serial data output enabled disabled	TXSDEN
			1 0					clock and data output swap swapped clock and data output normal clock and data output	TXSDSCSWAP

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								serial clock output polarity	TXSCINV
		1						inverted	
		0						normal	
								enable serial clock output	TXSCEN
	1							enabled	
	0							disabled	
								serial clock output enable programming by I^2C-bus	I2CTXSCEN
1								by I^2C-bus interface	
0								by external pin TXSC	
0	1	0	0	1	0	1	1		default value

Table 59 Register TXRFOUTC0 (address: F4h, default value: 03h)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								serial output signal amplitude	RFS[3:0]
				0	0	0	0	minimum; 70 mV (p-p)	
				0	0	1	1	default; 300 mV (p-p)	
				1	1	1	1	maximum; 1100 mV (p-p)	
		x	x						reserved
								serial output termination	RFOUTTERMAC
	1							AC-coupled	
	0							DC-coupled	
x									reserved
0	0	0	0	0	0	1	1		default value

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	analog supply voltage	–0.5	+3.6	V
V_{DD}	digital supply voltage	–0.5	+3.6	V
V_n	DC voltage			
	on pins RXPC(Q), RXPD0(Q) to RXPD3(Q), RXFP(Q), RXPAR(Q), TXPARERR(Q), TXPCO(Q), RXPRSCL(Q) and TXPRSCL(Q)	0.7	V_{CC} + 0.5	V
	on pins RXSD(Q), CREF(Q), TXPC(Q), TXPD0(Q) to TXPD3(Q), TXPAR(Q), UI, RREF, LOSTH, RSSI, LOS, CS, SDA, SCL, LM0 to LM2, INT, ENRX, ENTX, WINSIZE, INWINDOW, ENDDR, LOWSWING, ENBA, PAREVEN, OVERFLOW, FIFORESET, ENTXSC, TXSD(Q), TXSC(Q), LOL, FREF0, FREF1, CLKDIR and IPUMP	–0.5	V_{CC} + 0.5	V
I_n	input current			
	on pins RXPC(Q), RXPD0(Q) to RXPD3(Q), RXFP(Q), RXPAR(Q), TXPARERR(Q), TXPCO(Q), RXPRSCL(Q) and TXPRSCL(Q)	–20	+20	mA
	on pins RXSD(Q) and CREF(Q)	–30	+30	mA
	on pin INT	–2	+2	mA
	on pins TXPC(Q), TXPD0(Q) to TXPD3(Q) and TXPAR(Q)	–25	+25	mA
T_{amb}	ambient temperature	–40	+85	°C
T_j	junction temperature	–	125	°C
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	notes 1 and 2	16	K/W

Notes

1. In compliance with JEDEC standards JESD51-5 and JESD51-7.
2. Four-layer Printed-Circuit Board (PCB) in still air with 36 plated vias connected with the heatsink and the second and fourth layer in the PCB.

CHARACTERISTICS

$V_{CCA} = V_{CCD} = V_{CCO}$ = 3.14 to 3.46 V; T_{amb} = –40 to +85 °C; $R_{th(j-a)}$ < 16 K/W; all characteristics are specified for the default test settings (see Table 60); all voltages are referenced to V_{EE}; positive currents flow into the device; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
I_{CCA}	analog supply current		13	21	29	mA
I_{CCD}	digital supply current	notes 1 and 2	350	395	456	mA
I_{DD}	digital supply current		0	0.3	1	mA
I_{CCO}	supply current for clock generator		41	55	64	mA
$I_{CC(tot)}$	total supply current	notes 1 and 2	404	471	550	mA
P_{tot}	total power dissipation	notes 1 and 2	1.3	1.6	1.8	W
CMOS inputs: pins UI, CS, DR0 to DR2, LM0 to LM2, ENRX, ENTX, PAREVEN, WINSIZE, LOWSWING, FREF0, FREF1, ENBA, FIFORESET, CLKDIR, ENTXSC and ENDDR						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{CC}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{CC}$	–	–	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–200	–	–	µA
I_{IH}	HIGH-level input current	$V_{IH} = V_{CC}$	–	–	10	µA
CMOS outputs: pins LOS, INT, INWINDOW, LOL and OVERFLOW						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –0.5 mA	V_{CC} – 0.2	–	V_{CC}	V
Open-drain output: pin INT						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.2	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{CC}$	–	–	10	µA
Serial outputs: pins TXSD(Q) and TXSC(Q)						
$V_{o(p-p)}$	default output voltage swing (peak-to-peak value)	single-ended with 50 Ω external load; DC swing; note 3	220	300	380	mV
Z_o	output impedance	single-ended to V_{CC}	40	50	60	Ω
t_r	rise time	20% to 80%	–	60	90	ps

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_f	fall time	80% to 20%	–	60	90	ps
t_{D-C}	data-to-clock delay	between differential crossovers; see Fig.27	–50	–	+50	ps
δ	duty cycle signal TXSC(Q)	between differential crossovers	40	50	60	%
f_{bit}	output bit rate		30	–	3200	Mbit/s
Serial input: pins RXSD(Q)						
$V_{i(p-p)}$	input voltage swing (peak-to-peak value)	single-ended; note 4; PRBS ($2^7 - 1$)	12	–	500	mV
$V_{i(sens)(p-p)}$	input voltage sensitivity (peak-to-peak value)	single-ended; PRBS ($2^7 - 1$)	–	5	12	mV
V_{sl}	typical slice level range	note 5	–50	–	+50	mV
Z_i	input impedance	differential	80	100	120	Ω
f_{bit}	input data rate		30	–	3200	Mbit/s
LVDS outputs: pins RXPD0(Q) to RXPD3(Q), RXPC(Q), RXPAR(Q), TXPARERR(Q), RXPRSCL(Q),TXPRSCL(Q), RXFP(Q) and TXPCO(Q)						
$V_{o(dif)}$	differential output voltage	R_L = 100 Ω; DC-coupled				
		low swing mode, DC	250	300	360	mV
		high swing mode, DC	400	500	600	mV
$V_{o(cm)}$	common mode output voltage	R_L = 100 Ω, DC-coupled	1.10	1.22	1.33	V
t_r, t_f	rise and fall time	C_L = 1 pF	100	200	250	ps
t_{D-C}	data to clock delay	normal mode; see Fig.28	–200	–	+200	ps
		DDR mode; see Fig.28	$^1/_4T_{clk} - 250$	$^1/_4T_{clk} - 50$	$^1/_4T_{clk} + 150$	ps
δ_{RX}	duty cycle RXPC(Q)	normal mode	45	50	55	%
		DDR mode	47	50	53	%
δ_{TX}	duty cycle TXPCO(Q)	normal mode	45	50	55	%
		DDR mode	47	50	53	%
skew	channel to channel skew	RXPD0 to RXPD3, RXPAR and RXFP; note 6	–	–	100	ps
LVDS inputs: pins TXPD0(Q) to TXPD3(Q), TXPAR(Q) and TXPC(Q)						
V_i	input voltage range		0	–	V_{CC}	mV
$V_{i(th)(dif)}$	differential input voltage threshold	DC	–100	–	+100	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i(p-p)}$	input voltage swing (peak-to-peak value)	single-ended; note 6	–	–	1000	mV
$V_{i(hys)}$	differential hysteresis input voltage	T_{amb} = 0 °C to 85 °C	25	–	–	mV
		T_{amb} = –40 °C to 0 °C	15	–	–	mV
$z_{i(dif)}$	differential input impedance		80	100	120	Ω
$t_{h(co)}$	hold time co-directional clocking	see Fig.29	–	150	300	ps
$t_{su(co)}$	set-up time co-directional clocking	see Fig.29	–	20	300	ps
$t_{h(contra)}$	hold time contra-directional clocking	see Fig.29	–	–1100	–850	ps
$t_{su(contra)}$	set-up time contra-directional clocking	see Fig.29	–	1300	1450	ps
$t_{h(co)DDR}$	hold time co-directional clocking in DDR mode	f_{bit} = 124 to 800 Mbit/s; see Fig.29	–	$0.3T_{clk}$ + 40	$0.3T_{clk}$ + 240	ps
		f_{bit} = 30 to 124 Mbit/s; see Fig.29; note 6	–	4780	5000	ps
$t_{su(co)DDR}$	set-up time co-directional clocking in DDR mode	f_{bit} = 124 to 800 Mbit/s; see Fig.29	–	$-{}^1/_4T_{clk}$ – 130	$-{}^1/_4T_{clk}$ + 200	ps
		f_{bit} = 30 to 124 Mbit/s; see Fig.29; note 6	–	–4560	–3700	ps
$t_{h(contra)DDR}$	hold time contra-directional clocking in DDR mode	see Fig.29	–	$-{}^1/_4T_{clk}$ – 1200	$-{}^1/_4T_{clk}$ – 1000	ps
$t_{su(contra)DDR}$	set-up time contra-directional clocking in DDR mode	see Fig.29	–	${}^1/_4T_{clk}$ + 1400	${}^1/_4T_{clk}$ + 1600	ps
δ	duty cycle clock TXPC(Q)	note 6	40	50	60	%
Reference frequency input; pins CREF(Q)						
$V_{i(p-p)}$	input swing (peak-to-peak value)	single-ended	50	–	1000	mV
V_i	input voltage range	note 6	V_{CC} – 1	–	V_{CC} + 0.25	V
Z_i	input impedance	single-ended to V_{CC}	40	50	60	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Δf_{CREF}	reference clock frequency accuracy	SDH/SONET requirement	–20	–	+20	ppm
f_{CREF}	reference clock frequency	see Section “Reference clock programming”; R = 1, 2, 4, 8, 16 or 32	18 × R	19.44 × R	21 × R	MHz
Reference voltage; pin RREF						
V_{ref}	reference voltage	10 kΩ resistor to V_{EE}	1.17	1.21	1.26	V
Received signal strength indicator; pin RSSI						
$V_{i(p-p)}$	detectable input voltage swing on serial data input (peak-to-peak value)	single-ended	5	–	500	mV
S_{RSSI}	RSSI sensitivity	see Fig.4	15	17	20	mV/dB
$V_{RSSI(32mV)}$	output voltage	serial data input voltage V_i = 32 mV; PRBS($2^{31} - 1$)	580	680	780	mV
ΔV_o	output voltage variation	input 30 to 3200 Mbit/s; PRBS($2^{31} - 1$); V_{CC} = 3.14 to 3.47 V; ΔT = 120 °C	–50	–	+50	mV
Z_o	output impedance		–	1	10	Ω
$I_{o(source)}$	output source current		–	–	1	mA
$I_{o(sink)}$	output sink current		–	–	0.4	mA
LOS detector						
hys	hysteresis	note 7	–	3	–	dB
t_a	assert time	$\Delta V_{i(p-p)}$ = 3 dB	–	–	5	µs
t_d	de-assert time	$\Delta V_{i(p-p)}$ = 3 dB	–	–	5	µs
Clean-up PLL: pin IPUMP						
$I_{cp(source)}$	charge pump source current	CLUPPLLHG = 0	–	–0.1	–	mA
		CLUPPLLHG = 1	–	–1	–	mA
$I_{cp(sink)}$	charge pump sink current	CLUPPLLHG = 0	–	0.1	–	mA
		CLUPPLLHG = 1	–	1	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Jitter characteristics						
$J_{tol(p-p)}$	jitter tolerance to serial data input signal (peak-to-peak value)	STM1/OC3 mode; PRBS(2^{23} – 1)				
		f = 6.5 kHz	3	>10	–	UI
		f = 65 kHz	0.3	>1	–	UI
		f = 1 MHz	0.3	>0.5	–	UI
		STM4/OC12 mode; PRBS(2^{23} – 1)				
		f = 25 kHz	3	>10	–	UI
		f = 250 kHz	0.3	>1	–	UI
		f = 5 MHz	0.3	>0.5	–	UI
		STM16/OC48 mode; PRBS(2^{23} – 1)				
		f = 100 kHz	3	10	–	UI
		f = 1 MHz	0.3	1	–	UI
		f = 20 MHz	0.3	0.5	–	UI
$J_{gen(p-p)}$	jitter generation at serial data and clock output (peak-to-peak value)	STM1/OC3 mode; notes 8 and 9				
		f = 500 Hz to 1.3 MHz	–	–	16	mUI
		f = 12 kHz to 1.3 MHz	–	–	4	mUI
		f = 65 kHz to 1.3 MHz	–	–	4	mUI
		STM4/OC12 mode; notes 8 and 9				
		f = 1 kHz to 5 MHz	–	–	63	mUI
		f = 12 kHz to 5 MHz	–	–	13	mUI
		f = 250 kHz to 5 MHz	–	–	13	mUI
		STM16/OC48 mode; note 8				
		f = 5 kHz to 20 MHz	–	32	250	mUI
		f = 12 kHz to 20 MHz	–	30	50	mUI
		f = 1 MHz to 20 MHz	–	6	50	mUI
PLL characteristics receiver						
t_{acq}	acquisition time	30 Mbit/s; note 6	–	–	200	µs
$t_{acq(pc)}$	acquisition time at power cycle	30 Mbit/s; note 6	–	–	10	ms
$t_{acq(o)}$	acquisition time octave change	30 Mbit/s; note 6	–	–	10	µs
I²C-bus input and output: pins SCL and SDA						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{CC}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{CC}$	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{hys}	hysteresis of Schmitt-trigger inputs	note 6	$0.05V_{CC}$	–	–	V
V_{OL}	LOW-level output voltage on pin SDA (open-drain)	I_{OL} = 3 mA	0	–	0.4	V
I_{LI}	input leakage current		–10	–	+10	µA
C_i	input capacitance	note 6	–	–	10	pF
I²C-bus timing; note 6						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{LOW}	SCL LOW time		1.3	–	–	µs
$t_{HD;STA}$	hold time START condition		0.6	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
$t_{SU;STA}$	set-up time START condition		0.6	–	–	µs
$t_{HD;DAT}$	data hold time		0	–	0.9	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{SU;STO}$	set-up time STOP condition		0.6	–	–	µs
t_r	SCL and SDA rise time		20	–	300	ns
t_f	SCL and SDA fall time		20	–	300	ns
t_{BUF}	bus free time between STOP and START		1.3	–	–	µs
C_b	capacitive load for each bus line		–	–	400	pF
t_{SP}	pulse width of allowable spikes		0	–	50	ns
V_{nL}	noise margin at LOW-level		$0.1V_{CC}$	–	–	V
V_{nH}	noise margin at HIGH-level		$0.2V_{CC}$	–	–	V

Notes

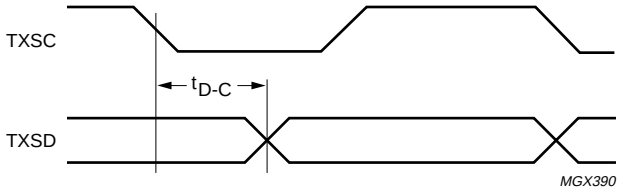
1. For the typical specification LVDS outputs: RXPAR(Q), RXPRSCL(Q), TXPARERR(Q), TXPCO(Q) and TXPRSCL(Q) are disabled. Also serial output TXSC(Q) is disabled.
2. The following conditions are valid for the maximum specification and are additional to the default settings: bit CLUPPLLEN = 1 (clean-up PLL is enabled); bit CLUPPLLHG = 1 (high gain); line loop back is enabled; pin LOWSWING = LOW (high swing for LVDS outputs); bits RFS[3:0] = 1111 (maximum output swing for TXSD(Q) and

TXSC(Q). These maximum settings yield the following maximum specification values: I_{CCD} = 680 mA, $I_{CC(tot)}$ = 774 mA and P_{tot} = 2.7 W.

3. The output swing is adjustable between 70 mV (typical) and 1100 mV (typical) in 16 steps controlled by bits RFS[3:0] of the register TXRFOUTC0 (F4h).
4. The RF input is protected against a differential overvoltage; the maximum input current is 30 mA.
5. The slice level is adjustable in 256 steps controlled by register LIMSL (D2h).
6. Guaranteed by design.
7. The hysteresis is adjustable in 8 steps controlled by bits HTLCB[2:0] of register LIMLOSCON (D1h).
8. Reference frequency of 19.44 MHz, with a phase-noise of less than −140 dBc for frequencies of more than 12 kHz from the carrier (measured during 60 seconds, within the appropriate bandwidth).
9. For bit rates lower than 1.8 Gbit/s, the jitter decreases by the octave division ratio M.

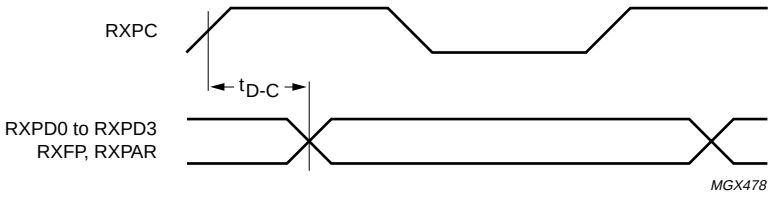
Table 60 Default test settings

PIN	SETTING
UI = LOW	pre-programmed mode
DR0 = LOW, DR1 = HIGH, DR2 = LOW	STM16/OC48
LM0 = HIGH, LM1 = HIGH, LM2 = HIGH	normal mode
ENRX = HIGH	receiver enabled
ENTX = HIGH	transmitter enabled
ENDDR = LOW	DDR mode disabled
LOWSWING = HIGH	low LVDS swing
FREF0 = HIGH, FREF1 = HIGH	19.44 MHz reference
RREF	R_{RREF} = 10 kΩ to V_{EE}
IPUMP	open circuit
RSSI	open circuit
LOSTH	V_{LOSTH} = 0.6 V
ENTXSC = HIGH	serial output clock enabled
WINSIZE = HIGH	1000 ppm
ENBA = HIGH	automatic byte alignment
PAREVEN = HIGH	even parity
CREF(Q)	AC-coupled, f_i = 19.44 MHz, V_i = 0.2 V (p-p) single-ended
RXSD(Q)	input STM16; PRBS ($2^{23} - 1$)
RXPD0(Q) to RXPD3(Q), RXFP(Q), RXPAR(Q), RXPC(Q), TXPCO(Q), TXPARERR(Q), TXPRSCL(Q) and RXPRSCL(Q)	100 Ω differential outputs
TXPC(Q), TXPD0(Q) to TXPD3(Q) and TXPAR	open circuit
FIFORESET = LOW	normal mode
CLKDIR = HIGH	co-directional clocking
TXSD(Q) and TXSC(Q)	external load of 50 Ω to V_{CC}
CMOS outputs	not loaded



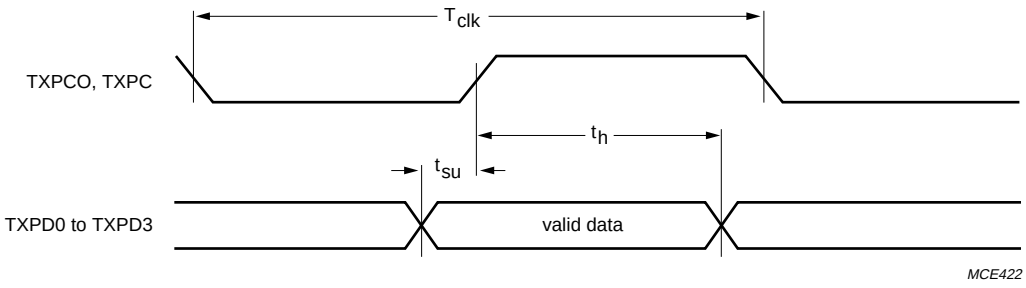
The timing is measured from the crossover point of the clock output signal to the crossover point of the data output (all signals are differential).

Fig.27 Serial bus output timing.



The timing is measured from the crossover point of the clock output signal to the crossover point of the data output (all signals are differential).

Fig.28 Parallel bus output timing.



The timing is measured from the crossover point of the reference signal to the crossover point of the input.

Fig.29 Parallel bus co-directional (TXPC) and contra-directional (TXPCO) timing.

APPLICATION INFORMATION

Calculations on the clean-up PLL

The important specifications of the clean-up PLL are the bandwidth (f_{-3dB}) and the jitter peaking. If these are known, the component parameters can be calculated. First assume that the bandwidth of the VCXO control input ($f_{-3dB(vcxo)}$) is much higher than f_{-3dB} and C2 is left out. This simplifies the loop into a second order, type II PLL. In a second order PLL, the damping factor ζ determines the amount of peaking. To obtain peaking of less than 0.1 dB, ζ must be higher than 4.3. For peaking of less than 0.05 dB, ζ must be higher than 6. See Fig.30 for an example.

Now R and C1 may be calculated with the following formulas:

$$R = \frac{RDIV \times 2 \times \pi \times f_{-3dB}}{K_{VCXO} \times I_{CP}}$$

$$C_1 = \frac{K_{VCXO} \times I_{CP} \times \zeta^2}{RDIV \times \pi^2 \times (f_{-3dB})^2}$$

Where:

RDIV = reference divider ratio (1, 2, 4, 8, 16 or 32)

f_{-3dB} = clean-up PLL bandwidth in Hz

K_{VCXO} = VCXO gain in Hz/V

I_{CP} = charge pump current in A (100 μA or 1 mA, depending on I²C-bus bit CLUPPLLHG)

ζ = damping factor.

These formulas are valid if:

$\zeta >> 1$ and

$f_{-3dB(VCXO)} > 2 \times f_{-3dB}$ and

$$\frac{C1 + C2}{2 \times \pi \times R \times C1 \times C2} > 2 \times f_{-3dB}.$$

The transfer has a first order roll-off (i.e. 20 dB/decade), up to the bandwidth of the VCXO control input. If a second order roll-off is required C2 may be added, as long as

$$\frac{C1 + C2}{2 \times \pi \times C1 \times C2} > 2 \times f_{-3dB}$$

Example: The clean-up PLL uses a VCXO with a frequency of 20 MHz and has a gain K_{VCXO} = 2000 Hz/V. The bandwidth of the control input is $f_{-3dB(VCXO)}$ = 10 kHz. Since the reference frequency is 20 MHz, the reference divider ratio RDIV = 1. According to the specification, the maximum allowed jitter peaking is 0.1 dB. To add some margin the design is for less than 0.05 dB peaking, so ζ = 6. Also according to the specification, f_{-3dB} should be less than 100 kHz. To satisfy the conditions as previously described, $f_{-3\,dB} < 0.5 \times f_{-3\,dB(VCXO)} < 5$ kHz. To cope with component tolerances, $f_{-3dB(VCXO)}$ = 2.5 kHz is chosen.

$$R = \frac{1 \times 2 \times \pi \times 2500}{2000 \times 100 \times 10^{-6}} \Omega = 78540 \Omega$$

$$C_1 = \frac{2000 \times 100 \mu F \times 6^2}{1 \times \pi^2 \times 2500^2} = 116.7 nF$$

Choosing I_{CP} = 1 mA yields R = 7854 Ω and C1 = 1.167 μF.

To calculate f_{-3dB} and ζ, if R and C1 are known, use the following formulas:

$$f_{-3dB} = \frac{K_{VCXO} \times I_{CP} \times R}{2 \times \pi \times RDIV}$$

$$\zeta = \frac{R}{2} \times \sqrt{\frac{K_{VCXO} \times I_{CP} \times C1}{RDIV}}$$

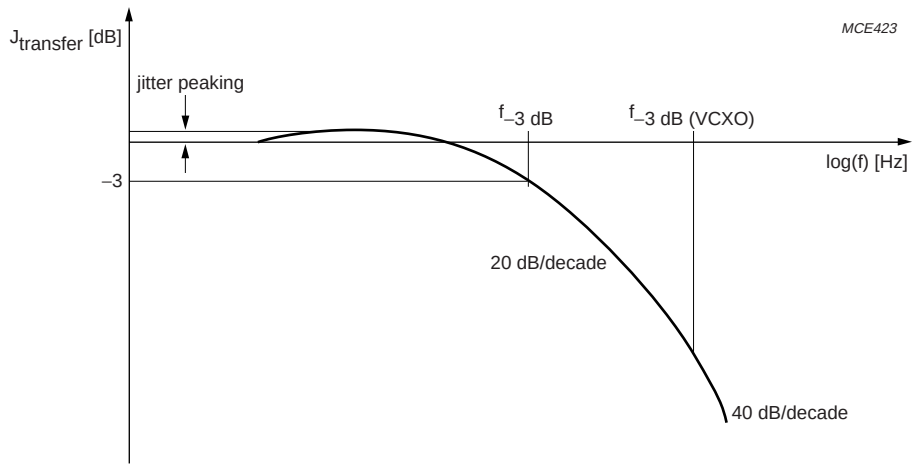


Fig.30 Clean-up PLL jitter transfer.

I/O CONFIGURATIONS

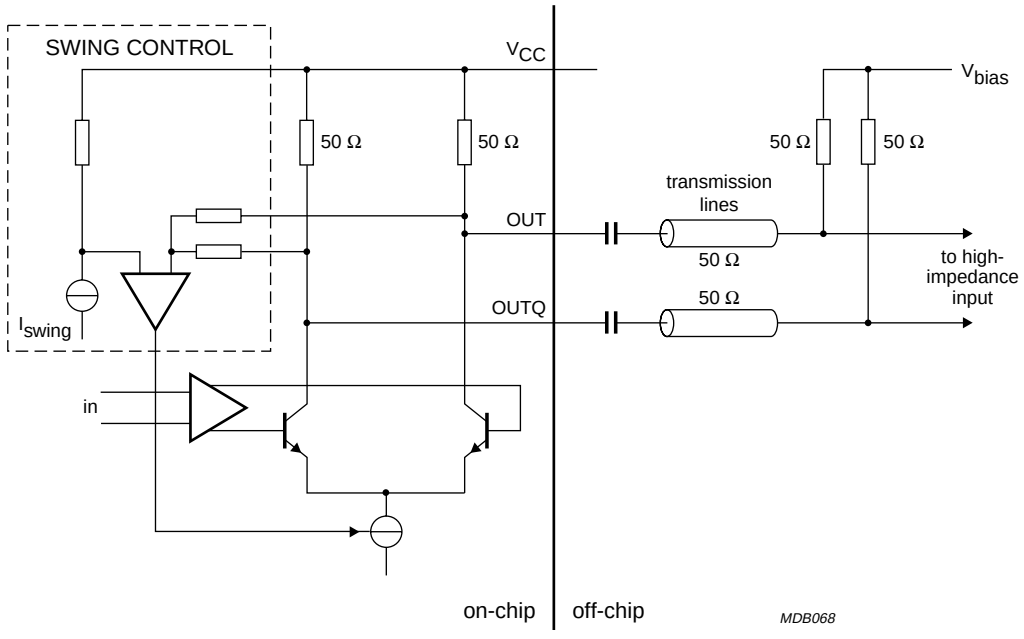


Fig.31 Serial RF output (AC-coupled).

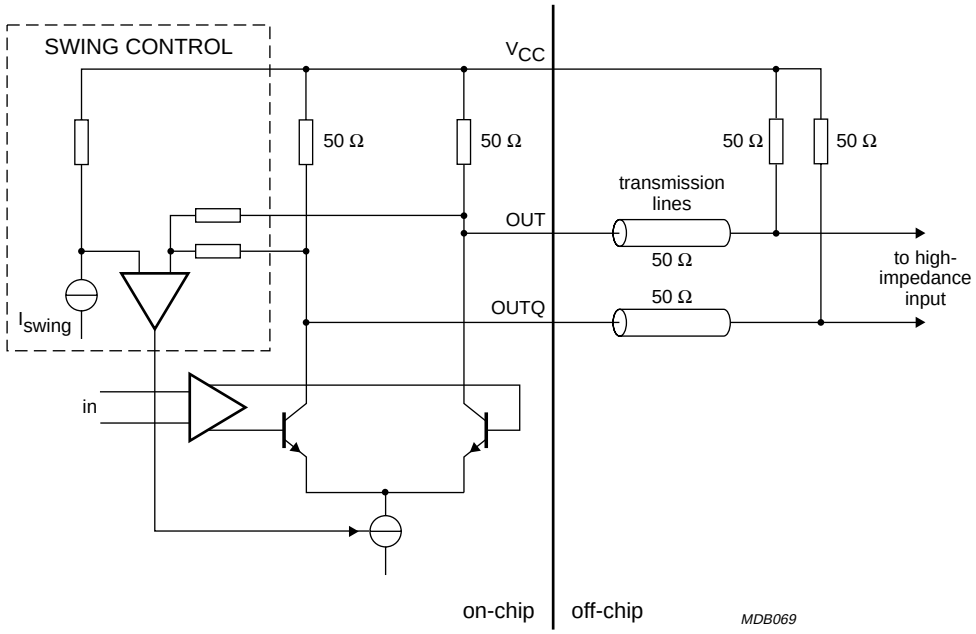


Fig.32 Serial RF output (DC-coupled).

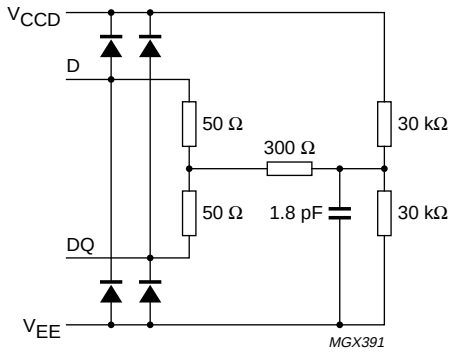


Fig.33 LVDS input.

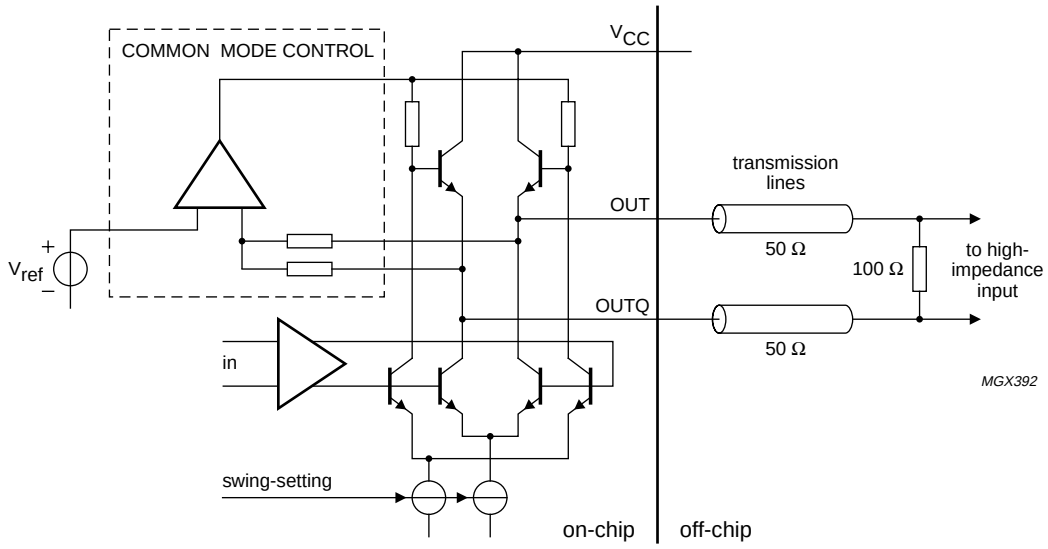


Fig.34 LVDS output (DC-coupled).

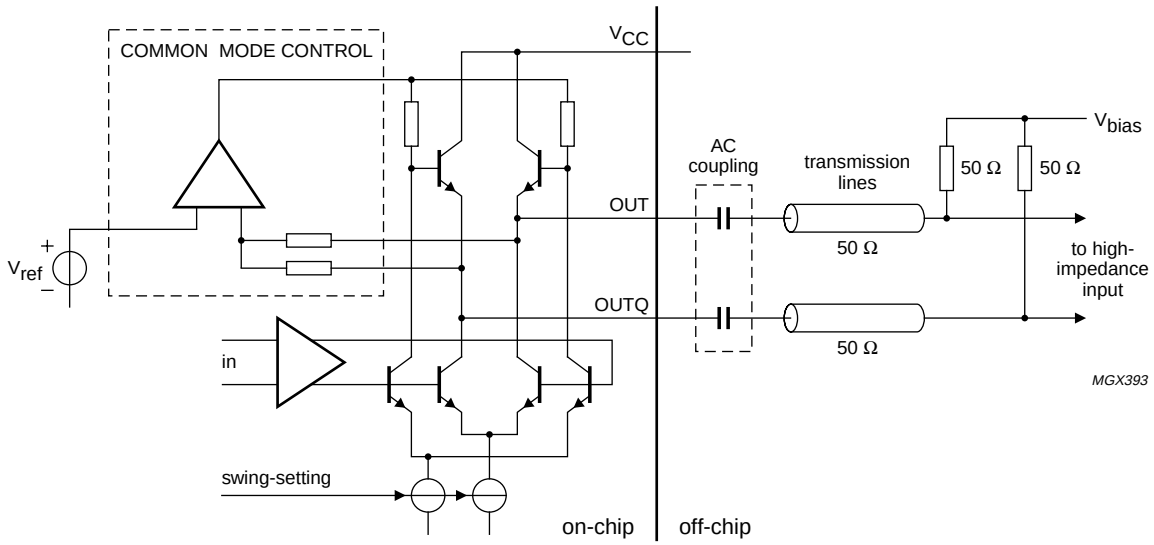


Fig.35 LVDS output (AC-coupled).

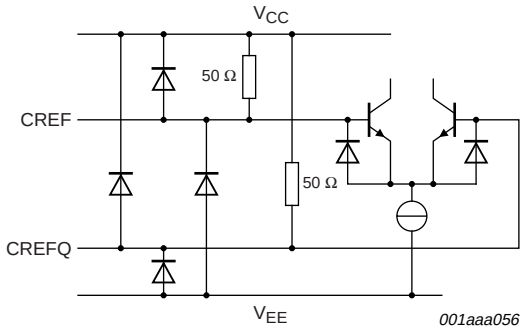
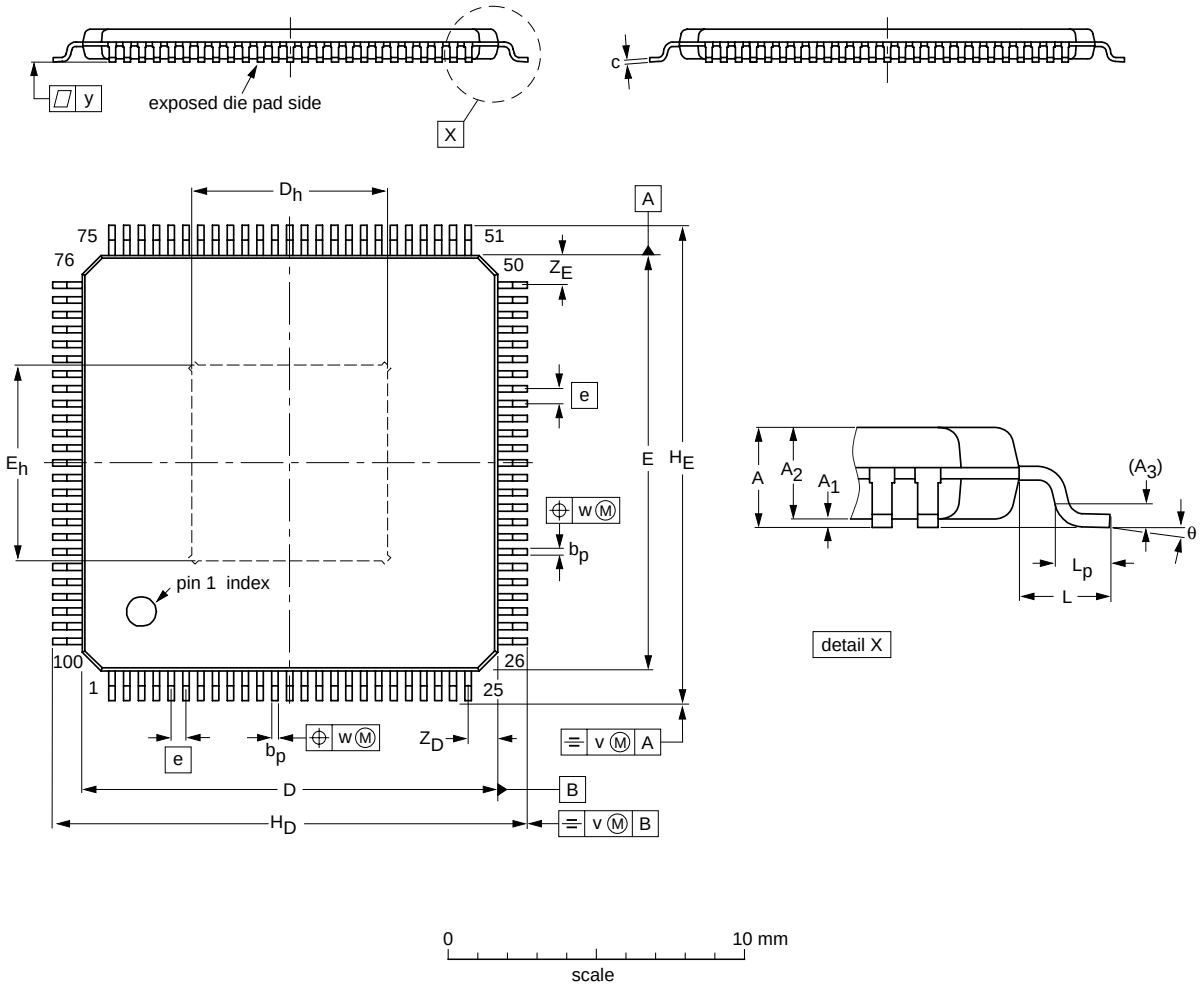


Fig.36 Reference clock input.

PACKAGE OUTLINE

HTQFP100: plastic thermal enhanced thin quad flat package; 100 leads; body 14 x 14 x 1 mm; exposed die pad **SOT638-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	14.1 13.9	7.1 6.1	14.1 13.9	7.1 6.1	0.5	16.15 15.85	16.15 15.85	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT638-1						~~01-03-30~~ 03-04-07

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON-T and SSOP-T packages
  - for packages with a thickness 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
9. Hot bar or manual soldering is suitable for PMFP packages.

ADDITIONAL SOLDERING INFORMATION

The die pad has to be soldered to the PCB for thermal and grounding reasons.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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