TJF1103

100BASE-T1 PHY for industrial single-pair Ethernet

Rev. 1.0 — 22 May 2026 Product data sheet

1 General description

The TJF1103 is a 100BASE-T1 compliant Ethernet PHY. The device provides 100 Mbit/s transmit and receive capability over unshielded twisted-pair cables, supporting a cable length of up to 15 m. It is available in two variants. The TJF1103A variant contains standard MII/RMII and RGMII(-ID) MAC interfaces. The TJF1103B variant provides an SGMII interface.

For sustainable system efficiency and flexibility, the TJF1103 has been optimized for low power consumption and to be highly robust, while maintaining a small package footprint.

The TJF1103 is designed to handle the stringent requirements of industrial applications. It is typically used in electronic control units (ECUs) such as industrial gateways, PLC, motor drives, robotics, commercial vehicles.

Efficient IEEE1588v2 and 802.1AS-2020 compliant time stamping provides a high-resolution global time synchronization accuracy.

2 Features and benefits

2.1 General

- IEEE 802.3 Clause 96 compliant 100BASE-T1 PHY, see ref.[1]
- –40°C to +105°C ambient temperature
- Compact 36-pin HVQFN package (6 × 6 mm) for PCB space-constraint applications
- Standard MII/RMII/RGMII MAC interface (TJF1103A)
  - Optional integrated delay (RGMII-ID) in receive and transmit clock path
  - 3.3 V, 2.5 V, or 1.8 V LVCMOS I/O standard for MII/RMII/RGMII/MDIO
- SGMII-compliant MAC interface (TJF1103B)
- IEEE1588v2 and 802.1AS-2020 2-step timestamping support
  - Synchronization of timestamp clock with other switch or PHY devices
  - Timestamp delivery via in-band (RX-only) or SMI communication
  - RX and TX start of of frame (SOF) indication via GPIO pins
- IEEE1149.1 and IEEE1149.6 compliant JTAG interface for boundary scan
- MDIO register access
  - IEEE 802.3 Clause 45
  - IEEE 802.3 Clause 22 (indirect access)

2.2 Optimized for industrial use cases

- Low latency for digital control
- Support for shielded and unshielded twisted-pair cable
- Adaptive receive equalizer optimized for cable length of up to 15 m
  - Echo cancellation up to 25 m[1]

1 OPEN Whole communication channel (WCC) requirements as per OPEN Alliance Definitions for Communication Channel v1.0.

- Enhanced integrated pulse shaping for low RF emissions
- EMC-optimized output driver configuration for RGMII (TJF1103A)
- MDI pins protected against ESD up to ±4 kV HBM according to JEDEC JS-001
- MDI pins protected against ESD up to ±500V CDM according to JEDEC JS-002
- MDI pins do not need external filtering or ESD protection

2.3 Low-power mode

- Inhibit output for voltage regulator control
- Robust remote wake-up detection via bus lines
- PHY level sleep/wakeup support, including forwarding
- Wake-up via SMI-access

2.4 Diagnosis

- Advanced PHY diagnostic features
  - Signal Quality Indicator (SQI)
  - Signal MSE (Mean Square Error) indicating the signal error at the slicer
  - Diagnosis of cable errors (short or open)
  - Link training time measurement
  - Link losses since reset/power on
  - Symbol errors since power on
- Optional Ethernet frame generator and checker for built-in self-test (BIST)
- Latent fault detection
- Real-time monitoring of link stability and data quality
- Gap-free supply undervoltage detection with fail-silent behavior
- Gap-free supply undervoltage detection
- Temperature monitor with overtemperature detection
- Internal, external and remote loopback modes for diagnostics

2.5 Miscellaneous

- 3.3 V or 2.5 V single supply operation
- 3.3 V, 2.5 V, 1.1 V individual supply operation
- 3.3 V, 2.5 V I/O for RST_N, INH, and wake interface
- GPIO, LED, PPS_SYNC, and reference clock inputs/outputs
- Support for crystal or digital clock input
- Pin strapping to configure:
  - Managed and autonomous operation modes
  - LEADER/FOLLOWER mode
  - Polarity correction
  - xMII/JTAG modes
  - PHY address
- On-chip termination resistors
- Jumbo frame support up to 16 kB

3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TJF1103AHN	HVQFN36	plastic thermal enhanced very thin quad flat package; no leads; 36 terminals; body 6 × 6 × 0.85 mm	SOT1092-2
TJF1103BHN			

4 Block diagram

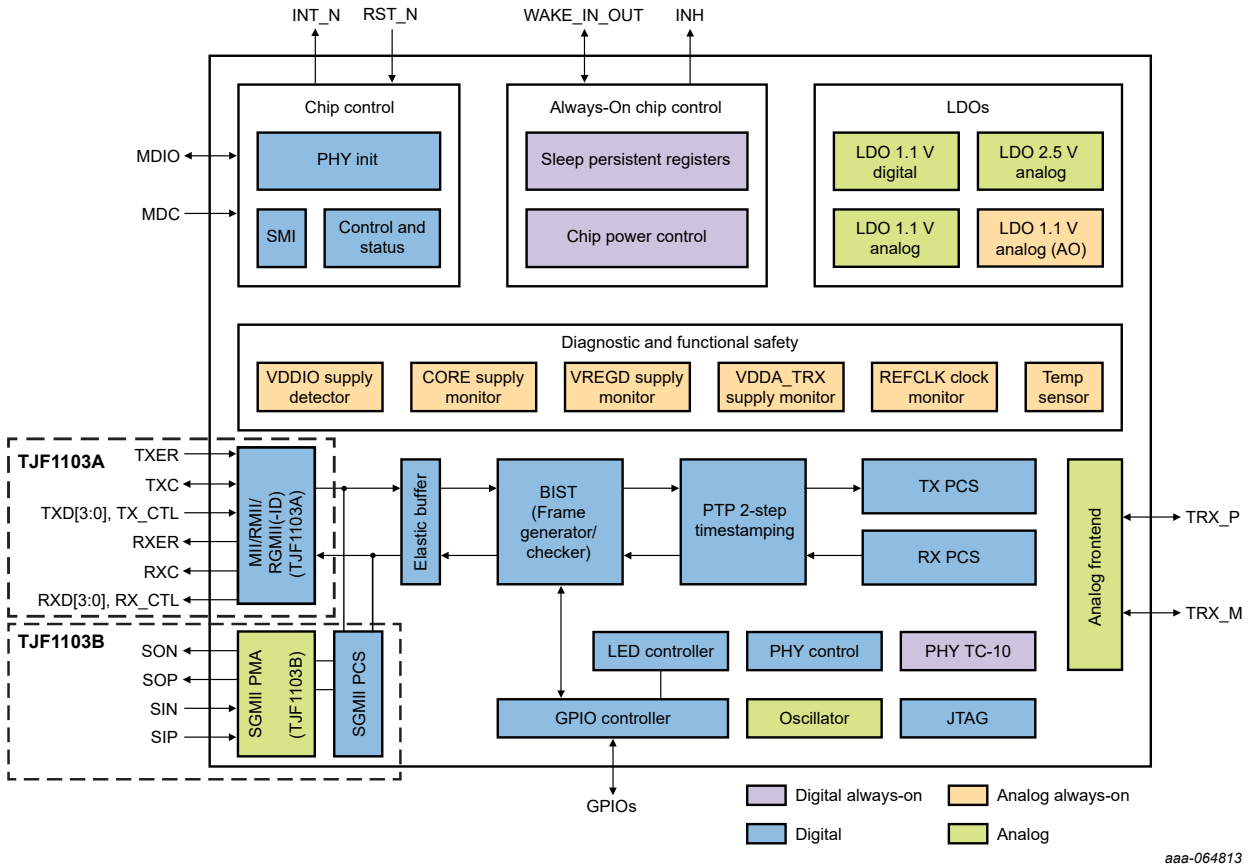


Figure 1. Block diagram

5 Pinning information

5.1 Pinning

The pin configurations of the TJF1103A and TJF1103B are shown in Figure 2. The following standard interfaces are provided in the TJF1103A: MII, RMII, RGMII, MDIO and MDI. The following standard interfaces are provided in the TJF1103B: SGMII, MDIO and MDI. Die pad is ground.

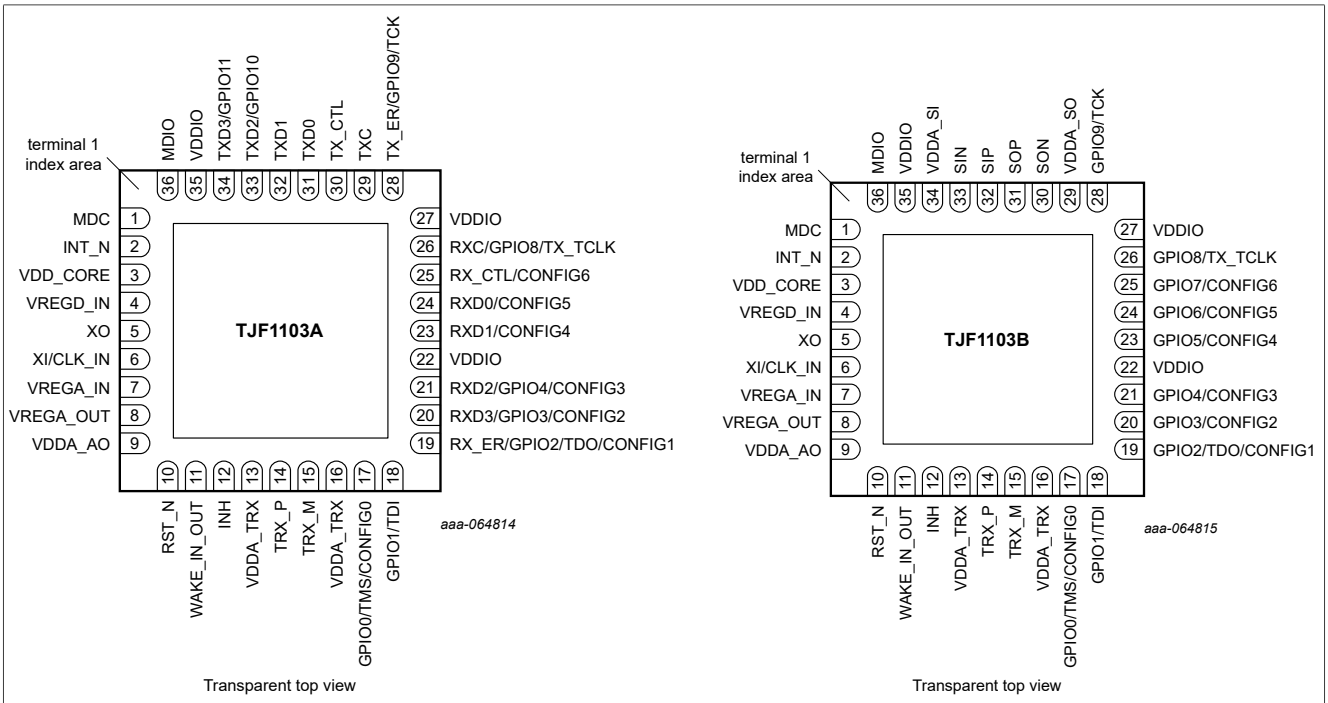


Figure 2. Pin configuration diagrams

5.2 Pin description

Table 2. TJF1103A pinning

Symbol	Pin	Type[1][2]	IO supply domain[3]	Description
MDC	1	I	VDDIO	SMI clock input
INT_N	2	O, PU	VDDIO	interrupt low-side switch output
VDD_CORE	3	P	—	digital supply (1.1 V)
VREGD_IN	4	P	—	regulator input (1.1 V, 2.5 V, 3.3 V)
XO	5	AO	—	crystal feedback
XI/CLK_IN	6	AI	—	crystal input/digital clock input
VREGA_IN	7	P	—	analog regulator input (2.5 V, 3.3 V)
VREGA_OUT	8	P	—	analog regulator output (2.5 V)
VDDA_AO	9	P	—	always on supply (2.5 V, 3.3 V)
RST_N	10	I, PU	VDDA_AO	reset input

Table 2. TJF1103A pinning*...continued*

Symbol	Pin	Type[1][2]	IO supply domain[3]	Description
WAKE_IN_OUT	11	IO	VDDA_AO	local/forwarding wake-up input/output (configurable)
INH	12	O	VDDA_AO	inhibit high-side switch output for Vreg control
VDDA_TRX	13	P	—	MDI analog voltage supply (2.5 V)
TRX_P	14	AIO	—	plus terminal for Tx/Rx signal
TRX_M	15	AIO	—	minus terminal for Tx/Rx signal
VDDA_TRX	16	P	—	MDI analog voltage supply (2.5 V)
GPIO0/TMS/CONFIG0	17	IO	VDDIO	JTAG test mode select, GPIO0, CONFIG0
GPIO1/TDI	18	IO	VDDIO	JTAG test data in, GPIO1
RX_ER/GPIO2/TDO/ CONFIG1	19	IO	VDDIO	RMII/MII RX_ER, GPIO2, JTAG test data out, CONFIG1
RXD3/GPIO3/CONFIG2	20	IO	VDDIO	RGMII/MII RX data 3 output, GPIO3, CONFIG2
RXD2/GPIO4/CONFIG3	21	IO	VDDIO	RGMII/MII RX data 2 output, GPIO4, CONFIG3
VDDIO	22	P	—	digital interface I/O voltage (1.8 V, 2.5 V, 3.3 V)
RXD1/CONFIG4	23	IO	VDDIO	RGMII/RMII/MII RX data 1 output, CONFIG4
RXD0/CONFIG5	24	IO	VDDIO	RGMII/RMII/MII RX data 0 output, CONFIG5
RX_CTL/CONFIG6	25	IO	VDDIO	RGMII/RMII/MII interface receive control input, CONFIG6
RXC/GPIO8/TX_TCLK	26	IO	VDDIO	RGMII/MII interface receive clock, GPIO8, test clock TX_TCLK
VDDIO	27	P	—	digital interface I/O voltage (1.8 V, 2.5 V, 3.3 V)
TX_ER/GPIO9/TCK	28	IO	VDDIO	JTAG test clock, MII TX_ER, GPIO9
TXC	29	IO	VDDIO	RGMII/RMII/MII transmit clock
TX_CTL	30	I, PD	VDDIO	RGMII/RMII/MII interface transmit control input
TXD0	31	I, PD	VDDIO	RGMII/RMII/MII TX data 0 input
TXD1	32	I, PD	VDDIO	RGMII/RMII/MII TX data 1 input
TXD2/GPIO10	33	IO, PD	VDDIO	RGMII/MII TX data 2 input, GPIO10
TXD3/GPIO11	34	IO, PD	VDDIO	RGMII/MII TX data 3 input, GPIO11
VDDIO	35	P	—	digital interface I/O voltage (1.8 V, 2.5 V, 3.3 V)
MDIO	36	IO	VDDIO	SMI Data I/O
GNDPAD	37	G	—	exposed die pad

[1] I: digital input; O: digital output; IO: digital input/output; AO: Analog output; AI: Analog Input; AIO: Analog input/output; PU: weak pull-up; PD: pull-down; P: power supply. G: ground
[2] Pin type depends on functional mode; consult the functional description for details.
[3] Only applicable to CMOS input/output pins

Table 3. TJF1103B pinning

Symbol	Pin	Type[1][2]	IO supply domain[3]	Description
MDC	1	I	VDDIO	SMI clock Input
INT_N	2	O, PU	VDDIO	interrupt low-side switch output
VDD_CORE	3	P	—	digital supply (1.1 V)
VREGD_IN	4	P	—	regulator Input (1.1 V, 2.5 V, 3.3 V)
XO	5	AO	—	crystal feedback
XI/CLK_IN	6	AI	—	crystal input/digital clock input
VREGA_IN	7	P	—	analog regulator input (2.5 V, 3.3 V)
VREGA_OUT	8	P	—	analog regulator output (2.5 V)
VDDA_AO	9	P	—	always on supply (2.5 V, 3.3 V)
RST_N	10	I, PU	VDDA_AO	reset Input
WAKE_IN_OUT	11	IO	VDDA_AO	local/forwarding wake-up input/output (configurable)
INH	12	O	VDDA_AO	inhibit high-side switch output for Vreg control
VDDA_TRX	13	P	—	MDI analog voltage supply (2.5 V)
TRX_P	14	AIO	—	plus terminal for Tx/Rx signal
TRX_M	15	AIO	—	Minus terminal for Tx/Rx signal
VDDA_TRX	16	P	—	MDI analog voltage supply (2.5 V)
GPIO0/TMS/CONFIG0	17	IO	VDDIO	GPIO0, JTAG test mode select, CONFIG0
GPIO1/TDI	18	IO	VDDIO	GPIO1, JTAG test data in
GPIO2/TDO/CONFIG1	19	IO	VDDIO	GPIO2, JTAG test data out, CONFIG1
GPIO3/CONFIG2	20	IO	VDDIO	GPIO3, CONFIG2
GPIO4/CONFIG3	21	IO	VDDIO	GPIO4, CONFIG3
VDDIO	22	P		digital interface I/O voltage (1.8 V, 2.5 V, 3.3 V)
GPIO5/CONFIG4	23	IO	VDDIO	GPIO5, CONFIG4
GPIO6/CONFIG5	24	IO	VDDIO	GPIO6, CONFIG5
GPIO7/CONFIG6	25	IO	VDDIO	GPIO7, CONFIG6
GPIO8/TX_TCLK	26	IO	VDDIO	GPIO8, test clock TX_TCLK
VDDIO	27	P	—	digital interface I/O voltage (1.8 V, 2.5 V, 3.3 V)
TCK/GPIO9	28	IO, PD	VDDIO	JTAG test clock, GPIO9
VDDA_SO	29	P	—	analog SGMII transmitter supply (1.1 V)
SON	30	AO	—	minus Terminal for SGMII output
SOP	31	AO	—	plus Terminal for SGMII output
SIP	32	AI	—	plus Terminal for SGMII input
SIN	33	AI	—	minus Terminal for SGMII input
VDDA_SI	34	P	—	analog SGMII receiver supply (1.1 V)
VDDIO	35	P	—	digital interface I/O voltage (1.8 V, 2.5 V, 3.3 V)
MDIO	36	IO	VDDIO	SMI data I/O

Table 3. TJF1103B pinning*...continued*

Symbol	Pin	Type[1][2]	IO supply domain[3]	Description
GNDPAD	37	G	—	exposed die pad

[1] I: digital input; O: digital output; IO: digital input/output; AO: Analog output; AI: Analog Input; AIO: Analog input/output; PU: weak pull-up; PD: pull-down; P: power supply. G: ground
[2] Pin type depends on functional mode; consult the functional description for details.
[3] Only applicable to CMOS input/output pins

6 Functional description

6.1 Operating modes

A mode transition diagram showing internal device-level state transitions is shown in Figure 3. It represents externally observable behavior.

Internally, the device architecture, including the register layout and interrupt tree, is scalable and extends to multiport PHY devices.

See the TJF1103 application notes ref.[6] for a detailed description of application use-cases.

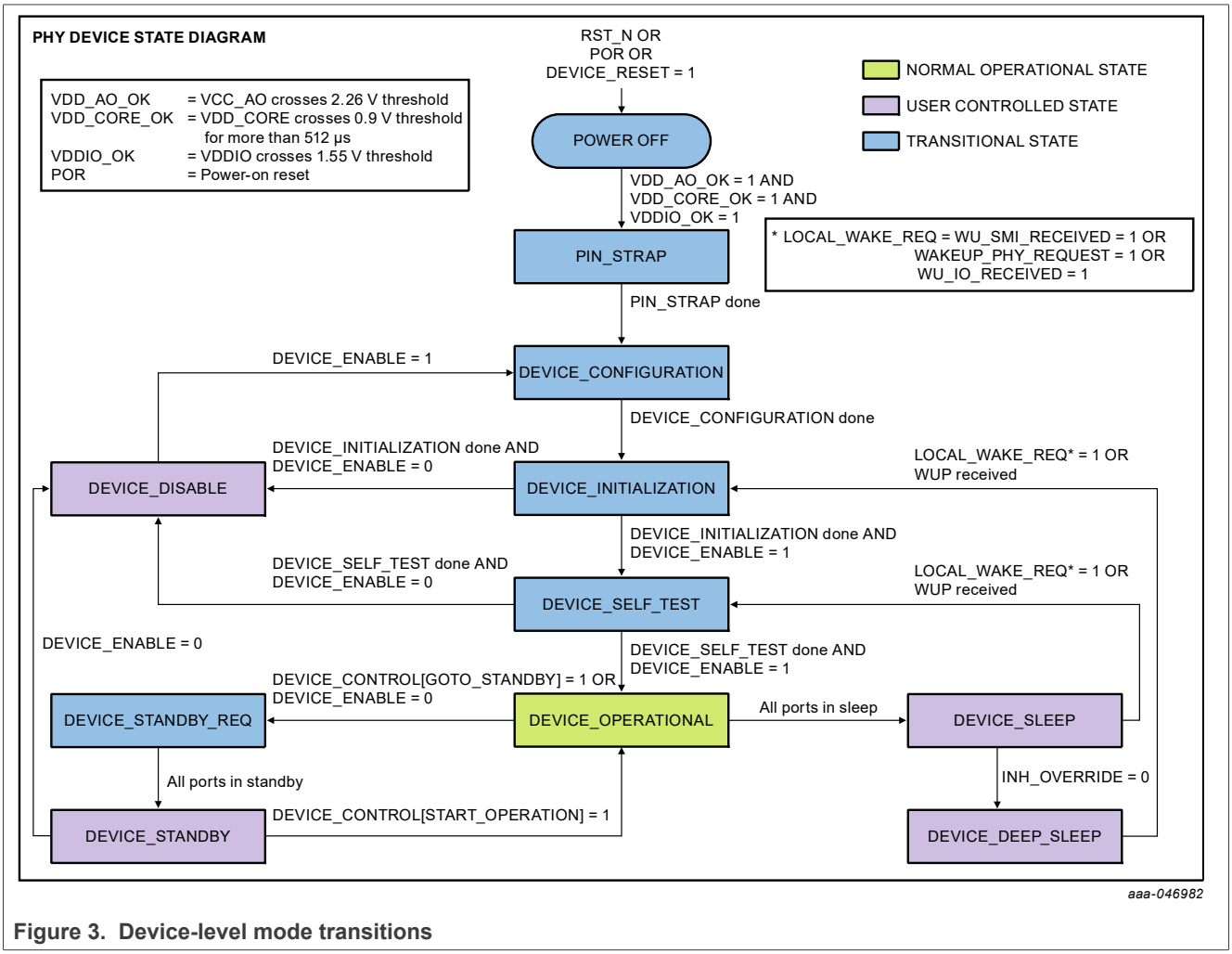


Figure 3. Device-level mode transitions

6.2 Managed/autonomous operation

The device is configured in either managed or autonomous mode, which determines the startup behavior. The mode can be set via pin strapping (see Table 18) or via bit PHY_CONFIG.AUTO_OPERATION (Table 310).

In managed mode, the device transitions to STANDBY state after power-on and device initialization. This allows additional configuration options to be set before bringing the device into OPERATIONAL state by setting PHY_CONTROL[START_OPERATION]. SMI access is required to trigger this transition.

In autonomous mode, the device proceeds to OPERATIONAL state without any interaction needed. In OPERATIONAL state, link-up can begin immediately. This enables very fast link-up after reset and allows parallel link-up and host controller boot-up.

6.3 Data path

The TJF1103 data path consists of multiple connected building blocks: the SGMII SerDes (B variant), xMII (A variant), rate-matching FIFO, the PTP and BIST blocks, and the 100BASE-T1 PHY. Figure 4 provides an overview of the data path and its associated multiplexer controls.

Note: *After device reset, the PTP and BIST blocks are bypassed and the xMII and EPHY blocks are connected.*

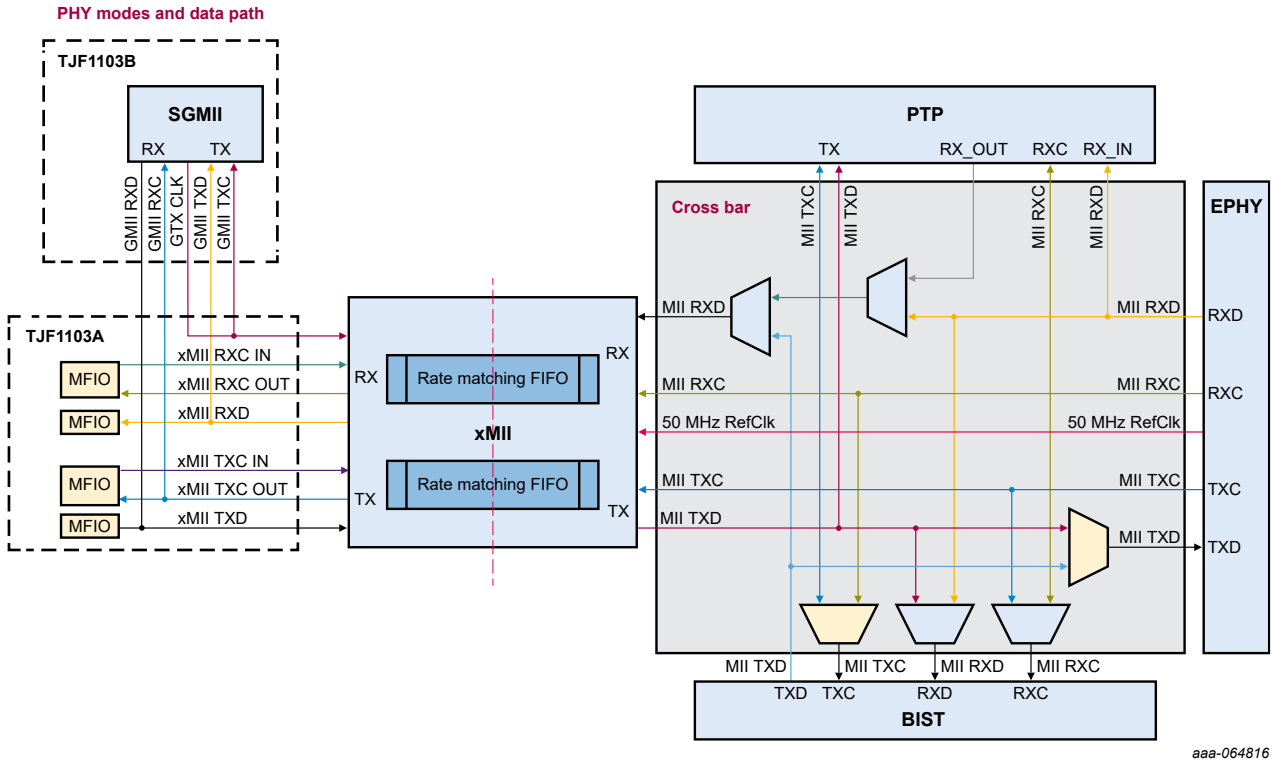


Figure 4. Datapath block diagram

Table 4. xMII Datapath control - TJF1103A

MODE	MII_BASIC_CONFIG[XMII_MODE]	MII_BASIC_CONFIG[ROLE]	XMII_CLK_CONFIG[RMII_CLK_REF]	TXC dir.	RXC dir.	REFCLK src.	TX FIFO	RX FIFO
MII	100	0	0	out	out	XI pin	No	No
revMII	100	1	0	in	in	XI pin	Yes	Yes
RMII	101	0	0	in	—	XI pin	Yes	Yes
RMII clock mode	101	0	1	in	—	TXC	Yes	Yes
revRMII	101	1	0	out	—	XI pin	Yes	Yes
RGMII	111	0	0	in	out	XI pin	Yes	No

Table 5. xMII Data path control - TJF1103B

MODE	MII_BASIC_CONFIG[CMOS_OR_SERDES][1]	MII_BASIC_CONFIG[XMII_MODE]	MII_BASIC_CONFIG[ROLE]	XMII_CLK_CONFIG[RMII_CLK_REF]	TXC dir.	RXC dir.	REFCLK src.	TX FIFO	RX FIFO
SGMII	1	000	0	0	—	—	XI pin	Yes	Yes

[1] Bit CMOS_OR_SERDES is always 1 and bits XMII_MODE always 000 in the TJF1103B.

Table 6. BIST datapath control

BIST MODE	BIST_ENABLE	BIST_TX_TO_EPHY	BIST_TX_TO_XMII	BIST_RX_EPHY_OR_XMII	DRIVER_PORT	CAPTURE_PORT
Mode 1 (EPHY)	1	10	00	1	CBT1_TX	CBT1_RX
Mode 2 (xMII)	1	10	00	0	CBT1_TX	XMII_TX
Mode 3	1	00	10	0	XMII_RX	XMII_TX
Mode 4	1	00	10	1	XMII_RX	CBT1_RX
Disabled (default)	0	—	—	—	DISABLED	

The PTP block is added to the datapath by deasserting PORT_PTP_CONTROL[BYPASS].

6.4 Startup self-test

The TJF1103 executes a self-test sequence on startup. The test is split into two parts: a device-level self-test and a port-level self-test. Both tests are part of the device and port startup sequence (see Section 6.1). The tests consists of several steps including voltage, clock, and latent fault checks.

Voltage supply inputs are tested for overvoltage (OV) and/or undervoltage (UV) conditions. The 25 MHz reference (Crystal or TXC pin in RMII-clkmode) is compared against the internal free-running oscillator.

When both the device and the port self-test checks have been completed and passed, bit FUSA_STATUS in the device status register (Table 60) is set and a FUSA_PASS_IRQ interrupt triggered automatically. When a test fails, the issue is reported via the associated status register.

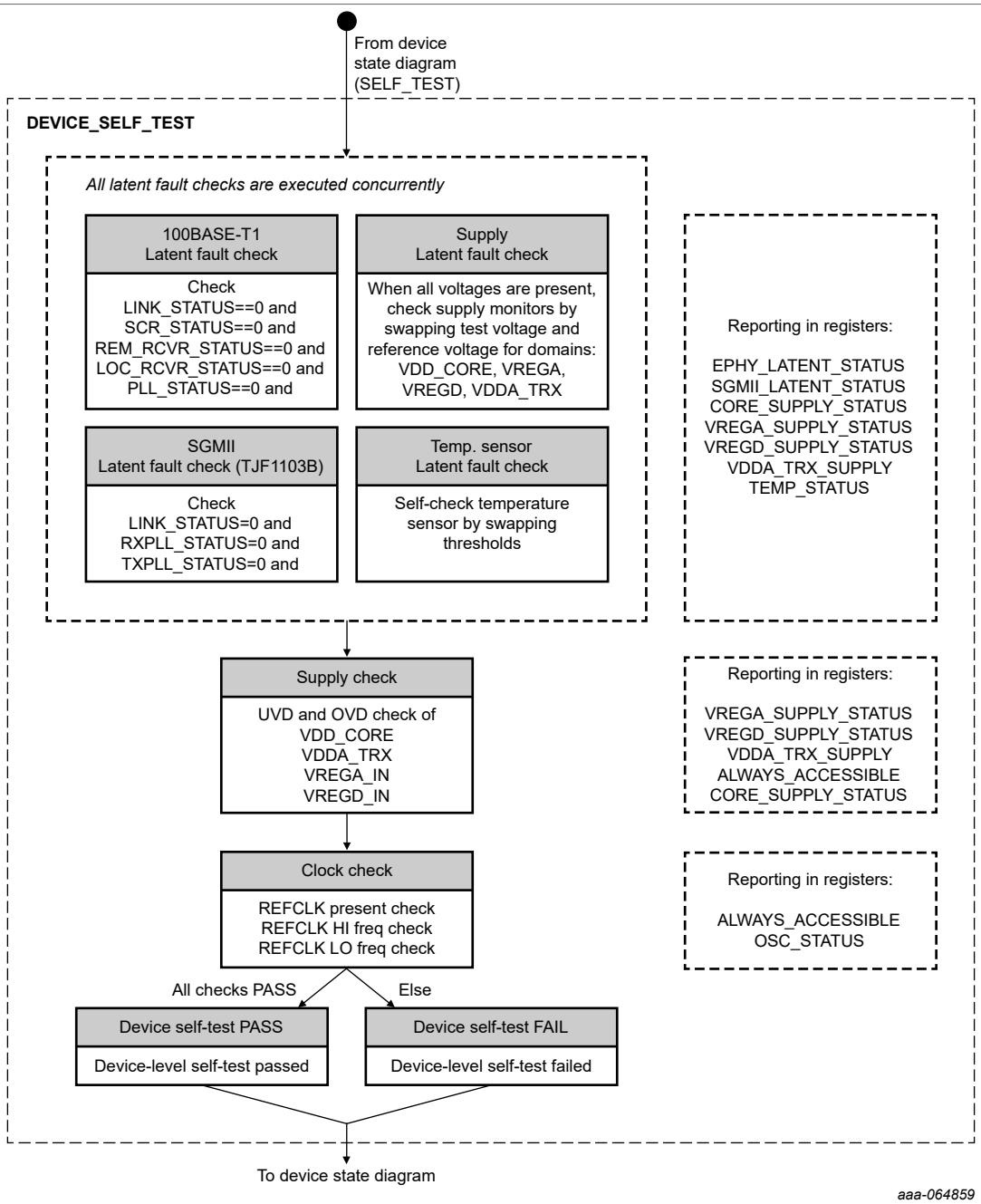


Figure 5. Device self-test sequence

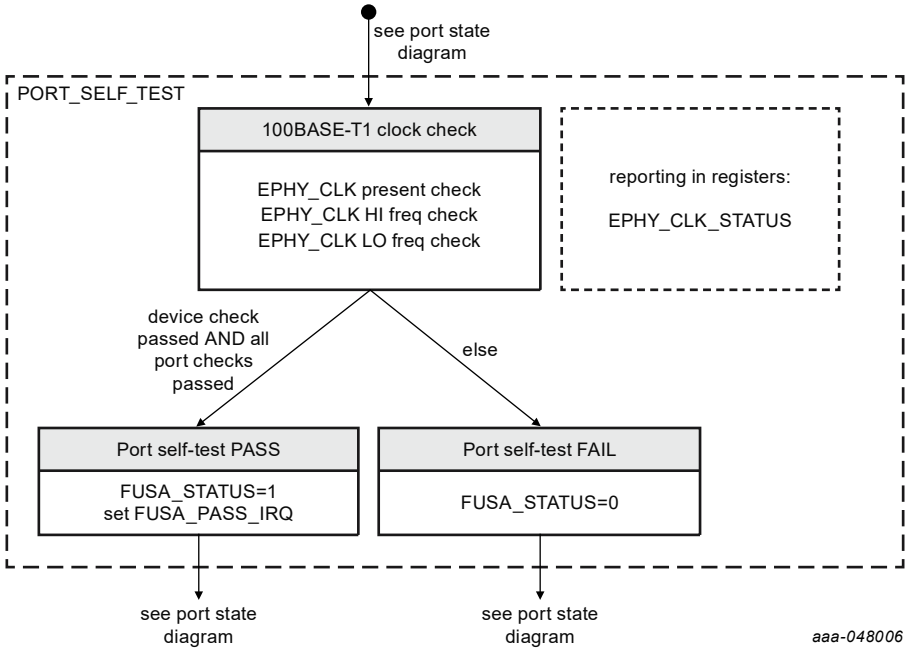


Figure 6. Port self-test sequence

6.5 xMII interfaces - TJF1103A

The TJF1103A supports a number of xMII modes that can be selected via pin strapping (see Section 6.8) and via MDIO registers.

6.5.1 MII

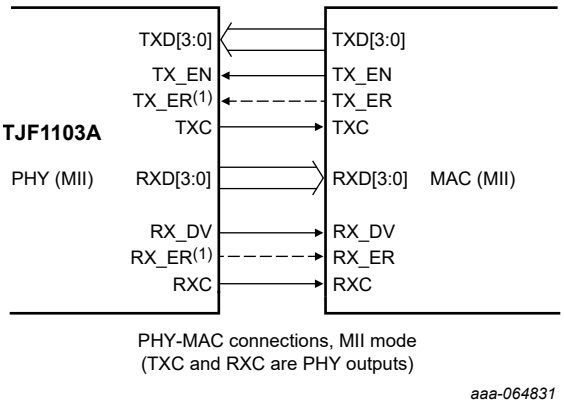
The connections between the PHY and MAC are shown in Figure 7. Data is exchanged via 4-bit wide data nibbles on TXD[3:0] and RXD[3:0]. Transmit and receive data is synchronized with the transmit (TX_CLK) and receive (RX_CLK) clocks, respectively (TXC_CLK and RXC_CLK are mapped to pins TXC and RXC on the TJF1103; see Table 8). For MII operation, the clock signals are provided by the PHY and are typically derived from an external clock or crystal (LEADER) or recovered from the MDI (FOLLOWER). Both clocks have a nominal frequency of 25 MHz (± 100 ppm). Normal data transmission from MAC to PHY is initiated by asserting TX_EN, while data reception from PHY to MAC is indicated by asserting RX_DV.

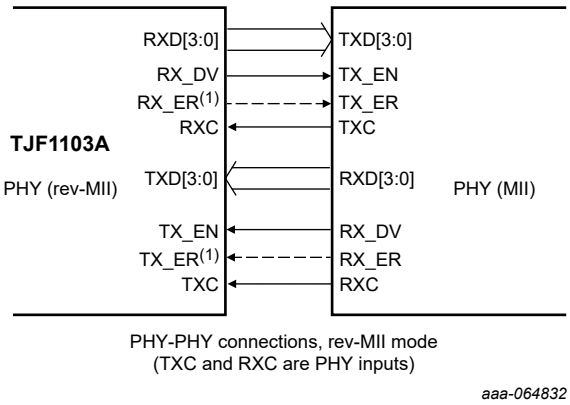
Along with MII mode, the TJF1103 supports reverse MII (rev-MII). In rev-MII mode, the PHY's MII interface acts like a MAC. In this mode TX_CLK and RX_CLK are inputs to the PHY, while the roles of TX_EN, TX_ER, TXD, RX_DV, RXD and RX_ER are unchanged. rev-MII mode can be used to connect two PHY devices for media-converter or range-extender applications.

Table 7. MII modes

MII mode[1]	Description
MII	In this mode, the device behaves as per the IEEE 802.3 MII spec with TX_CLK (mapped to TXC) and RX_CLK (mapped to RXC) as outputs
rev-MII	In this mode, the device behaves like a MAC interface as described in IEEE 802.3 MII spec. TX_CLK and RX_CLK are inputs. As in MII mode, RXD, RX_DV and RX_ER are outputs. TXD, TX_EN and TX_ER remain inputs to the TJF1103A.

[1] The MII mode is selected via pin strapping (see Section 6.8).





(1) external or internal pull-down may be needed.

Figure 7. MII interface connections

6.5.1.1 MII pinning

Mapping of MII interface pins to device pins is shown in Table 8.

Table 8. Pinning in MII-mode

MII Function	Pin	Symbol	Type[1]	Description
RX_ER	19	RX_ER/GPIO2/TDO/CONFIG1	O	receive error output; optional.[2]
RXD3	20	RXD3/GPIO3/CONFIG2	O	receive data bit 3 of RXD[3:0] nibble
RXD2	21	RXD2/GPIO4/CONFIG3	O	receive data bit 2 of RXD[3:0] nibble
RXD1	23	RXD1/CONFIG4	O	receive data bit 1 of RXD[3:0] nibble
RXD0	24	RXD0/CONFIG5	O	receive data bit 0 of RXD[3:0] nibble
RX_DV	25	RX_CTL/CONFIG6	O	receive data valid output
RX_CLK	26	RXC/GPIO8/TX_TCLK	O[3] I[4]	receive clock
TX_ER	28	TX_ER/GPIO9/TCK	I, PD	transmit error input; optional, can be left open when not used[5]
TX_CLK	29	TXC	O[3] I[4]	transmit clock
TX_EN	30	TX_CTL	I, PD	transmit data enable input
TXD0	31	TXD0	I, PD	transmit data bit 0 of TXD[3:0] nibble
TXD1	32	TXD1	I, PD	transmit data bit 1 of TXD[3:0] nibble
TXD2	33	TXD2/GPIO10	I, PD	transmit data bit 2 of TXD[3:0] nibble
TXD3	34	TXD3/GPIO11	I, PD	transmit data bit 3 of TXD[3:0] nibble

[1] I: digital input; O: digital output; IO: digital input/output; PU: weak pull-up; PD: weak pull-down
[2] GPIO2 is available when not used as MII RX_ER signal; see RXER_GPIO_SWAP (Table 249)
[3] MII mode
[4] rev-MII mode
[5] GPIO9 is available when not used as MII TX_ER signal; see TXER_GPIO_SWAP (Table 249).

6.5.2 RMII

RMII data is exchanged via 2-bit wide data dibits on TXD[1:0] and RXD[1:0], as illustrated in Figure 8. To achieve 100 Mbit/s, the data is clocked at twice the frequency used for MII. See ref.[2]

Data and control signals are synchronized to a single clock signal, REF_CLK. This 50 MHz (± 50 ppm) clock is typically input to the PHY (RMII mode). Alternatively, the PHY can output a 50 MHz REF_CLK (rev-RMII mode). rev-RMII mode can be used in PHY back-to-back configurations or with a MAC that does not provide a 50 MHz REF_CLK.

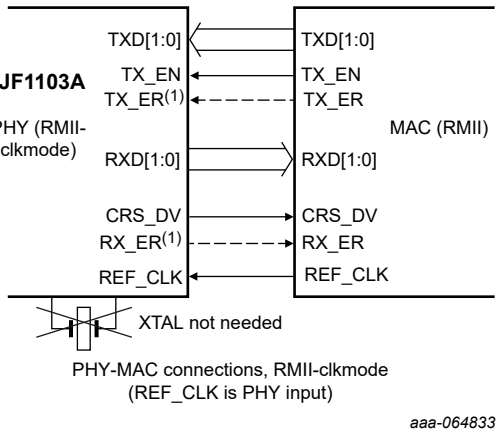
100BASE-T1 is an active-idle, full-duplex transmission scheme that does not employ the CRS signal. The CRS_DV signal is synchronized with REF_CLK and is functionally identical to RX_DV (see Section 6.5.1). When TX_EN is asserted at the start of a frame and RXD = 00, data is discarded until RXD is found to be 01. This arrangement allows the TX interface on this device to be connected to the RX interface on another PHY.

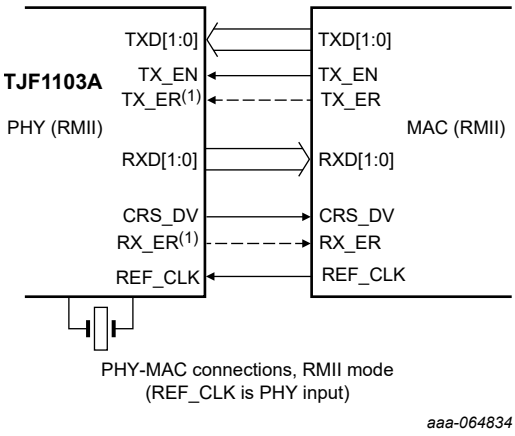
The TJF1103 supports the RMII modes detailed in Table 9.

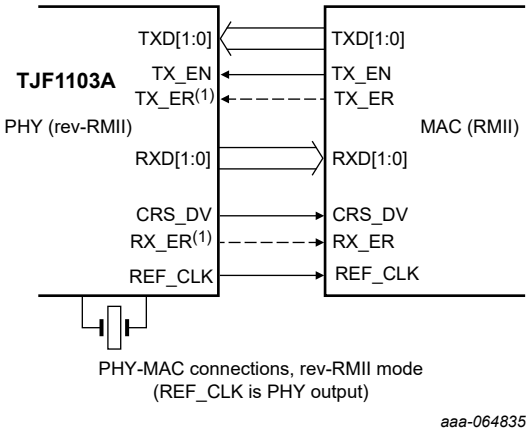
Table 9. RMII modes

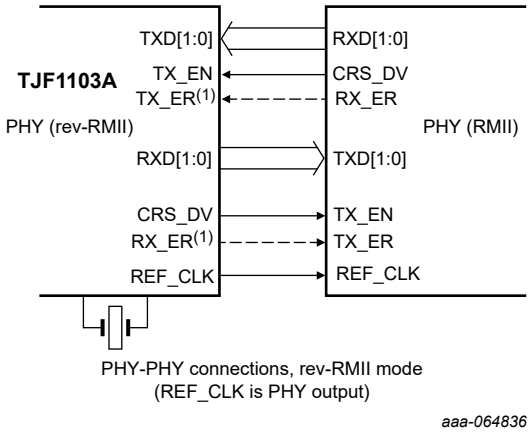
RMII mode[1]	Description
RMII	In RMII mode, REF_CLK is configured as an input and expects a 50 MHz clock.
rev-RMII	In rev-RMII mode, REF_CLK is configured as a 50 MHz clock output.
RMII-clkmode	As RMII mode, but the 50 MHz REF_CLK is used to clock the entire TJF1103 device. An external XTAL is not needed in this mode.

[1] The RMII mode is selected via pin strapping (Section 6.8).









(1) External or internal pull-down may be needed.

Note: *REF_CLK can be an input to both the MAC and the PHY.*

Figure 8. RMII signaling

6.5.2.1 RMII pinning

Mapping of RMII interface pins to device pins is shown in Table 10. Unused GPIOs can be left floating; see Section 6.16.2 for details on how to use available GPIOs.

Table 10. Pinning in RMII-mode

Function	Pin	Symbol	Type[1]	Description
RX_ER	19	RX_ER/GPIO2/TDO/CONFIG1	O	receive error output[2]
-	20	RXD3/GPIO3/CONFIG2	IO	GPIO3
-	21	RXD2/GPIO4/CONFIG3	IO	GPIO4
RXD1	23	RXD1/CONFIG4	O	receive data bit 1 of RXD[3:0] nibble
RXD0	24	RXD0/CONFIG5	O	receive data bit 0 of RXD[3:0] nibble
CRS_DV	25	RX_CTL/CONFIG6	O	carrier sense, receive data valid output
-	26	RXC/GPIO8/TX_TCLK	IO	GPIO8
TX_ER	28	TX_ER/GPIO9/TCK	I, PD	transmit error input. If unused, can be left open.[3]

Table 10. Pinning in RMII-mode...*continued*

Function	Pin	Symbol	Type[1]	Description
REF_CLK	29	TXC	O[4] I[5]	REF_CLK clock
TX_EN	30	TX_CTL	I, PD	transmit data enable input
TXD0	31	TXD0	I, PD	transmit data bit 0 of TXD[3:0] nibble
TXD1	32	TXD1	I, PD	transmit data bit 1 of TXD[3:0] nibble
-	33	TXD2/GPIO10	IO	GPIO10
-	34	TXD3/GPIO11	IO	GPIO11

[1] I: digital input; O: digital output; IO: digital input/output; PU: weak pull-up; PD: weak pull-down
[2] Optional, if not used pin GPIO2 is available; see RXER_GPIO_SWAP
[3] Optional, if not used pin GPIO9 is available; see TXER_GPIO_SWAP
[4] rev-RMII
[5] RMII

6.5.3 RGMII

RGMII PHY-MAC connections are shown in Figure 9 and ref.[3]. The RGMII protocol is intended as an alternative to the IEEE 802.3 GMII standard[2]. The objective is to reduce the number of pins between MAC and PHY in a cost-effective and technology-independent way.

Control signals are multiplexed and transmitted data is synchronized with both clock edges (double data rate). The interface is intended for 1000 Mbit/s operation, but also supports 100 Mbit/s and 10 Mbit/s data rates. This TJF1103 only supports 100 Mbit/s operation.

RGMII is a symmetrical interface. TXC is generated by the MAC and RXC is generated by the PHY. For 100 Mbit/s operation, the clock operates at 25 MHz (+/- 50 ppm) and data is duplicated on the falling edge of the appropriate clock.

RX_CTL and TX_CTL encode the RX_DV/RX_ER and TX_EN/TX_ER signals, respectively. RX_CTL/TX_CTL present the RX_DV/TX_EN signals on the rising edge and RXERR/TXERR on the falling edge. RXERR and TXERR are encoded to minimize the number of transitions during nominal data transmission.

TXERR = TX_ER xor TX_EN

RXERR = RX_ER xor RX_DV

This device implements RGMII v1.3 as well as RGMII 2.0 and ISO 21111-2 by supporting the RGMII integrated-delay option (RGMII-ID). See ref.[2] and ref.[4]

6.5.3.1 RGMII mode selection and clock delay configuration

RGMII mode, which determines the integrated delay (RXC or both RXC and TXC), can be configured via pin strapping (see Section 6.8.1).

The TXC and the RXC clock delays can be independently configured via registers RGMII_TXC_DELAY_CONFIG (Table 251) and RGMII_RXC_DELAY_CONFIG (Table 252).

Table 11. RGMII modes

RGMII mode	Description
RGMII	In RGMII mode, the interface functions according to RGMII v1.3 (no internal delay is implemented)
RGMII-ID	In RGMII-ID mode, the interface functions as per RGMII v2.0 (internal delay on RXC is enabled, no internal delay on TXC).

2 Not supported.

Table 11. RGMII modes...*continued*

RGMII mode	Description
RGMII-ID (TX/RX)	In RGMII-ID (TX/RX) mode, the interface functions as per RGMII v2.0 (internal delay on both RXC and TXC is enabled).
RGMII-ID (TX)[1]	In RGMII-ID (TX) mode, the internal delay in TXC is enabled. The delay in RXC is disabled.

[1] This mode cannot be selected via pin strapping, but only via register settings.

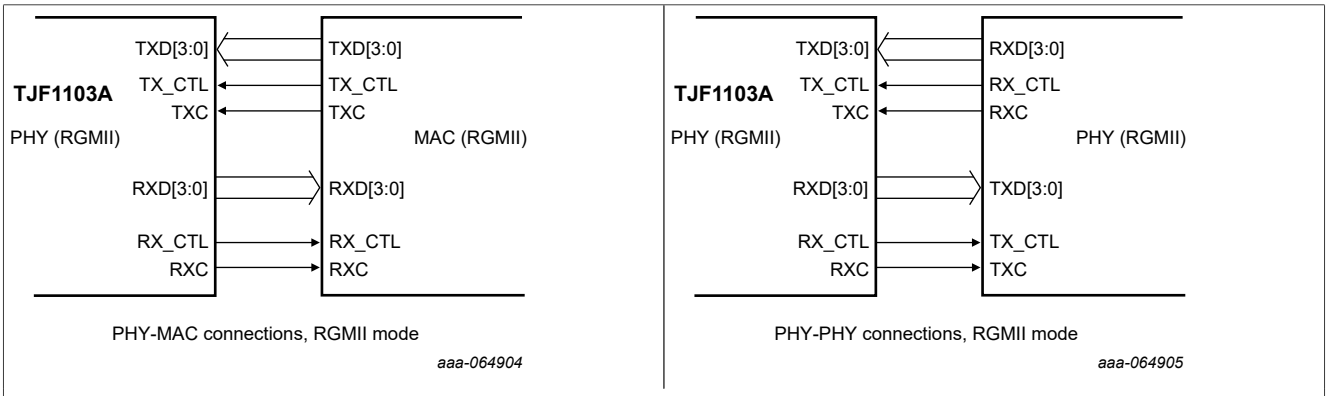


Figure 9. RGMII signaling

6.5.3.2 RGMII pinning

Mapping of RGMII interface pins to device pins is shown in Table 12. Unused GPIOs can be left floating; see Section 6.16.2 for details on how to use available GPIOs.

Table 12. Pinning in RGMII-mode

Function	Pin	Symbol	Type[1]	Description
—	19	RX_ER/GPIO2/TDO/ CONFIG1	IO	GPIO2
RXD3	20	RXD3/GPIO3/CONFIG2	O	receive data bit 3 of RXD[3:0] nibble
RXD2	21	RXD2/GPIO4/CONFIG3	O	receive data bit 2 of RXD[3:0] nibble
RXD1	23	RXD1/CONFIG4	O	receive data bit 1 of RXD[3:0] nibble
RXD0	24	RXD0/CONFIG5	O	receive data bit 0 of RXD[3:0] nibble
RX_CTL	25	RX_CTL/CONFIG6	O	receive data control output
RXC	26	RXC/GPIO8/TX_TCLK	O	receive clock
-	28	TX_ER/GPIO9/TCK	IO	GPIO9
TXC	29	TXC	I	transmit clock
TX_CTL	30	TX_CTL	I, PD	transmit data control input
TXD0	31	TXD0	I, PD	transmit data bit 0 of TXD[3:0] nibble
TXD1	32	TXD1	I, PD	transmit data bit 1 of TXD[3:0] nibble
TXD2	33	TXD2/GPIO10	I, PD	transmit data bit 2 of TXD[3:0] nibble
TXD3	34	TXD3/GPIO11	I, PD	transmit data bit 3 of TXD[3:0] nibble

[1] I: digital input; O: digital output; IO: digital input/output; PU: weak pull-up; PD: weak pull-down

6.5.4 Alternate xMII pinning

The MII, RMII and RGMII standards do not dictate the physical pin arrangement of the xMII bus.

Besides the default xMII pinning of the TJF1103A described in Section 5.1, alternate xMII pin mappings are possible. Alternate mapping is selected via bits XMII_DATA_CONFIG[TXD30_SWAP] and XMII_DATA_CONFIG[RXCTL_SELECT]. These two settings can be applied independently to allow for a more compact PCB layout with fewer or no signal swaps.

Setting bit TXD30_SWAP flips the TXD bus from TXD[3:0] to TXD[0:3]. Setting bit RXCTL_SELECT moves the RX_CTL function to the opposite side of the RXD[3:0] bus. The alternate pinning configurations are illustrated in Figure 10.

GPIO pins made available on RXD[2:3] and TXD[2:3] move accordingly.

Note: *Alternate xMII pin settings cannot be selected via pin strapping. Therefore, the RXD and TXD pins always revert to their default setting on device startup.*

Note: *The alternate pinning described in this section only applies to the TJF1103A variant.*

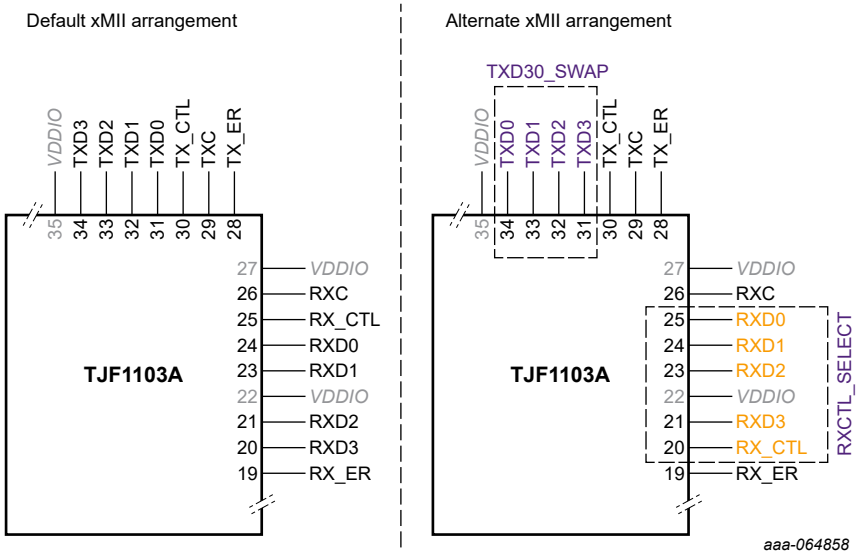


Figure 10. Default and alternate xMII pin arrangements

6.5.5 xMII elastic buffers

The xMII interface uses elasticity buffers to compensate for any divergence between 100BASE-T1 link and the xMII clocks. These buffers can compensate for rate differences of up to 100 ppm in all xMII modes. The clocking scheme, and therefore the need for buffering, depends on the selected xMII mode.

Note: *When using a crystal that exceeds the RMII and RGMII specification (50 ppm), the MAC must also be able to operate under such conditions.*

The latencies caused by these buffers are included in the overall xMII to MDI latency numbers reported in the dynamic characteristics table. For each xMII mode, Table 13 details when buffers are added in the data path and when they are bypassed.

Table 13. Elastic buffer scheme

xMII mode	TX Interface	RX Interface
RGMII[1]	enabled	bypassed
RMII[1] **/ revRMII**[1] **/ RMII-clkmode**[1]	enabled	enabled
MII[1]	bypassed	bypassed
revMII[1]	enabled	enabled

[1] TJF1103A only

6.6 SGMII interface - TJF1103B

6.6.1 Introduction

Serial-GMII (SGMII) is a SerDes interface for PHY-MAC connection (see ref.[5]). The SGMII protocol is intended as an alternative to the RGMII standard. It uses fewer interface signals and provides better EMC performance by using differential signaling.

The device contains a 4-wire SGMII interface[3] that implements clock data recovery so additional clock pairs are not needed.

The SGMII transfer rate is fixed at 1.25 GBaud. For 100 Mbit/s operation, the RX and TX interfaces elongate the frame by replicating each octet 10 times. The SGMII transmitter (SON, SOP) is enabled automatically on device startup in order to minimize time to communication.

6.6.2 Block diagram

A block diagram of the SGMII subsystem is shown in Figure 11.

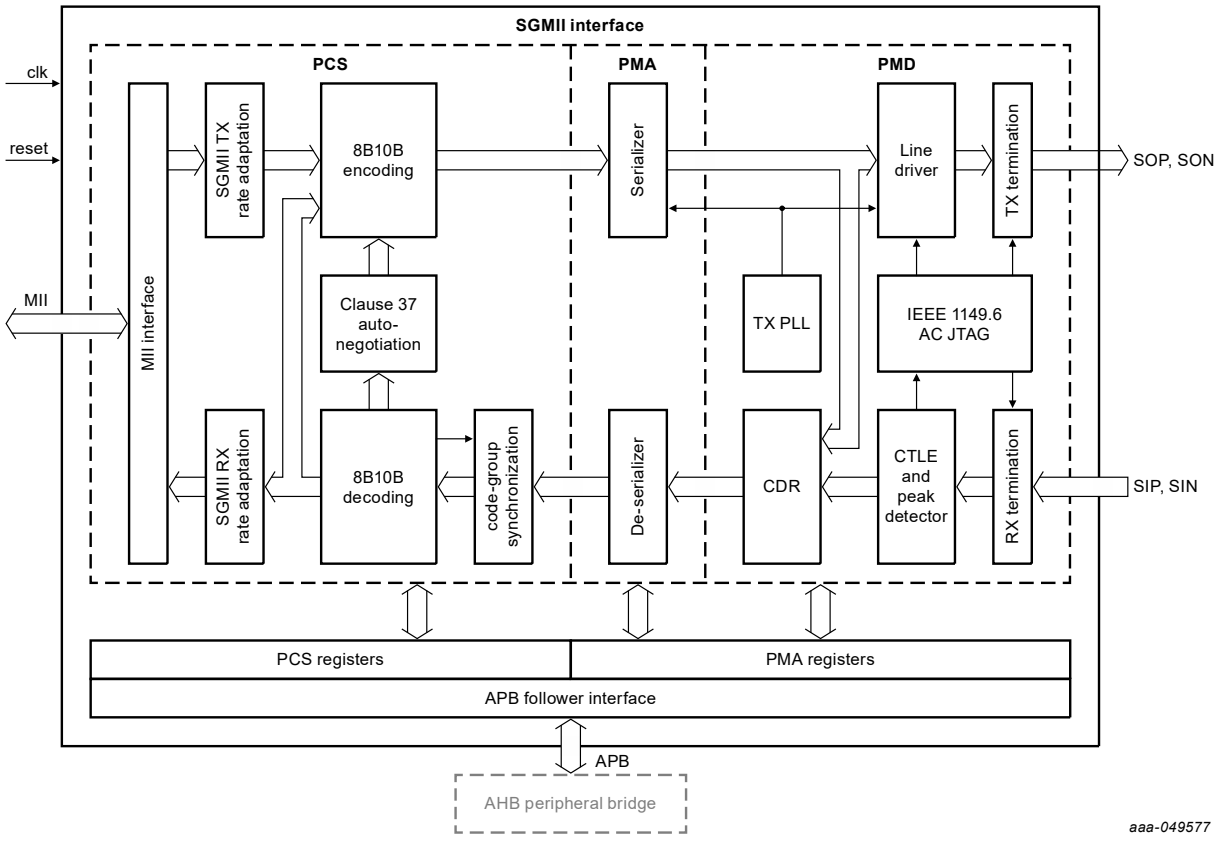


Figure 11. SGMII block diagram

6.6.3 Signaling

The SGMII block is AC-compliant with the SGMII 1.8 specification. The interface must always be AC coupled with 100 nF capacitors. The SGMII receiver input compliance mask is shown in Figure 44.

3 SGMII 8-wire interface is not supported.

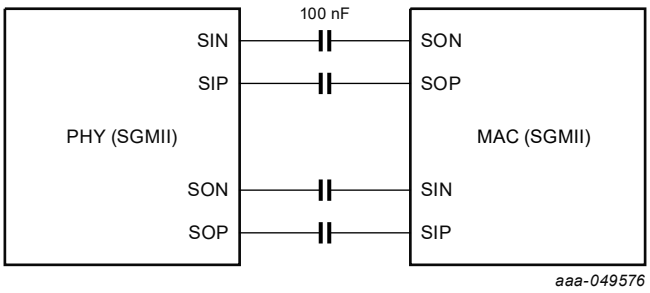


Figure 12. SGMII signaling

6.6.4 Polarity

The polarity of differential pairs SI and SO can be flipped via bits RX_POL_INV_0 and TX_POL_INV_0, respectively, in the SGMII_PCS_CONFIG1 control register (Table 274).

6.6.5 Auto-negotiation

The SGMII interface implements (optional) auto-negotation. In this mode, PHY and MAC handshake the supported interface capabilities to find the optimal operating conditions. The device advertises its speed and duplex mode (full-duplex or half-duplex).

In SGMII-PHY mode, the device communicates the link speed as well as 100BASE-T1 link availability by passing tx_config_Reg from PHY to MAC. If configured in SGMII-MAC mode, the received auto-negotiation data is ignored.

Auto-negotiation is automatically enabled and control information automatically exchanged between PHY to MAC via tx_config_Reg[15:0] as shown in Table 14. The PHY advertises the LINK_AVAILABILITY via tx_config_Reg[15]. Duplex mode and speed are fixed at full duplex and 100 Mbit/s.

Table 14. Auto-negotiation control information passed between PHY and MAC

Bit number	tx_config_Reg[15:0] sent from the PHY to the MAC	tx_config_Reg[15:0] sent from the MAC to the PHY
15	link: 1 = link up, 0 = link down	0
14	reserved for auto-negotiation acknowledge as specified in 802.3z	1
13	0	0
12	duplex mode: 1 = full duplex, 0 = half duplex	0
11:10	speed: bits 11, 10: 11 = reserved; 10 = 1000 Mbit/s 01 = 100 Mbit/s; 00 = 10 Mbit/s	0
9:1	0	0
0	1	1

6.6.6 SGMII startup procedure

After configuration and startup of the SGMII, the PCS function within the SGMII module must be powered down and restarted.

Set MMD30.SGMII_BASIC_CONTROL.LPM to 1 (30.B000h, bit 11) and then clear it to 0. No delay is required between setting and clearing the LPM bit. The SGMII_BASIC_CONTROL register is not readable while the LPM bit is asserted.

Apply the sequence after issuing the START_OPERATION command and after the device subsequently clears the START_OPERATION bit. Poll the START_OPERATION bit until the device clears it before applying the sequence. Alternatively, wait at least 1 ms after issuing the START_OPERATION command.

Apply the fix after the following events:

- Device restart (via hardware reset, software reset or power on)
- Wake-up from sleep
- Reset of the SGMII block via MMD30.SGMII_BASIC_CONTROL.RST (30.B000h.15)

Note that the device automatically asserts the START_OPERATION command in autonomous mode. It is still required to restart the PCS SGMII afterwards.

6.6.7 Mode of operation

6.6.7.1 Normal operation

During normal operation, the transmit and receive data paths of the SGMII interface are active. The transmit path accepts Ethernet data frames from the switch through the MII interfaces, applies rate adaptation for 100 Mbit/s Ethernet data, and applies 1000BASE-X 8B10B encoding. After serialization, the data is driven onto the physical medium by the line driver. The line driver has an on-chip transmitter termination for good impedance matching with the medium. The TXPLL generates the half-bitrate clock needed for serializing the data. The chip-internal MII interface clocks are derived from the clock generated by the TXPLL.

The receive path receives a serial data stream from the physical medium, to which it provides an impedance match with the on-chip receiver termination. The CTLE equalizes the received signals to compensate for channel losses, before recovering the clock and data from the serial stream by the CDR. The recovered data is deserialized before aligning and decoding 8B10B code groups. Finally, rate adaption is applied for 100 Mbit/s Ethernet data before making the data frames available to the on-chip MII interface.

The interface starts autonomously in Normal mode. When the interface is in standby state, setting bit START_OPERATION in the SGMII_ADVANCED_CONTROL register (Table 265) transitions the interface to Normal mode.

6.6.7.2 Standby

The SGMII interface can be disabled by setting bit GOTO_STANDBY in the SGMII_ADVANCED_CONTROL register (Table 265).

6.6.7.3 PCS loopback

The on-chip PCS RX-to-TX loopback is an operating mode in which the received data is not applied by the PCS to the MII interface but is instead applied to the transmit path of the PCS. In this operating mode, the SGMII interface effectively sends the serial data stream, received from the SGMII link partner, back to the link partner over the transmitter data path.

6.6.7.4 PMA loopback

The on-chip PMA TX-to-RX loopback is an operating mode in which the serial data stream on the transmit path is not provided to the line driver but is instead looped back to the CDR. The CDR, in turn, does not receive the serial data from the SGMII link partner, through the CTLE, but instead recovers it from the serializer on the transmit path.

6.6.8 Boundary scan

In boundary scan mode, the SGMII interface is used to perform AC-JTAG operations to test the interconnections between the SGMII interface and other ICs for manufacturing defects.

6.7 MDIO

The MDIO interface is a management interface used to control the device through a two-wire shared bus. Individual PHYs are selected through a PHYAD identifier, configured via pin strapping. This device supports up to 27 addresses, see Section 6.8.1.

Note: *PHYAD zero is reserved and cannot be assigned. Optionally, the device can listen on PHYAD zero for broadcast read/writes.*

There are two versions of the MDIO protocol, IEEE 802.3 Clause 22 and IEEE 802.3 Clause 45. The earlier Clause 22 standard allows up to 32 registers to be accessed in up to 32 PHY devices. The more recent Clause 45 standard allows access to up to 65,536 registers per PHY per MMD. The TJF1103 supports both MDIO protocols, but only Clause 45 provides a full view on all registers, see Section 6.7.5 and Section 6.7.4.

Frame formats of both standards are illustrated in Section 6.7.2 and Section 6.7.1.

Note: *Do not interleave Clause 22 access with Clause 45 access. Use either Clause 22 or Clause 45 exclusively.*

A typical MDIO topology is shown in Figure 13.

Note: *The TJF1103 does not have integrated pull-up or pull-down resistors on MDIO or MDC.*

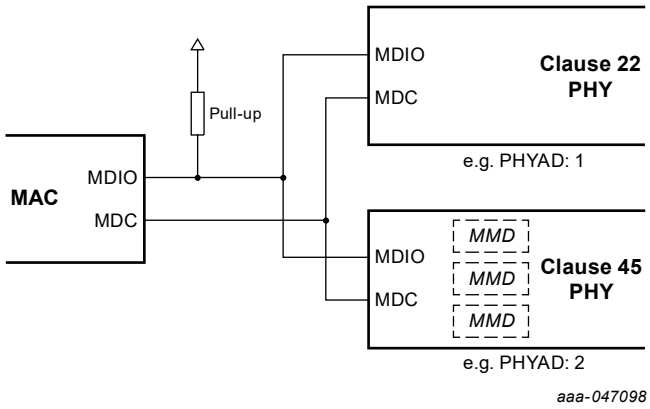
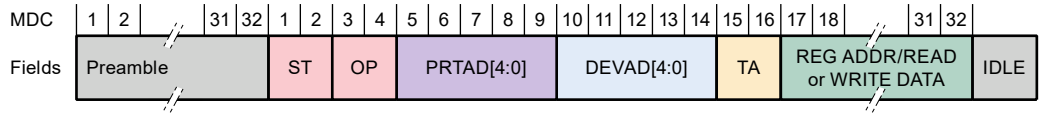


Figure 13. MDIO signaling

6.7.1 IEEE 802.3 Clause 45

Figure 14 shows the IEEE Clause 45 frame format and access types.



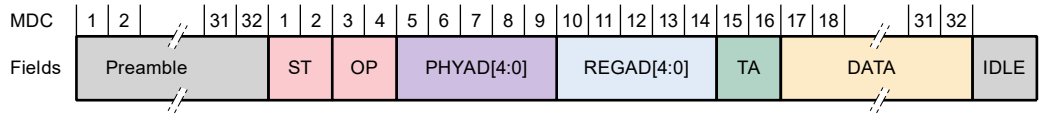
	Management frame fields							
	PRE	ST	OP	PRTAD	DEVAD	TA	ADDRESS/DATA	IDLE
Address	1...1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Post-read-increment-address	1...1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

aaa-047099

Figure 14. Clause 45 frame format and access types

6.7.2 IEEE 802.3 Clause 22

Figure 15 shows the IEEE Clause 22 frame format and access types.



	Management frame fields							
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Read	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

aaa-047100

Figure 15. Clause 22 frame format and access types

6.7.3 MDIO broadcast

The TJF1103 supports MDIO broadcast functionality, which is disabled by default. When enabled, the TJF1103 responds on a configurable PHY address (by default PHYADR 0) to read and write requests.

This feature is enabled by setting bit BROADCAST_ENABLE in the SMI_CONFIG register (Table 91).

6.7.4 Clause 45 MMD register organization

The TJF1103 supports 3 MMDs:

- PMA (MMD 01)
- PCS (MMD 03)
- NXP vendor specific (MMD 30)

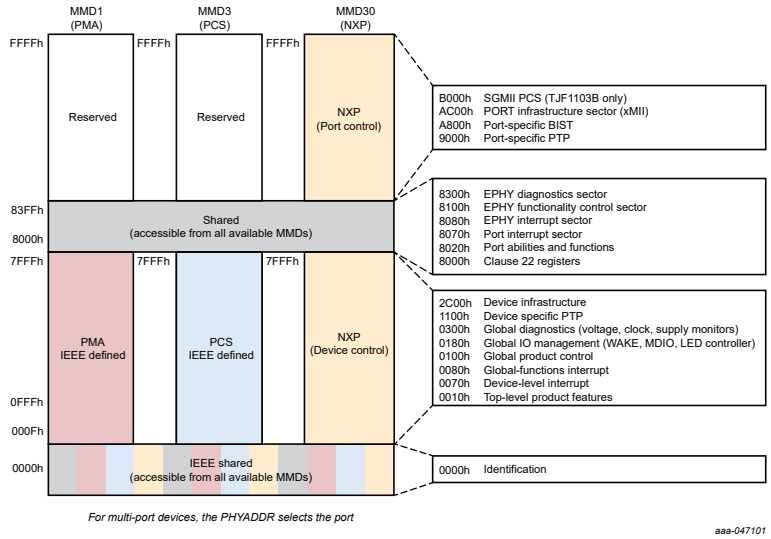


Figure 16. MMD organization

The lower parts of MMD 1 and MMD 3 follow the IEEE 802.3 specification for PMA and PCS devices. The lower part of MMD 30 contains device and global control registers (e.g. LED, GPIO). The higher part of MMD 30 is used to configure port-related functions.

Note: *The register organization separates port from device control in order to support multi-port devices (not used in the TJF1103).*

Common functionality is mapped into all MMDs (see Shared section in Figure 16). In this sense, the shared MMD is not a real MMD. The shared registers are mapped into ranges 0000h to 001Fh and 8000h to 83FFh.

Standard Clause 22 registers are mapped in the vendor-specific register space of all MMDs from 8000h to 801Fh.

6.7.5 Clause 22 register organization

The device implements limited Clause 22 access as detailed in Section 7.1, which are the only registers directly accessible through IEEE Clause 22 and IEEE Clause 45 type transactions. Note that the C22 registers are not exclusive to IEEE Clause 22 accesses.

CL22 registers are composed of:

- PHY identification registers.
- FAVORITE_IRQS, which contains common IRQs. This register can be used to shortcut the IRQ tree.
- IEEE Clause 45 indirection registers, used if the MAC does not support Clause 45 MDIO.
- ALWAYS_ACCESSIBLE register, which is the only register accessible in the absence of VDD_CORE. VDDIO and VDDA_AO must be present to access this register.

The CL22 register overview table (Table 30) lists the register offsets as mapped into Shared MMD Clause 45 space.

Note: *The addresses contained in the CL22 register overview table cannot be used directly for IEEE Clause 22 MDIO access. Table 30 lists the register offsets as mapped into Shared MMD Clause 45 space. When accessing these registers through a physical Clause 22 transaction, 8000h must be subtracted from the offset. For example, PHY_ID_1 is located at 2h and ALWAYS_ACCESSIBLE at 1Fh.*

Note: *Do not interleave Clause 22 with Clause 45 accesses. Use Clause 22 or Clause 45 exclusively. Consult the application note for additional information (ref.[6]).*

6.8 Pin strapping

6.8.1 Configuring pin strapping

The TJF1103 uses pin strapping to configure critical configuration data at device start-up or reset. For this, the CONFIG pins on the device support a 3-level strapping that is sensed after device reset (power-on reset, RST_N pin or reset register). Other than PHYAD and JTAG mode, configuration parameter values can be changed at any time over MDIO.

During sampling, the CONFIG pin settings must not be overruled by the microcontroller. This can be achieved if:

- The RX interface of the xMII microcontroller pins is high-ohmic during the initialization phase (recommended) or
- The RX interface of the xMII microcontroller pins is actively driven and is logically consistent with the specified pin strapping or
- The RST_N pin is not released until the relevant microcontroller pins have been configured as inputs (high-ohmic).

Pull-up and pull-down configurations are shown in Figure 17. Care must be taken if a CONFIG pin is used to drive loads that pull in the opposite direction to the configuration resistor. For LEDs, the polarity can be selected to match the direction of the configuration resistor. In the case of negative LED polarity (as shown in the pull-down case), the polarity of the LED driver must be adjusted via software.

The pin strapping sequence will have latched the configuration within 3 ms after RST_N has been deasserted.

Table 15. 3-Level strap resistor values

Strap Setting	R_{pu}	R_{pd}
O	OPEN	OPEN
H	10 kΩ	OPEN
L	OPEN	10 kΩ

Note: *The sum of all resistances on a CONFIG pin must be greater than 145 kΩ in order to be reliably detected as O (OPEN).*

Note: *See the application note ref.[6] for layout guidelines.*

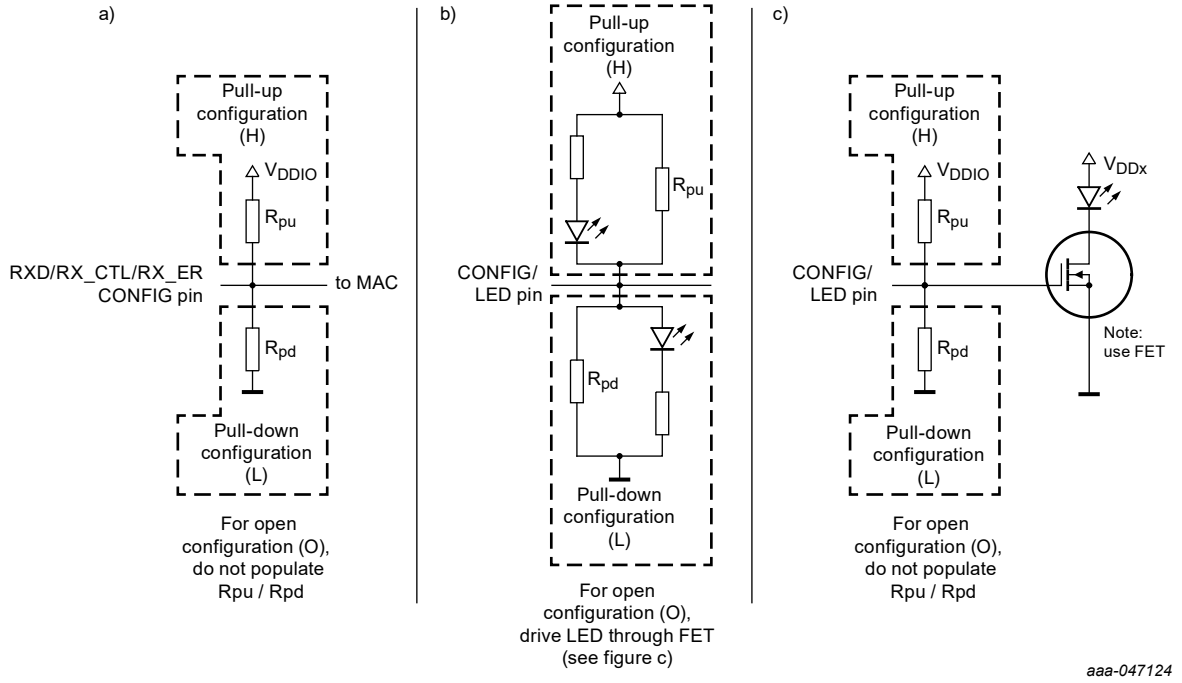


Figure 17. Pin strap configurations

6.8.2 Configuration options

The available CONFIG pins are grouped to configure xMII mode, the PHYAD and miscellaneous settings.

Table 16. MODE group

xMII MODE (TJF1103A)	xMII MODE (TJF1103B)	Pin CONFIG3	Pin CONFIG4
RGMII-ID (RXC)	SGMII-PHY	O	O
RGMII	SGMII-MAC	O	H
RGMII-ID (both TXC/RXC)	*reserved*	O	L
RMII	*reserved*	H	O
RMII-clkmode	*reserved*	H	H
RMII-rev	*reserved*	H	L
MII	*reserved*	L	O
MII-rev	*reserved*	L	H
JTAG	JTAG	L	L

Table 17. PHYAD group

PHYAD	Pin CONFIG0	Pin CONFIG1	Pin CONFIG2
1	H	H	H
2	H	H	L
3	H	H	O
4	H	L	H

Table 17. PHYAD group*...continued*

PHYAD	Pin CONFIG0	Pin CONFIG1	Pin CONFIG2
5	H	L	L
6	H	L	O
7	H	O	H
8	H	O	L
9	H	O	O
10	L	H	H
11	L	H	L
12	L	H	O
13	L	L	H
14	L	L	L
15	L	L	O
16	L	O	H
17	L	O	L
18	L	O	O
19	O	H	H
20	O	H	L
21	O	H	O
22	O	L	H
23	O	L	L
24	O	L	O
25	O	O	H
26	O	O	L
27	O	O	O

Table 18. Miscellaneous group

LEADER/FOLLOWER	AUTONOMOUS Mode	Polarity Correction	Pin CONFIG5	Pin CONFIG6
LEADER	enabled	enabled	O	O
LEADER	disabled	enabled	O	H
FOLLOWER	enabled	enabled	O	L
FOLLOWER	disabled	enabled	H	O
LEADER	enabled	disabled	H	H
LEADER	disabled	disabled	H	L
FOLLOWER	enabled	disabled	L	O
FOLLOWER	disabled	disabled	L	H
reserved	*reserved*	*reserved*	L	L

6.9 Reconfiguration

Writing to the configuration registers is disabled by default to prevent registers being reconfigured unintentionally. It must be enabled to allow the configuration to be changed. Multiple, hierarchical CONFIG_ENABLE switches are provided.

Table 19 and Table 20 provide an overview of the registers that are protected in the TJF1103A and TJF1103B, respectively, and how they are protected.

A single device configuration enable bit (SUPER_CONFIG_ENABLE) enables all reconfiguration options. Device configuration usually happens after power-on as part of the software initialization routine. However, PHY reconfiguration is possible at any time.

Registers not listed in this table are not write-protected for reconfiguration.

Table 19. Reconfiguration-protected registers in TJF1103A

Level 1	Level 2	Level 3	Protected registers
MMD30.DEVICE_CONTROL[SUPER_CONFIG_ENABLE]			
	MMD30.DEVICE_CONTROL[GLOBAL_CONFIG]		
			MMD30.DEVICE_CONFIG
			MMD30.WISE_CONFIG
			MMD30.WISE_PARAMETERS
			MMD30.SMI_CONFIG
	MMD30.GLOBAL_INFRA_CONTROL[CONFIG_ENABLE]		
			MMD30.GPIO0_FUNC_CONFIG - MMD30.GPIO11_FUNC_CONFIG
			GPIO_IO_CLK_CONFIG
	MMD30.PORT_CONTROL[CONFIG_ENABLE]		
			MMD30.PORT_FUNC_ENABLE
		Shared.PHY_CONTROL[CONFIG_ENABLE]	
			MMD1.BASE_T1_PMA_CONTROL
			MMD1.E100BT1_PMA_TEST_CONTROL
			SharedMMD.PHY_CONFIG
			SharedMMD.PHY_PARAMETERS
			SharedMMD.WAKE_SLEEP_CONFIG
			SharedMMD.WAKE_SLEEP_PARAMETERS
			SharedMMD.PHY_COMPLIANCE_TEST
		MMD30.PORT_BIST_CONTROL[CONFIG_ENABLE]	
			MMD30.BIST_INTERCEPT_CONFIG
		MMD30.PORT_INFRA_CONTROL[CONFIG_ENABLE]	
			MMD30.INFRA_CONFIG
			MMD30.MII_BASIC_CONFIG
			MMD30.XMII_CLK_CONFIG

Table 19. Reconfiguration-protected registers in TJF1103A*...continued*

Level 1	Level 2	Level 3	Protected registers
			MMD30.XMII_CLK_IO_CONFIG
			MMD30.XMII_DATA_CONFIG
			MMD30.XMII_DATA_IO_CONFIG
			MMD30.RGMII_RXC_DELAY_CONFIG
			MMD30.RGMII_TXC_DELAY_CONFIG
			MMD30.RX_PREAMBLE_COUNT
			MMD30.TX_PREAMBLE_COUNT
			MMD30.RX_IPG_LENGTH
			MMD30.TX_IPG_LENGTH

Table 20. Reconfiguration-protected registers in TJF1103B

Level 1	Level 2	Level 3	Protected registers
MMD30.DEVICE_CONTROL[SUPER_CONFIG_ENABLE]			
	MMD30.DEVICE_CONTROL[GLOBAL_CONFIG]		
			MMD30.DEVICE_CONFIG
			MMD30.WISE_CONFIG
			MMD30.WISE_PARAMETERS
			MMD30.SMI_CONFIG
			MMD30.PORT_FUNC_ENABLES
	MMD30.GLOBAL_INFRA_CONTROL[CONFIG_ENABLE]		
			MMD30.GPIO0_FUNC_CONFIG - MMD30.GPIO11_FUNC_CONFIG
			GPIO_IO_CLK_CONFIG
	MMD30.PORT_CONTROL[CONFIG_ENABLE]		
		Shared.PHY_CONTROL[CONFIG_ENABLE]	
			MMD1.BASE_T1_PMA_CONTROL
			MMD1.E100BT1_PMA_TEST_CONTROL
			SharedMMD.PHY_CONFIG
			SharedMMD.PHY_PARAMETERS
			SharedMMD.WAKE_SLEEP_CONFIG
			SharedMMD.WAKE_SLEEP_PARAMETERS
			SharedMMD.PHY_COMPLIANCE_TEST
		MMD30.PORT_BIST_CONTROL[CONFIG_ENABLE]	
			MMD30.BIST_INTERCEPT_CONFIG
		MMD30.PORT_INFRA_CONTROL[CONFIG_ENABLE]	

Table 20. Reconfiguration-protected registers in TJF1103B*...continued*

Level 1	Level 2	Level 3	Protected registers
			MMD30.INFRA_CONFIG
		MMD30.SGMII_ADVANCED_CONTROL[CONFIG_ENABLE]	
			MMD30.SGMII_ADVANCED_CONFIG

6.10 Test protection

Test functions are disabled by default to prevent unintentional interference with normal PHY operations. As with reconfigration (see Section 6.9), test functions need to be enabled before they can be executed. Multiple hierarchical TEST_ENABLE switches are provided.

Table 21 provides an overview the registers that are protected, and how they are protected.

Table 21. Test function-protected registers

Level 1	Level 2	Level 3	Protected registers
MMD30.DEVICE_SUPER_TEST_ENABLE[1]			
	Shared.PORT_FUNC_ENABLES.TEST_ENABLE[1]		
			MMD30.BIST_GEN_CTRL.BIST_GEN_EN
			MMD30.BIST_CHECK_CTRL.BIST_CHECKER_EN
		Shared.PHY_CONFIG.TEST_ENABLE[1]	
			MMD1.E100BT1_PMA_TEST_CONTROL.PMA_TEST_MODE
		MMD30.INFRA_CONFIG.TEST_ENABLE[1]	
			MMD30.XMII_CONTROL.MAC_LOOPBACK
	MMD30.DEVICE_CONFIG.TEST_ENABLE[1]		
			MMD30.COMPL_TEST_INTF
			Shared.PHY_COMPLIANCE_TEST.TX_TCLK_EN

[1] Associated configuration enable bit (CONFIG_ENABLE; see Section 6.9) may need to be set before TEST_ENABLE settings can be changed.

6.11 Polarity detection/correction

When the 100BASE-T1 PHY is in FOLLOWER mode, it can automatically detect and flip the MDI polarity (polarity detection and correction). This feature can be enabled/disabled via pin strapping. It can also be disabled by setting bit POLARITY_CORRECT_DISABLE in the PHY_CONFIG register (Table 310).

The MDI polarity can be swapped by setting register bit POLARITY_SWAP in the PHY_CONFIG register (Table 310). When set, pins TRX_P and TRX_M are swapped and polarity detection and correction operate on the swapped pinning.

The status of polarity inversion is indicated by bit DETECTED_POLARITY in the PHY_STATUS register (Table 307). If polarity correction is disabled, bit DETECTED_POLARITY flags a conflict between actual signal polarity and current MDI polarity. In this case, bit POLARITY_SWAP should be inverted.

A polarity conflict is also signaled via an IRQ in the EPHY_FUNCTIONAL_IRQ_SOURCE group; see Section 6.13. Polarity can be changed in LEADER mode.

6.12 Diagnosis

6.12.1 Link up/status

A number of flags are used to capture link up.

Bit LINK_AVAILABLE is asserted when the following flags in the PHY_STATUS register (Table 307) are set:

- SENDN_OR_DATA
- REM_RCVR_STATUS
- SCRAMBLER_STATUS
- LINK_STATUS
- LOC_RCVR_STATUS

Glitches can be filtered with hysteresis. The hysteresis is configured via bit LINK_AVAILABLE_HYST_TIME in the PHY_PARAMETERS table (Table 312). LINK_AVAILABLE_HYST_TIME = 0 corresponds to the compliance 'link up condition'. This signal is then identical to communication ready (comm_ready) as defined in the OPEN Alliance specification.

The SENDN_OR_DATA status bit indicates whether the PHY control state machine is in SEND_IDLE_OR_DATA state.

The LINK_STATUS bit indicates whether the link status from the Link Monitor FSM is set.

The RECEIVE_LINK_STATUS (Table 40) flag indicates if the PMA/PMD receive link is up. This flag is latched LOW.

Note: *It is recommended to use the LINK_AVAILABLE flag in the PHY_STATUS register (Table 307) as a link state indicator.*

Note: *It is not possible to obtain the link status on a GPIO/LED output with the accuracy required by PHY-C Test 4.1.4.a.*

6.12.2 SQI

The signal quality indicator (SQI) is in the SIGNAL_QUALITY register (see Table 327). The SQI field determines the link quality between values 0 (worst, no-link) and 7 (best). The SQI value is only valid if bit VALID in the SIGNAL_QUALITY register is set. Assuming gaussian noise, an SQI level of 3 or more indicates a BER of 10^{-10} or better.

In addition to the current SQI value, the lowest observed SQI value is stored in SIGNAL_QUALITY[SQI_WORST]. SIGNAL_QUALITY[SQI_WORST] is cleared on being read and set to the current SQI value. In order to avoid extensive SQI polling, an SQI threshold level can be defined. If this threshold is exceeded, an IRQ (EPHY_DIAGNOSTIC_IRQ_MSTATUS[SQI_WARN]) is asserted. The threshold is configured via SIGNAL_QUALITY[SQI_WARN_LIMIT].

6.12.3 MSE

The mean square error is captured after channel equalization has removed ISI, echo and attenuation effects. The MSE metric captures signal distortion caused by uncorrelated noise and interference. The MSE is captured after setting bit ENABLE in the MSE register (Table 328).

The 8-bit MSE value read from the register is scaled by 1024. To derive the mean square error in units of V^2, it must be divided by 1024. The resulting value is between 0.0 V^2 (best) and 0.25 V^2 (worst). The root mean square error can be derived as follows:

$$RMSE = \sqrt{\frac{MSE}{1024}}\ V_{rms} \quad (1)$$

6.12.4 Test modes

100BASE-T1 PHY specification supports four test modes according to IEEE Std 802.3, Clause 96 ref.[1].

These test modes are used for transmitter waveform, distortion, jitter and droop testing. A test mode is selected via bit PMA_TEST_MODE in the E100BT1_PMA_TEST_CONTROL register (Table 49).

Note: *Before entering a test mode, re-configuration and testing must be enabled by setting, respectively, bit CONFIG_ENABLE in the PHY_CONTROL register (Table 306) and bit TEST_ENABLE in the PHY_CONFIG register (Table 310).*

6.12.4.1 Test mode 1

Test mode 1 is used to test transmitter droop. In Test mode 1, the PHY transmits '+1' symbols for 600 ns followed by '–1' symbols for a further 600 ns. This sequence is repeated continuously.

6.12.4.2 Test mode 2

Test mode 2 is used to test transmitter timing jitter in LEADER or FOLLOWER configuration. In test mode 2, the PHY transmits data symbol sequence {+1, –1} repeatedly. The transmission of the symbols is synchronized with the local external oscillator in LEADER mode and with the recovered receiver clock in FOLLOWER mode.

6.12.4.3 Test mode 4

Test mode 4 is used to test transmitter distortion. In test mode 4, the PHY transmits the sequence of symbols generated by the scrambler polynomial $gs_1 = 1 + x^9 + x^{11}$.

The bit sequence x0n, x1n is derived from the scrambler according to the following equations:

x0n = Scrn[0]

x1n = Scrn[1] XOR Scrn[4]

This stream of 3-bit nibbles is mapped to a stream of ternary symbols according to Table 22.

Table 22. TestMode 4 ternary symbol mapping

X1n	X0n	PAM-3 Transmit Symbol
0	0	0
0	1	+1
1	0	0
1	1	–1

6.12.4.4 Test mode 5

Test mode 5 is used to test the transmit PSD mask. In test mode 5, the PHY transmits a random sequence of PAM-3 symbols. In this mode, the PHY is forced to LEADER mode as per IEEE 802.3

6.12.4.5 Recovered clock (TCLK)

The recovered clock can be output on GPIO8. To enable TCLK, the following registers must be configured:


```
PHY_CONTROL[CONFIG_ENABLE] = 1
  PHY_COMPLIANCE_TEST[TX_TCLK_EN] = 1

DEVICE_CONTROL[GLOBAL_CONFIG_ENABLE] = 1
  DEVICE_CONFIG[TEST_ENABLE] = 1

  // Activate the test interface
  COMPL_TEST_INTF[TEST_INTF_EN] = 1
  COMPL_TEST_INTF[FUNC_SEL] = b0001
  COMPL_TEST_INTF[COMPL_TCLK_EN] = 1
```

The indentations in the first two entries indicate that the associated CONFIG_ENABLE bits need to be set before the settings can be changed.

6.12.5 Loopback

The device supports the following loopback modes:

- PMA local loopback
- PMA remote loopback
- PCS loopback
- xMII PHY loopback
- xMII MAC loopback

6.12.5.1 PMA local loopback

In PMA loopback mode, the PMA receive function utilizes the echo signals from the unterminated MDI. It decodes these signals to pass the data back to the MII Receive Interface as shown in Figure 18.

The MAC can compare the packets sent through the MII transmit function with the packets received from the MII receive function to validate PCS and PMA functions.

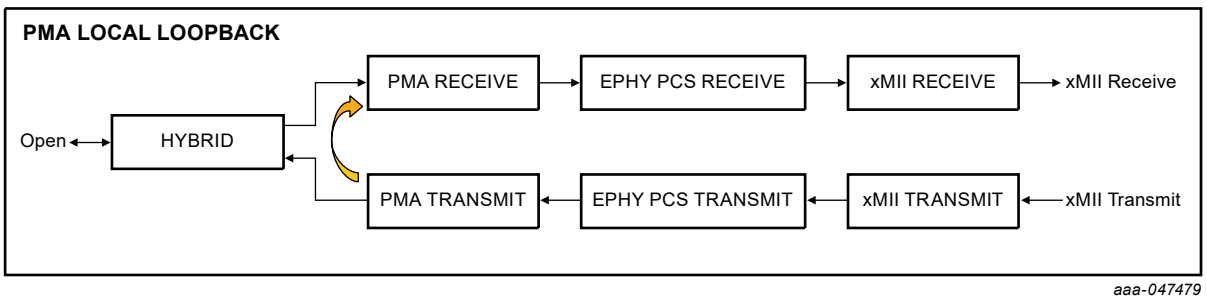


Figure 18. PMA local loopback

PMA local loopback is enabled by setting bit LOCAL_LOOPBACK in the MMD1.PMA_CONTROL1 register (Table 39). The PHY can be in any PHY_MODE (LEADER or FOLLOWER). Data can be sent once the following flags in MMD30.PHY_STATUS (Table 307) are set:

- LINK_AVAILABLE
- SENDN_OR_DATA
- REM_RCVR_STATUS
- SCR_STATUS
- LINK_MONITOR_STATUS
- LOC_RCVR_STATUS

Note: *PCS loopback overrules PMA loopback.*

6.12.5.2 PMA remote loopback

In PMA remote loopback mode, the data transmitted by the link partner on the MDI is mirrored back to the link partner. The received symbols are passed through the PMA receive and PCS receive functions, forwarded to the PCS transmit function, which in turn sends it back to the link partner.

PMA remote loopback allows the MAC to compare the packets sent to the MDI with the packets received back from the MDI and, therefore, to validate the functionality of the physical channel, including both 100BASE-T1 PHYs.

PMA remote loopback is enabled by setting bit REMOTE_LOOPBACK in the MMD1.PMA_CONTROL1 register (Table 39).

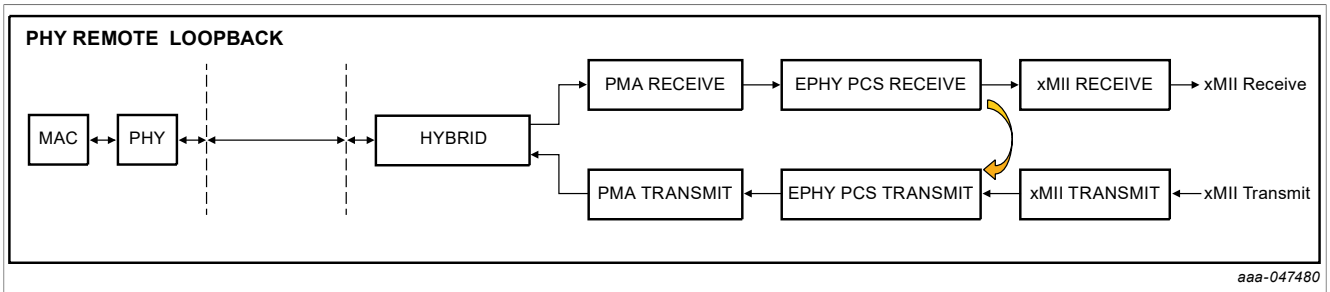


Figure 19. PMA remote loopback

6.12.5.3 PCS loopback

In PCS loopback mode, the PCS receive function gets ternary symbols An and Bn directly from the PCS transmit function as shown in Figure 20. The xMII receive data is transmitted through the PCS subsystem and mirrored to the xMII Transmit interface.

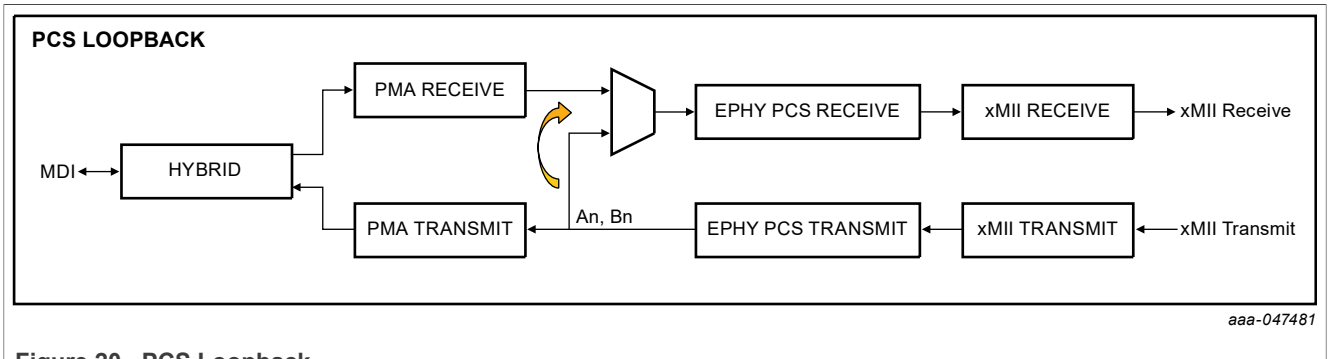


Figure 20. PCS Loopback

PCS loopback is enabled by setting bit LOOPBACK in the MMD3.PCS_CONTROL1 register (Table 51). Data can be sent once the following flags in MMD30.PHY_STATUS (Table 307) are set:

- LINK_AVAILABLE

- SENDN_OR_DATA
- REM_RCVR_STATUS
- SCR_STATUS
- LINK_MONITOR_STATUS
- LOC_RCVR_STATUS

6.12.5.4 xMII PHY loopback

In xMII PHY loopback mode, the frames received by the link partner at the MDI are passed through the PMA receive and PCS receive functions and forwarded to the xMII transmit function, which in turn sends it back to the link partner from where it came.

xMII PHY loopback allows the MAC to compare the packets sent to the MDI with the packets received back from the MDI and, therefore, to validate the functionality of the physical channel, both 100BASE-T1 PHYs and the xMII function including rate matching FIFOs.

xMII PHY loopback is enabled by setting bit PHY_LOOPBACK in the XMII_CONTROL register (Table 242).

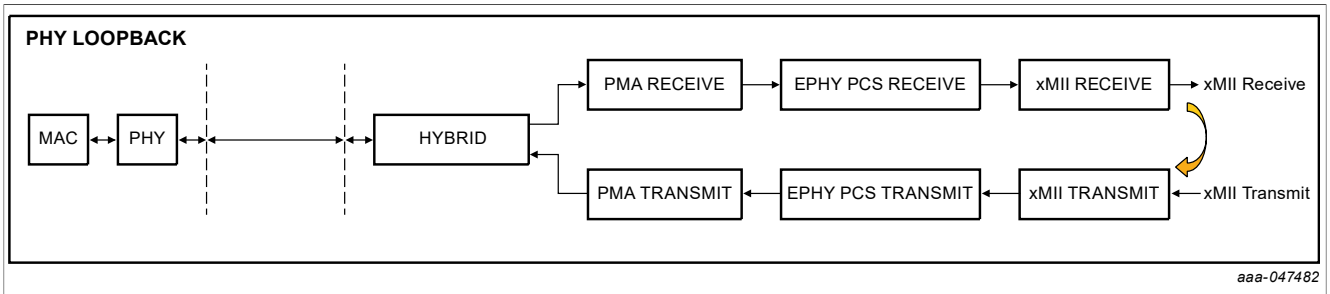


Figure 21. xMII PHY loopback

6.12.5.5 xMII MAC loopback

xMII MAC loopback is similar to PCS loopback, but with loopback directly at the xMII interface.

xMII MAC loopback is enabled by setting bit MAC_LOOPBACK in the XMII_CONTROL register (Table 242).

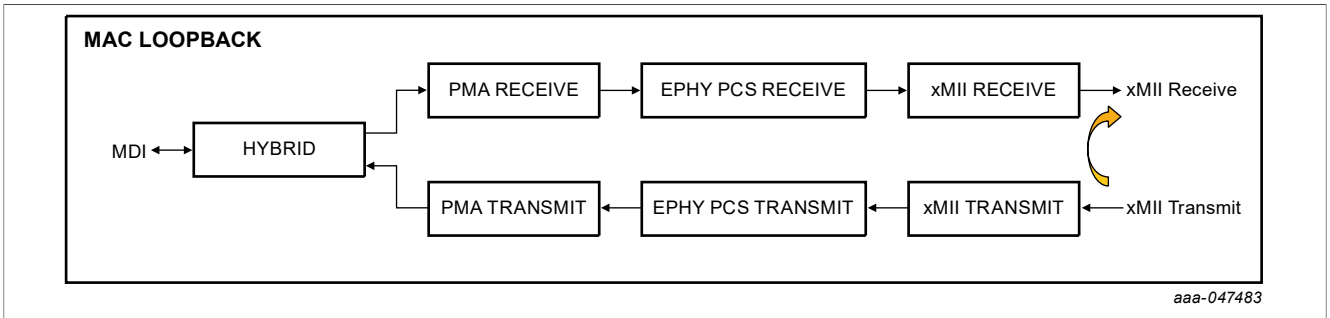


Figure 22. xMII MAC loopback

6.12.6 BIST generator/checker

The built-in self test (BIST) is an integrated Ethernet frame generator and checker intended for diagnosis. The generator and checker can be enabled independently. The frame header that is generated by the BIST generator is fully configurable via register settings with programmable interpacket gap (IPG).

The BIST frame generator can generate a mix of both good and bad frames. The BIST checker can also monitor incoming Ethernet frames and provide statistics on the number of good and bad frames received.

Together with the loopback modes, TJF1103 supports a number of BIST configurations allowing for self-testing of the entire communication chain.

6.12.6.1 Introduction

The BIST allows the data path to be tested without connecting a MAC to the PHY device.

Normally a MAC sends Ethernet frames to the PHY over an xMII interface. These frames are transmitted over the MDI and are eventually received by the remote PHY. The remote PHY transmits the frames through its xMII to the receiving MAC. For debugging purposes, the BIST module is able to replicate this behavior without involving a MAC. The BIST module consists of a generator and a checker. The generator generates Ethernet frames and the checker receives these frames and checks for errors. The number of error frames is captured in statistics counters.

A simplified block diagram of the BIST is shown in Figure 23.

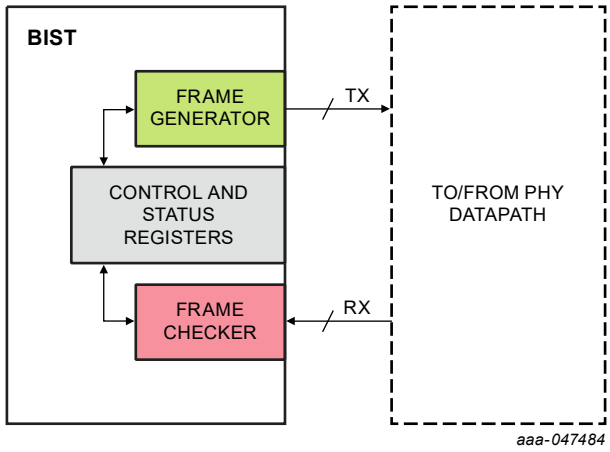


Figure 23. BIST block diagram

6.12.6.2 Functional description

The BIST module is not active by default, so the generator and checker need to be enabled (see BIST_GEN_CTRL and BIST_CHECK_CTRL registers, Table 212 and Table 230).

The generator composes Ethernet frames with configurable length, payload content and other header fields. The generated frames are dispatched either xMII or MDI facing (see TX_INTERCEPT and RX_INTERCEPT in Table 211).

The BIST checker checks the incoming data based on MDI or xMII (RXD) direction (see CHECK_EPHY_OR_XMII). The checker validates the CRC and RX_ER and logs status and diagnostics information.

There are two modes of operation. The mode is selected via bit BIST_GEN_MODE (Table 212).

Production mode is intended for production test. In this mode, the total number of frames generated by the generator is configurable. The same number of frames is expected at the checker. The total number of frames is a configurable combination of good frames and error injected frames (erroneous FCS). The BIST checker gathers statistics until a configurable timeout has expired (BIST_WAIT_TIMER) or all expected frames were received. Bit BIST_CHECK_DONE is set when the test has been completed. Status bit BIST_CHECK_FAIL indicates whether the test was passed or failed (see Table 232 and Table 231).

Continuous mode is similar to stress testing familiar from Ethernet test equipment. In this mode, the BIST generator generates continuous Ethernet frames and statistics are collected continuously. The Ethernet frames

tested can be generated by the BIST or the BIST can act as a sink for frames generated by external test equipment.

6.12.6.3 Generator

The BIST generator can generate the IEEE 802.3 Ethernet frame format with varying frame length and different types of payload data. Once the BIST generator has been configured (refer to Table 222 to Table 226), it begins generating Ethernet frames.

Table 23. Custom BIST generator frame

Preamble 7bytes	SFD 1 byte	DA 6 bytes	SA 6 bytes	EtherType 2 bytes	Frame Payload Data 46-1500 bytes	FCS 4 bytes	IPG 12 bytes

The number of preamble octets is configurable (PREAMBLE_LENGTH).

The IPG length is determined by bits IPG_LENGHT_TYPE and IPG_LENGTH:

- Fixed (IPG_LENGTH_TYPE = 0): the IPG for all frames is set to IPG_LENGTH.
- Increment (IPG_LENGTH_TYPE = 1): length incremented by 1 for each IPG until it reaches 255, then rolled-over to IPG_LENGTH
- Random (IPG_LENGTH_TYPE = 2). IPG_LENGTH acts as a minimum IPG as well as an LFSR seed.

The EtherType is configurable via the BIST_ETHER_TYPE register (Table 222).

The generator supports a number of modes for determining payload data length:

- Fixed (PAYLOAD_SIZE_TYPE = 0)
- Increment (PAYLOAD_SIZE_TYPE = 1)
- Random (PAYLOAD_SIZE_TYPE = 2)

In Fixed mode, the number of octets is set by PAYLOAD_SIZE (see Table 224).

In Increment mode, the data length starts with value PAYLOAD_SIZE[7:0]. The data length is incremented until it reaches PAYLOAD_SIZE[13:8]×256+255, when it rolls over to PAYLOAD_SIZE[7:0].

In Random mode, the payload length is determined by a 14-bit LFSR $x^{14}+x^{13}+x^{12}+x^{2}+1$ (LFSR is the current number generated by the LFSR random number generator). PAYLOAD_SIZE is used as seed. PAYLOAD_SIZE[7:0] sets the minimum payload size. PAYLOAD_SIZE[13:8] determined the maximum payload size.

If LFSR[13:8] ≤ PAYLOAD_SIZE[13:8], the full 14-bit LFSR[13:0] value determines the payload size.

If LFSR[13:8] > PAYLOAD_SIZE[13:8], the payload size is determined by LFSR[9:0].

If LFSR[13:0] < PAYLOAD_SIZE[7:0], the payload size is set to PAYLOAD_SIZE[7:0].

Note that LFSR is the current generated pseudo random value and is not a register

Frames in the standard range of 64 to 1535 octets are generated if PAYLOAD_SIZE[13:8] is set to 05h and PAYLOAD_SIZE[7:0] is set to 40h.

If PAYLOAD_SIZE[13:8] > 05h, jumbo frames will be generated. Jumbo frames up to the max size of 16383 bytes will be generated if PAYLOAD_SIZE[13:8] = 3Fh.

The payload data type is configurable as follows:

- Fixed (PAYLOAD_DATA_TYPE = 0): the fixed data octet is determined by FIXED_PAYLOAD_DATA.
- Increment (PAYLOAD_DATA_TYPE = 1): the data starts at 00h, increments by one and rolls over at FFh.

- PRBS (PAYLOAD_DATA_TYPE = 2): one of four PRBS schemes can be selected via BIST_PRBS_SELECT (PRBS7, PRBS9, PRBS11, PRBS15). The random seed is configured via BIST_LFSR_SEED. It is configurable (LFSR_SEED_USAGE) if the PRBS sequence is reset to the seed for each frame or continues free-running.

The BIST generator calculates the FCS as specified in the Ethernet standard and appends it to the frame. All frames are transmitted with TX_ER = 0.

The number of good frames and error frames is programmable. The total number of generated frames is the number of good frames plus the number of error injected frames. The generator generates the good frames first, then generates the bad frames.

In continuous mode, the generator only transmits good frames and good/bad frame plans are ignored. Setting bit STOP stops frame generation (see Table 212). To restart frame generation, set BIST_GEN_EN.

6.12.6.4 Checker

The BIST checker qualifies all received Ethernet frames and generates status and statistical results. The checker is enabled by setting bit BIST_CHECKER_EN (Table 230). The generator and checker work independently of each other. This means that generator and checker functionality can be distributed across two physical devices.

The checker classifies frames into good and bad frames. Good frames are frames with a correct FCS and bad frames with an incorrect FCS. The checker also counts the number of frames received with RX_ER set (R_RXER_FRAME_CNT, Table 235).

The statistics (R_GOOD_FRAME_CNT and R_BAD_FRAME_CNT) can be reset via STATISTIC_CNT_RST.

In production mode, status information is available (in Table 231) once the BIST test has been completed:

- GOOD_FRAME_ERROR indicates that the number of good frames does not match the expected number according to the configured plan.
- BAD_FRAME_ERROR indicates that the number of bad frames does not match the expected number according to the configured plan.
- RX_ER_DETECT_ER is set if a frame is received with RX_ER indication asserted
- RXDV_DETECT_ER is set if no data valid indication is observed

6.13 Interrupts

The TJF1103 signals important events, for instance changes to link availability, via the INT_N interrupt request (IRQ) pin. In order to efficiently determine which event triggered the IRQ, an interrupt tree is implemented. The INT_N pin is driven low when at least one interrupt request (IRQ) is active and enabled. Otherwise, the INT_N pin is high-Z.

Multiple devices can share the INT_N IRQ line using a wired-OR topology.

6.13.1 Interrupt tree

The interrupt tree is designed to support multi-port PHY devices. It differentiates between port, global and device-level interrupt sources. Port-level IRQs are presented once, because this device has a single port. Common functionality shared among multiple data ports is captured in the global section.

At device level, the port and global levels are combined. The ALWAYS_ACCESSIBLE register serves a specific purpose. This register is available for MDIO read and write access when the VDD_CORE supply or the chip-internal 25 MHz REFCLK[4] is not present.

4 REFCLK is an internal clock that is drived from the XTAL or the RMII REF_CLK pin in RMII-clkmode.

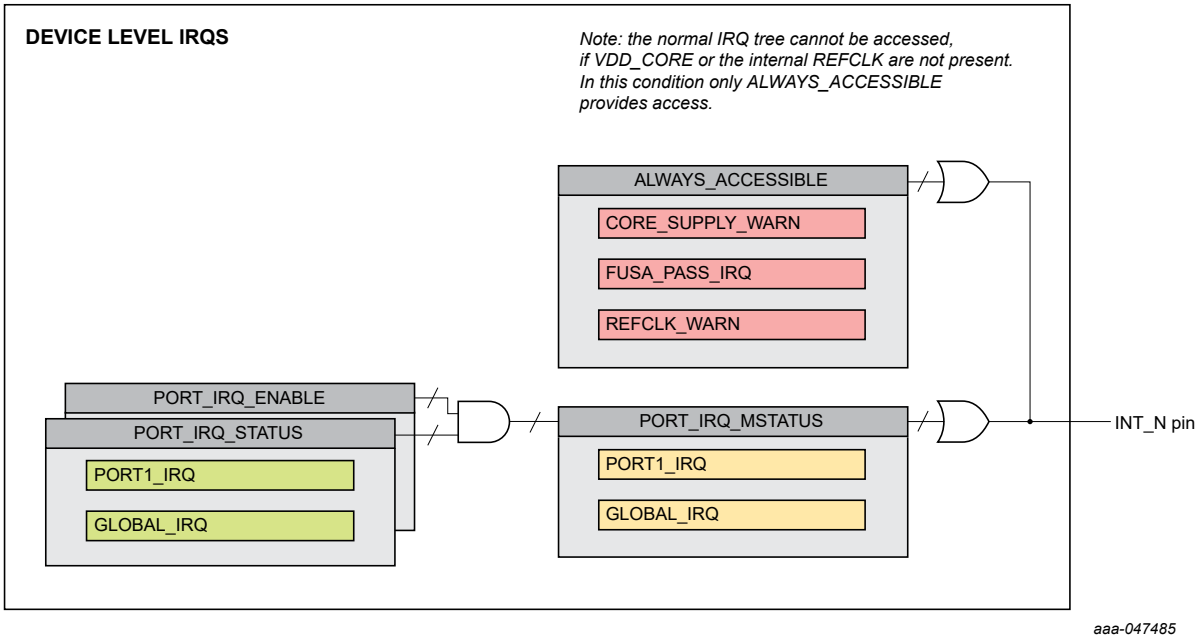


Figure 24. Device IRQ

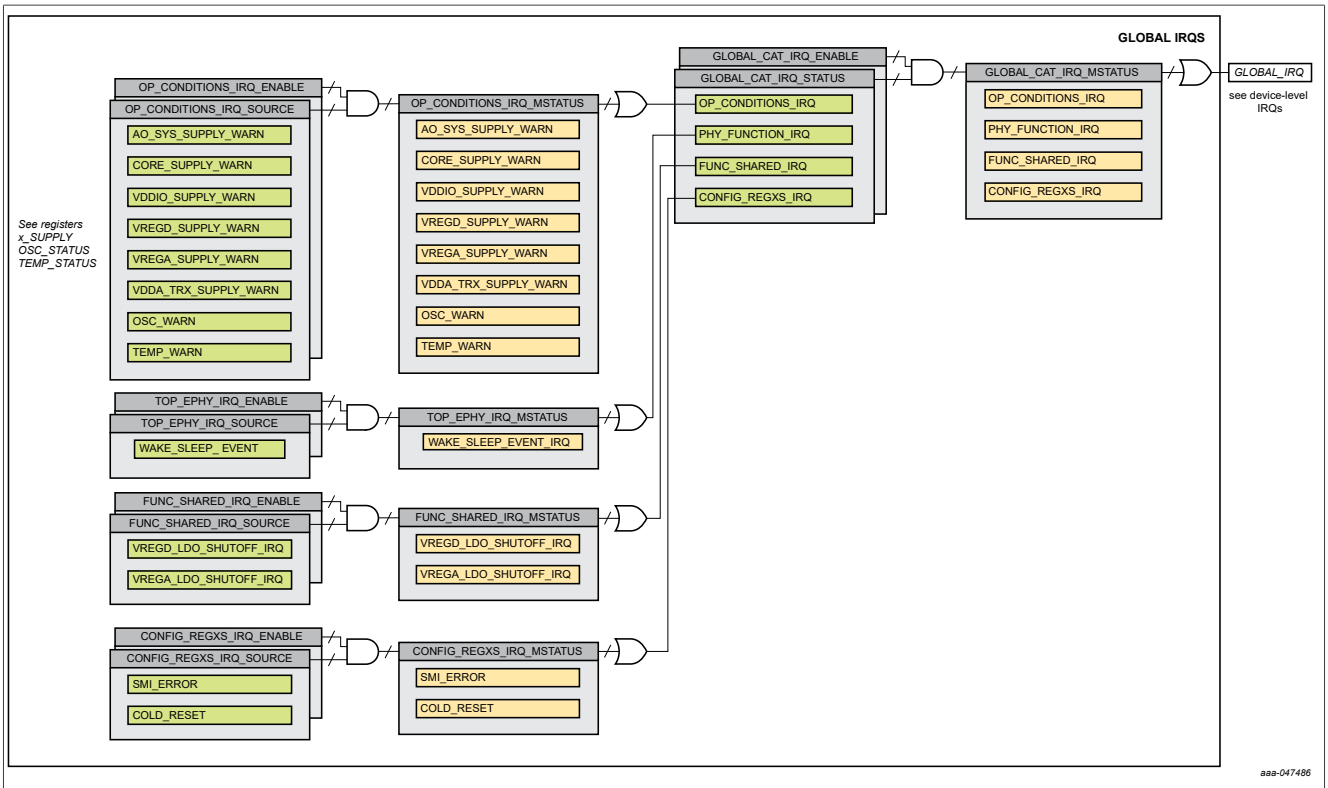


Figure 25. Global IRQs

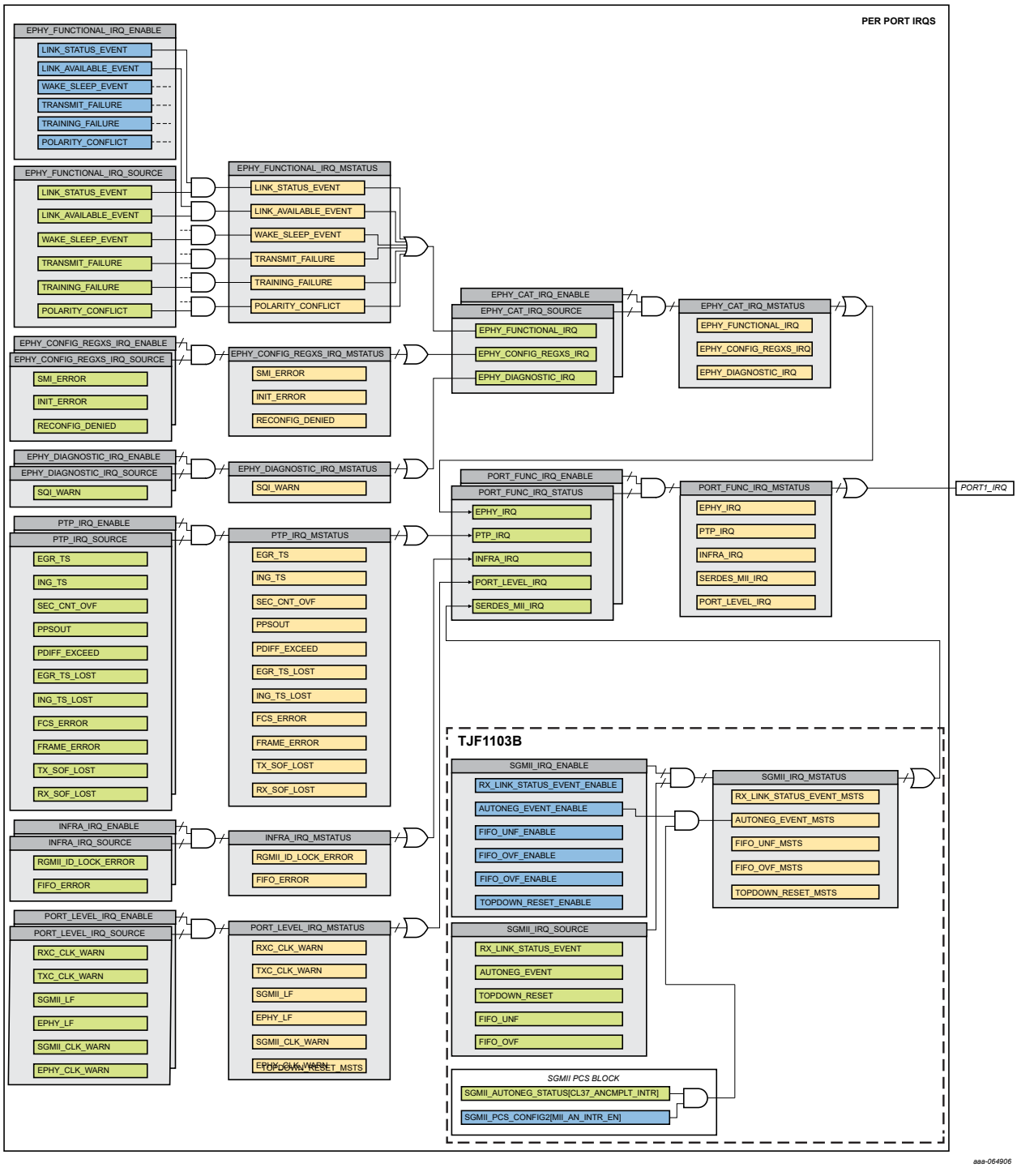


Figure 26. Port IRQs

6.13.2 Diagnostic interrupts

The non-maskable FUSA_PASS_IRQ interrupt is generated to signal that all self-checks, as described in the section Section 6.4, have been passed successfully.

A number of IRQs, listed in Table 24, signal a severe malfunction when triggered. Interrupts are disabled by default and can be enabled via the IRQ_ENABLE registers.

Table 24. Diagnostic and self-test related IRQs

Non-maskable interrupts	Description
FUSA_PASS_IRQ	The startup self-test has completed successfully
CORE_SUPPLY_WARN	Supply monitor for the core supply
VDDA_TRX_SUPPLY_WARN	Supply monitor for the VDDA_TRX supply
VREGA_SUPPLY_WARN	Supply monitor for the VREGA_IN supply
VREGD_SUPPLY_WARN	Supply monitor for the VREGD_IN supply
TEMP_WARN	Temperature monitor
OSC_WARN (not in RMII-clkmode)	XTAL frequency warning
VDDIO_SUPPLY_WARN	Supply monitor for the VDDIO
AO_SYS_SUPPLY_WARN	Supply monitor for the Always-On

6.14 Timestamping

The PTP timestamping module is a generic module designed to supports both 100 Mbit/s and 1000 Mbit/s operation. In the TJF1103, the timestamping block supports 100 Mbit/s mode and is internally connected to the on-chip MII bus, as illustrated in Section 6.3.

To compensate for chip-specific pipeline delays, egress and ingress path latency must be configured, in Table 173 and Table 175 respectively, as follows:

TX_PIPE_DLY_NS = 77

RX_PIPE_DLY_NS = 413

6.14.1 Introduction

IEEE 1588 v2 (PTP) is an industry standard that enables precise time synchronization of nodes in an Ethernet network. Synchronization is achieved by exchanging protocol-defined PTP event messages. Based on these PTP event messages, the follower[5] can correct offset and drift in its local clock to synchronize with the leader clock.

The PTP module is sandwiched between the internal 802.3 PHY's MII interface and external-facing MII/RMII/RGMII/SGMII interface. The module provides a 1588 digital clock implementation, transmit and receive frame parsing, start-of-frame detection, transmit and receive timestamp units, event timestamp unit and a Pulse-Per-Second (PPS) generator.

6.14.1.1 Features

The following features are provided by the IEEE 1588 v2 PTP block:

- Support for 100BASE-T1 and 1000BASE-T1 PHYs
- Supports hardware timestamping features of the IEEE 1588 v2 PTP clock
- Provides timestamping on ingress and egress PTP messages
- Hardware self-locking or software-assisted rate correction to an external reference clock
- Timestamping on external pin sync events

5 Unrelated to 100BASE-T1 Leader/Follower.

- Ingress and egress timestamps stored in ring buffer for host processing
- Support for two-step operation
- Supports in-band timestamp delivery for ingress path
- Supports detection of PTP frame encoded in Ethernet, both untagged and 802.1Q VLAN tagged (double tagged VLAN is not supported)
- Software-configurable frame filter to match PTP event frames

6.14.2 Overview

Figure 27 depicts the integration of the PTP module at system level..

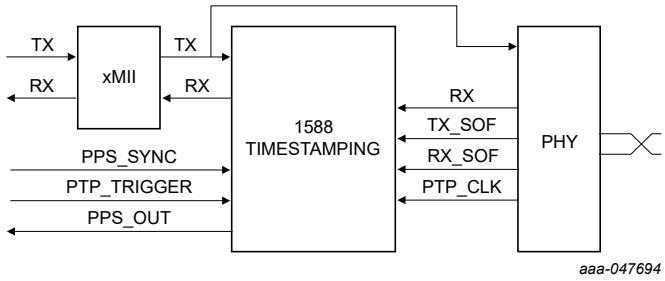


Figure 27. PTP PHY integration

The timestamping module comprises the following blocks, shown in Figure 28: the clock (referred to as the local time counter (LTC)), the transmit and receive frame parser and qualifier, transmit and receive timestamp FIFOs and miscellaneous functions such as control and status registers, PPS output and syncing.

The TX_SOF and RX_SOF indicators comes from the PHY sublayer and usually exhibit a pipeline delay. This device-specific delay is constant and can be corrected automatically by configuring registers TX_PIPE_DLY_NS and RX_PIPE_DLY_NS (see Section 6.14).

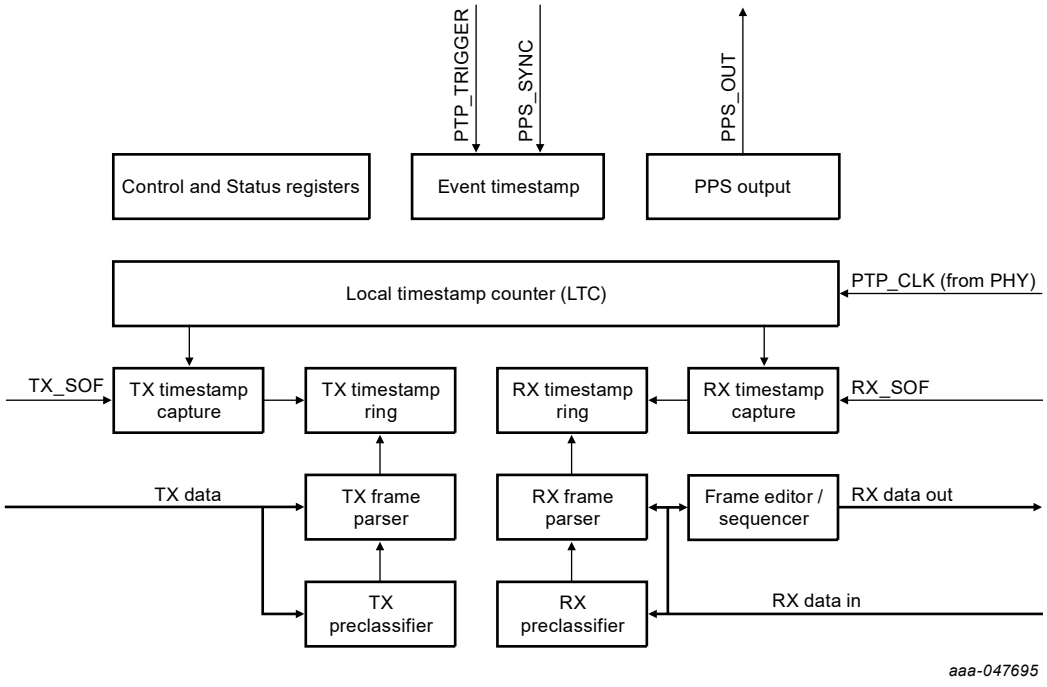


Figure 28. PTP block diagram

6.14.3 Clocking scheme

The IEEE 1588 PTP uses a timestamp clock that is derived from the Ethernet PHY block. The PTP clock frequency must be configured in the PTP_CLK_PERIOD register (Table 126). For 100BASE-T1, the PTP clock frequency is 66.6 MHz, so the PTP_CLK_PERIOD must be set to 15 ns.

6.14.4 Resets

By default, the PTP module is inactive. All clocks are disabled and the internal logic is reset. The host can enable the PTP module by setting PTP_ENABLE = 1 (Table 287).

6.14.5 Local time counter

The local time counter (LTC) module is the clock used for timestamping. It is local to the PHY and can be synchronized with other ICs via a PPS_SYNC facility. The software can interact with the LTC to control the absolute value, the rate and to change the offset.

The PTP_CLK is the digital clock that drives the LTC. Depending on the speed of the PHY, the PTP_CLK frequency is either 125 MHz (1000BASE-T1) or 66.66 MHz (100BASE-T1). A block diagram of the LTC structure is shown in Figure 29:

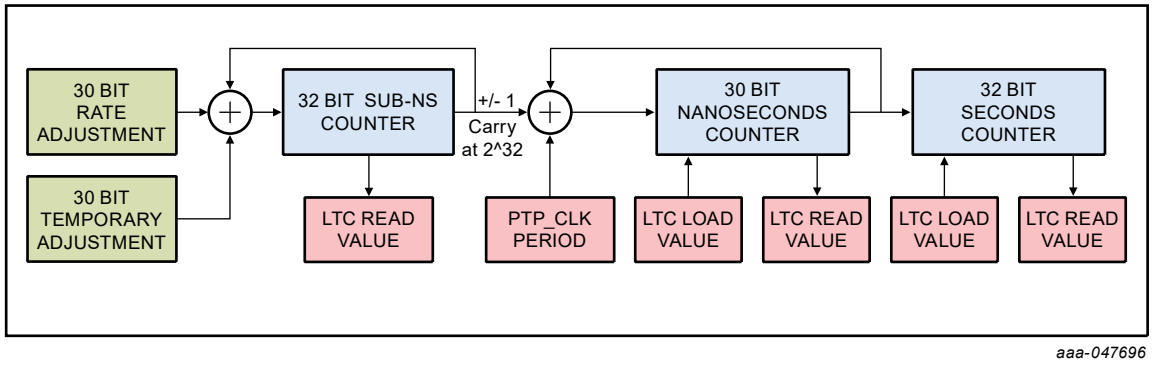


Figure 29. Block diagram of LTC

The LTC contains a 30-bit nanosecond counter and a 32-bit second counter.

The nanosecond counter is incremented by 8 (15) after every PTP_CLK cycle for 1000 Mbit/s (100 Mbit/s) operation. This translates to 8 ns (15 ns) per PTP_CLK tick. Once the nanosecond counter reaches the rollover value, the second counter is incremented by 1. The 32-bit second counter has a rollover time of 136 years.

A sub-ns counter is used for continuous and temporary rate-correction in fractions of a nanosecond per clock. Such ns fractions are accounted for in the 32-bit wide sub-ns counter, which has a granularity of 2^{-32}ns. When the sub-ns counter rolls over, an additional nanosecond is added or subtracted from the nanosecond counter.

6.14.5.1 Direct read/write

6.14.5.1.1 Immediate LTC load

An immediate load causes the values stored in the nanosecond and second registers (see Table 128 to Table 131) to be transferred to the LTC.

1. Program second/nanosecond values via LTC_WR_NSEC_0, LTC_WR_NSEC_1, LTC_WR_SEC_0, LTC_WR_SEC_1
2. Load these values into the internal LTC counters by setting bit LOAD_LTC (see Table 127)

6.14.5.1.2 PPS edge triggered load

PPS edge loading transfers the time loaded into the nanosecond and second registers (Table 128 to Table 131) into the LTC on the rising edge of the PPS_SYNC signal.

1. Program second/nanosecond values via LTC_WR_NSEC_0, LTC_WR_NSEC_1, LTC_WR_SEC_0, LTC_WR_SEC_1
2. Load these values into internal counters by setting LOAD_LTC_PPS (see Table 127)
3. The second and nanosecond values are loaded into local counters on the rising edge of the external PPS_SYNC signal.

When the frequency of the PPS_SYNC signal is greater than 1 Hz, loading of the external PPS sync signal must be staggered. The PPS_SYNC signal must be paused before loading the LTC. Once the data has been loaded, the PPS can be restarted. This step is needed to ensure that an edge can be reliably associated with an absolute time value. Pause the PPS signal, then follow step 1 and 2 before restarting the PPS Sync signal.

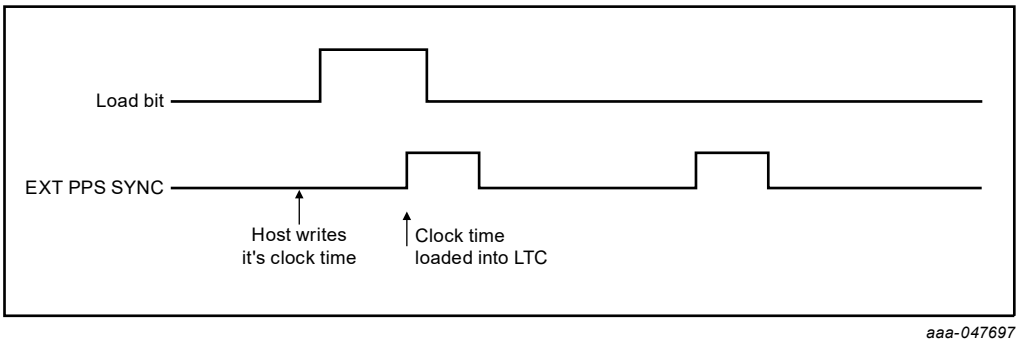


Figure 30. Loading LTC on rising edge of PPS

6.14.5.1.3 Immediate LTC read

1. Set the READ_LTC bit to capture the local clock time (see Table 127)
2. Read the time data from tables LTC_RD_DATA_0 to LTC_RD_DATA_4 (Table 132 to Table 136)
3. The time data stored (in Table 128 to Table 131) can be read multiple times as new values are only loaded when READ_LTC is reprogrammed.

6.14.5.1.4 PPS edge triggered read

The LTC value is latched on the rising or falling edge of the PPS input. It can then be read from the EXT_PPS_TS_DATAx registers (Table 149 to Table 153). The timestamp remains latched until EXT_PPS_TS_DONE is set (Table 154). Setting EXT_PPS_TS_DONE readies the hardware for latching the LTC at the next edge.

It is mandatory to read the EXT_PPS_TS_DATAx registers in order, starting with EXT_PPS_TS_DATA0. It is not necessary to read all five registers. The read sequence can be interrupted at any time by setting EXT_PPS_TS_DONE. This frees the register for the next PPS edge event.

Note: *The timestamp is retained in the registers until EXT_PPS_TS_DONE is set. Retaining the value allows the data to be read multiple times.*

6.14.5.2 Rate correction

In order to compensate for rate difference between the PHY and an external clock source (for instance a microcontroller or switch), digital rate correction can be applied. For every PTP_CLK cycle, a rate correction

value RATE_ADJ_SUBNS (see Table 137 and Table 138) is added to or subtracted from a hidden sub-nanosecond counter. On overflow/underflow of this sub-nanosecond counter, the carry is added to or subtracted from the nanosecond counter and integrated into the visible LTC. RATE_ADJ_SUBNS is a 30-bit value specified in units of 2^{-32} ns. Bit CLK_RATE_ADJ_DIR (in Table 138) determines whether the tuning value, RATE_ADJ_SUBNS, is added or subtracted.

As an example, lets assume the clock rate of the LTC is slow when compared with the external PPS. The difference is 0.125 ns in the time interval of one PTP_CLK cycle.

Then, RATE_ADJ_SUBNS = rate * 2^{32} = 30'h2000 0000.

Note: *For the TJF1103A: consult the application notes (ref.[6]) for limitations that apply when changing CLK_RATE_ADJ_DIR bit settings.*

6.14.5.3 Temporary rate correction

An LTC offset is corrected by temporarily speeding-up or slowing-down the LTC clock, thereby slowly integrating the offset error over multiple ptp_clk cycles. This avoids abrupt jumps and time discontinuities and guarantees a monotonic clock.

A temporary correction is similarly applied to rate-correction, with an additional time window configured in which the rate change is applied. Parameter TEMP_ADJ_SUBNS (Table 139 and Table 140) holds the temporary rate-correction value and TEMP_ADJ_DUR (Table 141 and Table 142) is used to configure the number of PTP_CLK clock cycles to be adjusted. Bit CLK_TEMP_ADJ_DIR in Table 140 controls the update direction (add/subtract). Setting self-clearing bit CLK_LD_TEMP_ADJ triggers a single temporary adjustment.

TEMP_ADJ_SUBNS is a 30-bit value specified in units of 2^{-32} ns.

The temporary rate correction is in addition to the regular rate-correction described earlier.

For example, let us assume an offset error of 25.5 ns. With an integration rate of 0.125 ns per ptp_cycle, the temporary correction must be applied for 25.5/0.125 = 204 ptp_cycles. Thus, the following values are written:

TEMP_ADJ_SUBNS = rate * 2^{32} = 30'h2000 0000

TEMP_ADJ_DUR = 25.5/0.125 = 204

6.14.6 LTC synchronization

A typical system including MAC, IEEE 1588 protocol engine and a PHY is depicted in Figure 31.

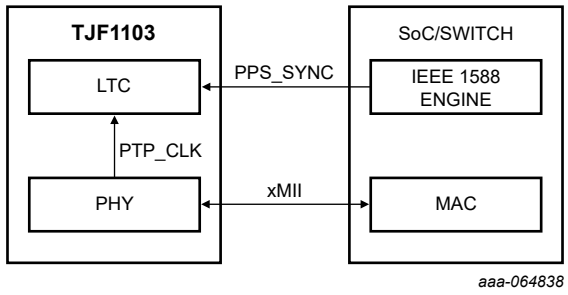


Figure 31. Example clocking scheme

An external crystal is usually used to drive the LTC. Crystal clock timing differs slightly from the timing in timestamping engines. For consistency, all timestamps in multi-port devices such as switches must be taken using the same timebase.

Time difference between the LTC and any other timestamping clocks can occur for the following reasons:

1. A relative frequency difference within the 100 ppm limit can be present between clocks.

2. The timestamp clock in another device is itself a PTP follower clock, and is therefore constantly being rate- and offset-corrected.

The PTP module can lock onto an external Pulse Per Second (PPS) signal. The PPS signal is then used to correct the LTC automatically. The PPS does not need to be a pulse *per second*. The LTC block can track any low-frequency signal, such as 1 Hz or 100 kHz. The rising or falling edge of an external PPS synchronization signal is used to correct timing drift. There are multiple ways to synchronize the LTC with the external reference PPS synchronization signal.

An external software tracking routine can be implemented to synchronize the LTC via a software-driven control loop. Alternatively, the PTP block can track an external PPS synchronization pulse autonomously.

6.14.6.1 Software tracking

After initialization, an external host reads the clock time from the PHY on the rising edges of consecutive PPS_SYNC signals and calculates the rate difference between the PHY and the IEEE 1588 protocol engine. Based on these calculations, the host can update the LTC by using rate adjustment method to correct the rate difference and temporary adjustment to correct the offset. The following steps summarize the mechanism employed for a relatively slow PPS input:

1. The host pre-loads the expected LTC value (LTC_0) at the PPS_SYNC edge. The LTC will be running once the PPS Sync input has fired.
2. Capture the LTC timestamp (LTC_1) at the next active PPS_SYNC edge. The relative rate difference is calculated by dividing the expected PPS cycle time by LTC_1 - LTC_0. The offset error can be determined through LTC_1.
3. Correct the rate and offset as described in Section 6.14.5.
4. Repeat continuously for rate- and offset-correction based on LTC snapshots LTC_{n+1} and LTC_n.

6.14.6.2 Hardware tracking

The PTP block implements an optional hardware control loop to track an external PPS_SYNC input. Rate difference and offset errors are detected automatically and corrected on-the-fly. Setting HW_LTC_LOCK_EN (Table 143) enables this feature.

Initialization is identical to the software tracking approach. The LTC value is pre-loaded and transferred into the working registers at the next active PPS Sync edge. The PPS reference frequency must be programmed via registers HW_EXT_PPS_x (Table 144 and Table 145).

Once the LTC has been loaded, the LTC value is captured at the next PPS_SYNC event. A phase comparator calculates the phase difference between observed LTC value and expected reference time. A direction signal is generated to indicate whether the LTC is lagging or leading. Using this information, the rate difference and offset errors are computed and adjusted at each PPS Sync cycle.

If the hardware is not able to track the PPS input and the error exceeds a boundary set by HW_LOCK_ER_LMT_0 and HW_LOCK_ER_LMT_1 (Table 146 and Table 147), a flag (PDIFF_EXCEED; Table 161) is asserted and an IRQ is generated.

6.14.7 PPS output

It is possible to generate a pulse-per-second (PPS) signal (PPS_OUT) based on the internal LTC and externalize it on a GPIO pin. This feature is enabled by asserting PPS_OUT_EN (Table 124). The hardware generates a nominal a 1 Hz signal with a pulse at each one-second transition. When enabled, the PPS generator generates a pulse-per-second strobe.

To change the polarity of the generated PPS signal, set bit PPS_OUT_POL.

It is also possible to loop the external PPS Sync signal out on PPS_OUT for debugging purposes (see PPS_SYNC_RETURN). The PPS_OUT signal can be used to measure LTC synchronization accuracy against an external reference clock.

6.14.8 Event timestamp

External events can be monitored and timestamped. A rising edge on the PTP_TRIGGER input latches the current LTC value into the EXT_TRG_TS_DATA registers (Table 155 to Table 159).

Note: *The timestamp is retained in the registers until bit EXT_PPS_TS_DONE (Table 154) is set. This allows to read the data multiple times.*

6.14.9 Egress timestamping unit

Egress timestamping is part of the transmit path. It is responsible for identifying a PTP message inside an Ethernet frame (classify), pulling relevant information out of the PTP message (parse) and for timestamping the frame. The captured timestamps are stored in a buffer (dataset capture and TS ring) for retrieval via MDIO. The data flow is depicted in Figure 32.

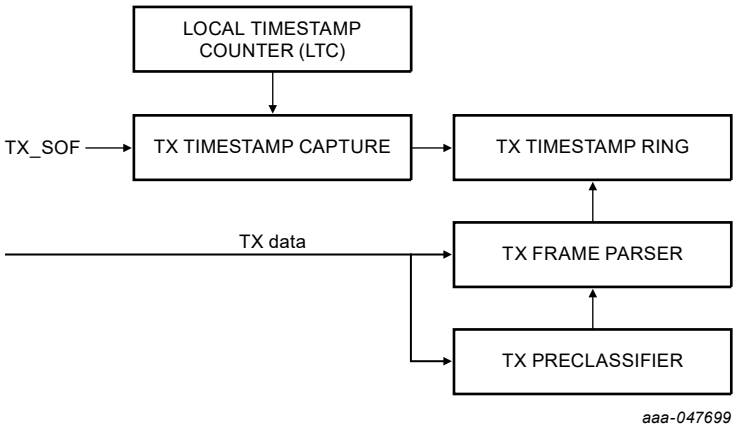


Figure 32. Egress timestamping unit

TX_SOF is generated by the Ethernet PHY, not the PTP module. TX_SOF is derived from PCS information and not from the start-of-frame delimiter (SFD). The parser inside the PTP block detects the actual SFD point and compensates for the delay between TX_SOF and SFD.

6.14.9.1 Pre-classifier and TX parser

The TX parser interfaces with the MII/GMII TX interface. It monitors the incoming transmit frames to detect relevant IEEE 1588 PTP event messages. It is able to recognize PTP event messages transported in layer 2 Ethernet frames[6]. The parser supports untagged and 802.1Q VLAN Tagged (single tagged) Ethernet frame coding. PTP messages are qualified by the MAC address. Two PTP standard fixed MAC address (01:1B:19:00:00:00 and 01:80:C2:00:00:0E) are supported. Additionally, a single entry DA match rule can be used to support user-defined MAC addresses (USER_MAC_DA).

Once TX Enable is asserted on the internal MII/GMII bus, the incoming frame is parsed to identify the PTP message. If the frame qualifies, all necessary PTP message contents are extracted and stored for future use. It also sets a flag to indicate that the detected incoming message is a PTP message.

The following frame filters can be enabled/disabled individually:

6 IP encapsulated PTP messages are not recognized.

1. Destination MAC match (two fixed addresses, one configurable (see USER_MAC_DA registers; Table 166 to Table 168)
2. VLAN tagged (see register VLAN_TAG_ALLOW; Table 164)
3. Message type: Sync, Delay_Req, Pdelay_Req, Pdelay_Resp event messages (see register EVENT_MSG_FILT; Table 172)
4. Match a specific versionPTP (see bit VERSION in Table 164)
5. Match a specific domain number (see bit DOMAIN_NUM in Table 164)

It is possible to timestamp the following PTP event messages:

Table 25. PTP Event Messages

PTP Message Type	Value
Sync	0
Delay_Req	1
Pdelay_Req	2
PDelay_Resp	3

6.14.9.2 TX timestamp ring buffer

The TX timestamp (TS) Ring buffer stores the timestamp data in up to 4 available slots. Additional metadata is stored along with the timestamp to correlate the information with an Ethernet frame. This includes PTP message sequence, domain number, message type and valid flag to indicate the data set has not been read yet.

The buffer is organized as a ring buffer with the oldest valid entry at the top ready to be latched to the EGR_RING_DATA_0 to 5 registers (Table 178 to Table 183) by a read operation. Once the timestamp has been read via the MDIO interface, the ring buffer pointer is advanced by setting bit EGR_RING_DONE (Table 184).

When the buffer is full, the oldest entry is flushed out to make room for a new entry. If enabled, an interrupt is generated on overflow.

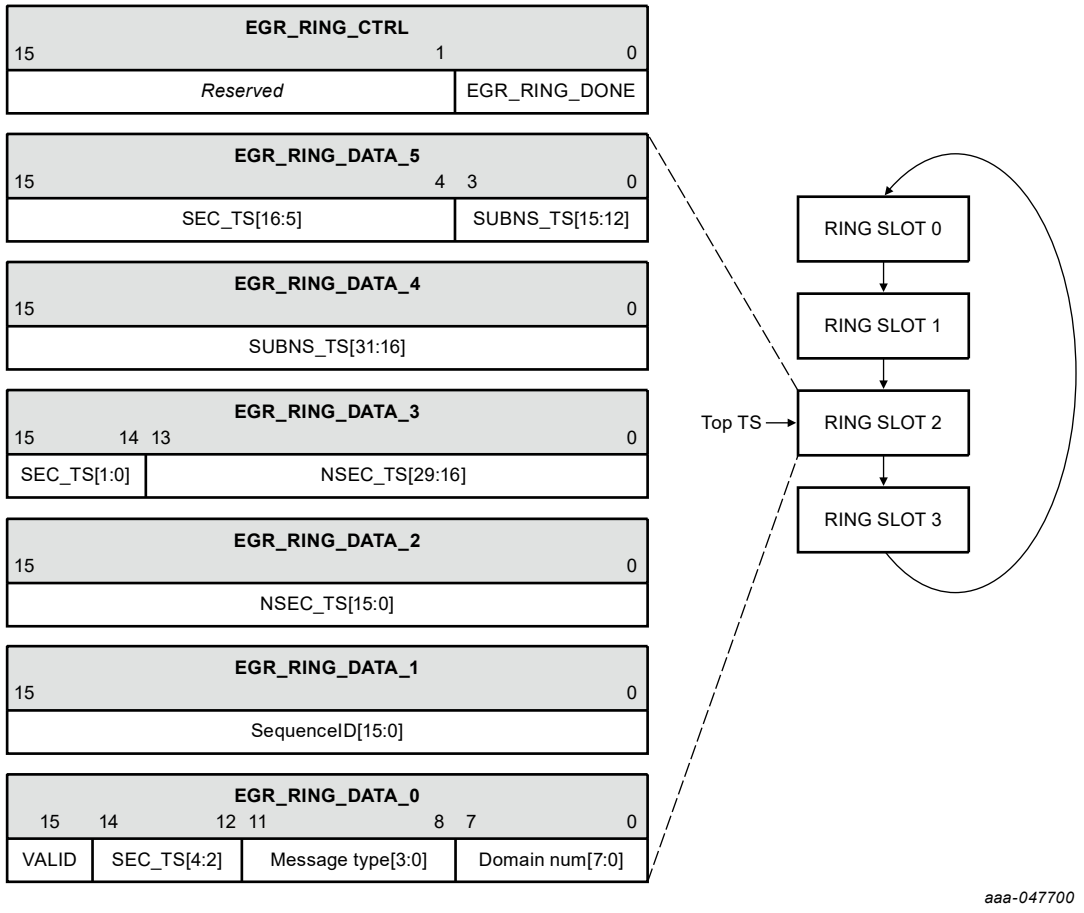


Figure 33. Egress TS ring buffer organization

6.14.10 Ingress timestamping unit

The ingress timestamping is part of the receive path. It is responsible for identifying a PTP message inside an Ethernet frame (classify), pulling relevant information out of the PTP message (parse) and for timestamping the frame. The captured timestamps are stored into a buffer (dataset capture TS ring) for retrieval via MDIO. Alternatively, the timestamp can be embedded directly into the Ethernet frame (message editor). The data flow is depicted in Figure 34.

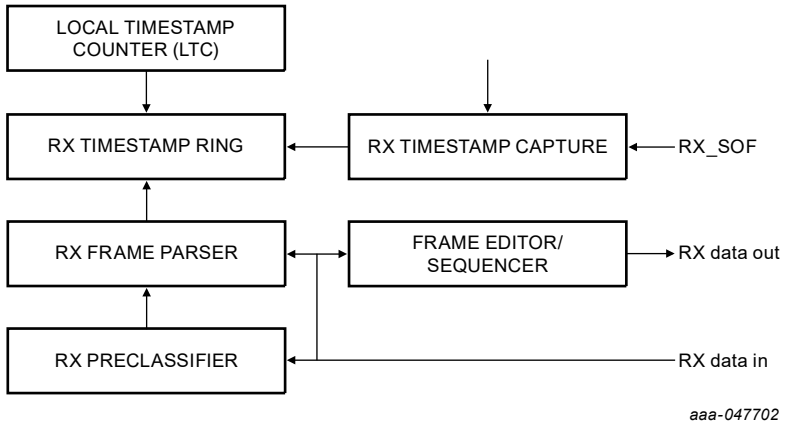


Figure 34. Ingress timestamping unit

RX_SOF is generated by the Ethernet PHY, not the PTP module. RX_SOF is derived from PCS information and not from the start-of-frame delimiter (SFD). The parser inside the PTP block detects the actual SFD point and compensates for the delay between RX_SOF and SFD.

6.14.10.1 Pre-classifier and RX parser

The RX parser interfaces with MII//GMII RX interface. It monitors the incoming receive frames to detect relevant IEEE 1588 PTP event messages. The parser and classifier logic is identical to Section 6.14.9.1.

6.14.10.2 RX timestamp ring buffer

The RX timestamp (TS) Ring buffer stores the timestamp data in up to 4 available slots. Additional metadata is stored along with the timestamp to correlate the information with an Ethernet frame. The organization of the ring structure and registers is as described in Section 6.14.9.2.

6.14.10.3 Frame message editor

As an alternative to delivering the RX timestamp using the ring buffer exposed via MDIO, it is possible to deliver the timestamp inside the PTP event frame. The message editor updates the PTP message header and the FCS in the Ethernet frame.

The engine is able to modify four reserved octets at PTP header offset 16 and overwrite these bits with 32 bits timestamp data. Three timestamp formats are supported:

Seconds/Nanoseconds format 0

The inserted timestamp holds 2 bits of the second counter and 30 bits of the nanosecond counter: {SEC[1:0], NSEC[29:0]}

Nanoseconds format 1

The inserted timestamp is a 32-bit (integer) of ns precision. For this, a 64-bit nanoseconds value is derived from the 32-bit second and 30-bit nanosecond base counters (seconds * 1000 + nanoseconds). The lower 32 bits of the resulting 64-bit value are inserted into the Ethernet frame.

Nanoseconds/subnanoseconds format 2

The inserted timestamp is a 32-bit (fixed point) integer of ns and subns precision. For this, a 64-bit nanosecond value is derived from the 32-bit second and 30-bit nanosecond base counters (seconds * 1000 + nanoseconds). A fixed point number is compiled from the ns and subns counters of the LTC. The resulting 32-bit value has (32-N) integer ns bits and fractional N-bits for the subns position. The position of the decimal (N) can be configured via bit ING_MSG_TS_PTR (see Table 177).

6.14.10.3.1 Checksum regeneration

Two parallel CRC-32 engines are used to check and regenerate a Frame Check Sequence (FCS) when a frame is modified. Each frame is checked by matching the residue with the magic number (32'hC704_DD7B). In parallel, a new FCS is computed to account for the modified 32 bits.

If a frame qualifies as a PTP event frame and the original FCS is correct, the timestamp is patched in and the FCS is regenerated. If the original FCS is found to be incorrect, the FCS is regenerated but an inverted value is sent to indicate to the MAC/PHY that a corrupted frame was received. This ensures that an FCS of a corrupted frame is not regenerated accidentally with the frame appearing correct.

6.14.11 Interrupts

The PTP module signals the occurrence of significant events via a PTP interrupt request (IRQ). This IRQ line is connected to the device interrupt tree at device level.

6.14.11.1 PTP interrupts

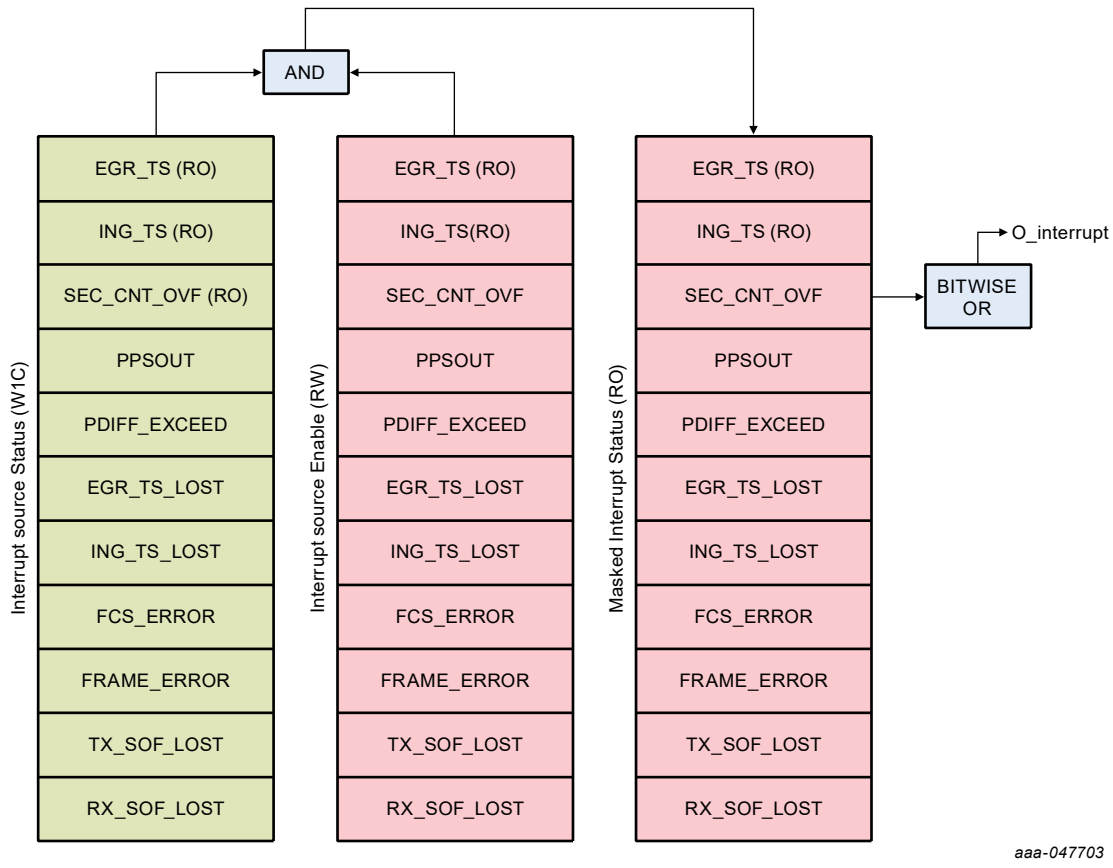


Figure 35. PTP interrupts

1. EGR_TS: egress timestamp event (read only)
2. ING_TS: Ingress timestamp event (read only)
3. SEC_OUT_OVF: seconds counter saturates all 32 bits (read only)
4. PPS_OUT: PPS OUT event
5. HW_SYNC_EXCD: hardware-measured phase difference between external PPS sync and local LTC exceeds 250 µs (if PPS sync has a period of 1 second)
6. EGR_TS_LOST: egress TS lost due to overflow
7. ING_TS_LOST: ingress TS lost due to overflow
8. FCS_ERROR: FCS input error detected (in-band signaling mode)
9. FRAME_ERROR: ingress frame error (preamble detected but no SFD; incomplete PTP TS data is received)
10. TX_SOF_LOST: TX SOF not detected for a PTP event frame
11. RX_SOF LOST: RX SOF is not detected for a PTP event frame

6.14.12 Diagnostics

The PTP module captures the following statistics from the parsed frames:

- Total number of recognized PTP event frames received
- Number of PTP event frames received with FCS errors[7]

6.15 TC10

Figure 36 describes the sleep handshake, which is the intended way to enter sleep when TC10 sleep is configured (WAKE_SLEEP_CONFIG.FUNCTION_SELECT='10'), making sure both PHYs enter sleep mode. Alternatively, e.g., when the handshake is not functioning or for testing purpose, DEVICE_SLEEP can be entered without TC10 hand-shake by SLEEP_REQUEST from DEVICE_STANDBY mode. See Figure 3.

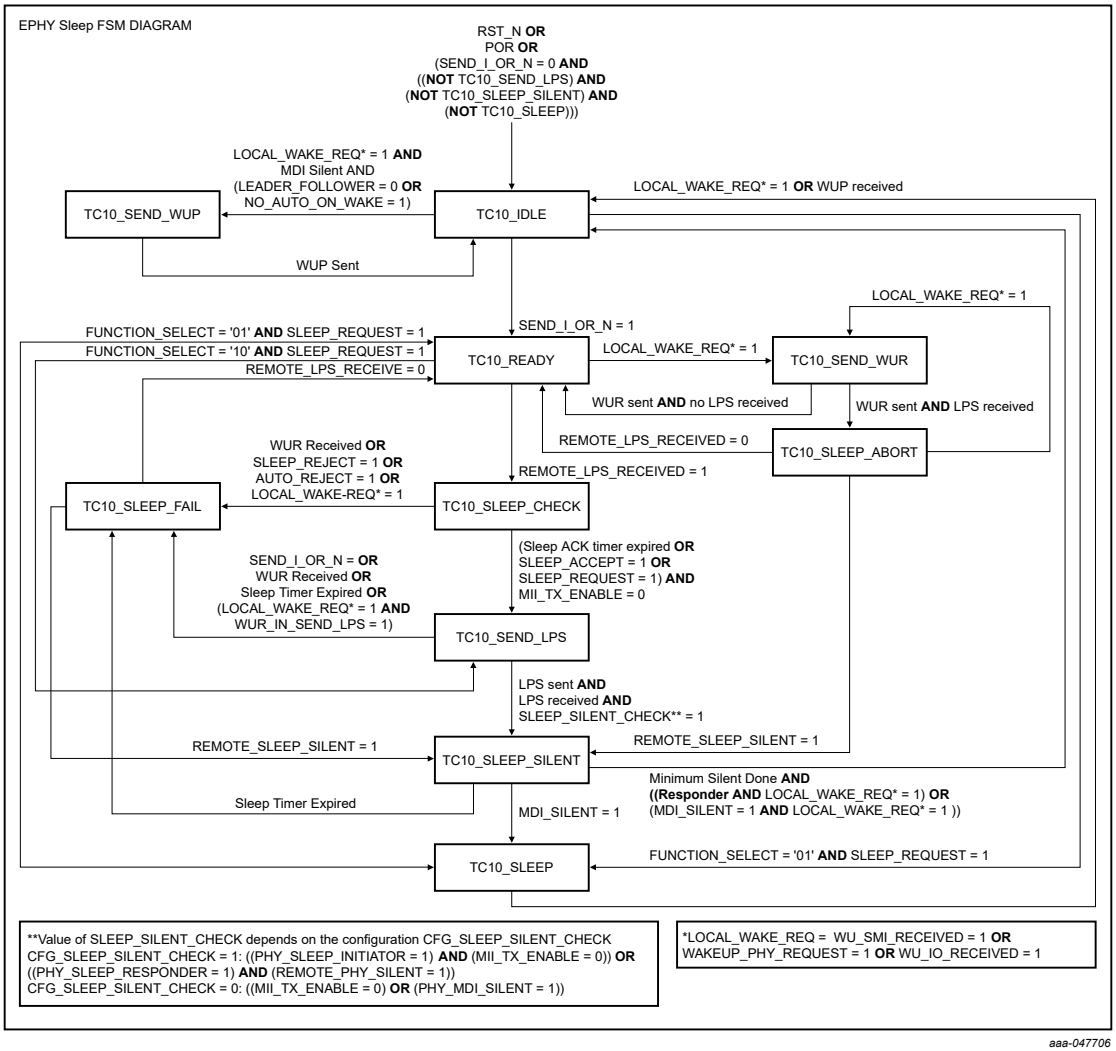


Figure 36. TC10 Ethernet PHY state transitions

7 Only available if the frame editor is enabled.

6.16 Miscellaneous

6.16.1 JTAG

The TJF1103 supports IEEE1149.1 and IEEE1149.6-compliant JTAG interfacing for boundary scan. A boundary scan description file (BSDL) is available on request.

JTAG mode is selected via pin strapping (see Section 6.8.1). In this mode, the JTAG TAP interface is accessible on pins TMS, TDI, TDO and TCK as shown in Table 26. Other pins function normally until an IEEE1149 instruction is executed.

A device reset via the RST_N pin is needed to exit JTAG mode.

Table 26. JTAG interface

JTAG Function	Symbol	Pin	Type[1]	Description
TMS	TMS/GPIO0/CONFIG0	17	IO, PU	JTAG test mode select (VDDIO domain)
TDI	TDI/GPIO1	18	I, PU	JTAG test data in (VDDIO domain)
TDO	RX_ER/GPIO2/TDO/CONFIG1	19	O	JTAG test data out (VDDIO domain)
TCK	TX_ER/GPIO9/TCK	28	I	JTAG test clock (VDDIO domain)

[1] I: digital input; O: digital output; IO: digital input/output; OD: digital open-drain output; AO: Analog output; AI: Analog Input; AIO: Analog input/output; PU: weak pull-up; P: power supply. G: ground

6.16.2 General-purpose I/Os

The device has 12 GPIOs multiplexed on functional device pins. Not all pins are available in all xMII modes. Table 27 provides an overview of which GPIOs are available in each xMII mode.

Table 27. Available GPIOs across xMII modes

GPIO	MII	RMII	RGMII	SGMII
GPIO0	Available	Available	Available	Available
GPIO1	Available	Available	Available	Available
GPIO2	Available[1]	Available[1]	Available	Available
GPIO3	—	Available	—	Available
GPIO4	—	Available	—	Available
GPIO5	—	—	—	Available
GPIO6	—	—	—	Available
GPIO7	—	—	—	Available
GPIO8	—	—	—	Available
GPIO9	Available[2]	Available[2]	Available	Available
GPIO10	—	Available	—	—
GPIO11	—	Available	—	—

[1] if RX_ER is not used
[2] if TX_ER is not used

Only available GPIOs can be used at any time. Configuration settings for GPIOs that are not available are ignored.

Each GPIO can be freely assigned to a function. The available functions are LED, PTP (timestamping) and Misc. The function is assigned via the FUNC_SELECT field in the associated GPIOx_FUNC_CONFIG registers (see Section 7.4.1.143).

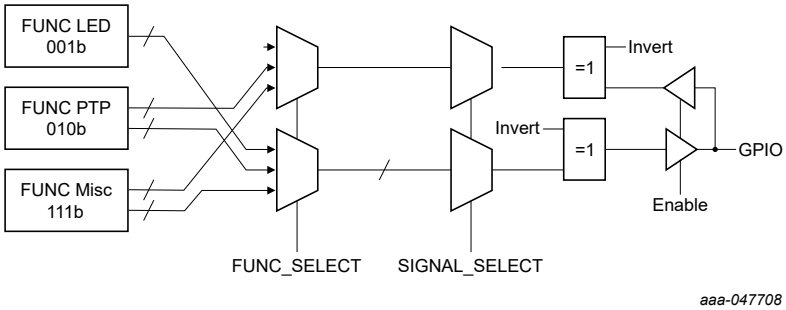


Figure 37. GPIO controller function/signal hierarchy

A number of signals are associated with each function. For example, multiple internal signals are associated with the LED function. Which internal signal is mapped to the associated GPIO is configured via bits SIGNAL_SELECT, as illustrated in Figure 37.

SIGNAL_SELECT to FUNC_SELECT mapping is detailed in Table 28.

Table 28. GPIO function and signal selection[1]

Function	Signal	FUNC_ SELECT	SIGNAL_ SELECT	Dir.[2]	Description
LED	LED0_A	001b	00000b	O	LED controller 0, channel A
	LED0_B	001b	00001b	O	LED controller 0, channel B
	LED1_A	001b	00010b	O	LED controller 1, channel A
	LED1_B	001b	00011b	O	LED controller 1, channel B
	LED2_A	001b	00100b	O	LED controller 2, channel A
	LED2_B	001b	00101b	O	LED controller 2, channel B
	LED3_A	001b	00110b	O	LED controller 3, channel A
	LED3_B	001b	00111b	O	LED controller 3, channel B
	reserved	001b	*others*	Z	—
PTP	PTP_SYNC	010b	00000b	I	PTP synchronization input (PPS in)
	PTP_TRIGGER	010b	00001b	I	external PTP timestamp trigger signal
	TX_SOF	010b	10000b	0	transmit start of frame (SOF) timestamp trigger
	RX_SOF	010b	10001b	I	receive start of frame (SOF) timestamp trigger
	PPS_OUT	010b	10010b	O	Recovered PPS output
	reserved	010b	*others*		
Misc	REGISTER_OUT	111b	10000b	O	GPIO_OUTPUTS register drives pin
	REF_CLK_OUT	111b	10001b	O	25 MHz REF_CLK_OUT output is enabled. Only available on GPIO9

Table 28. GPIO function and signal selection[1]*...continued*

Function	Signal	FUNC_ SELECT	SIGNAL_ SELECT	Dir.[2]	Description
	TX_CLK_OUT	111b	10010b	O	Test clock output.
	reserved	111b	*others*	Z	—

[1] See GPIO0_FUNC_CONFIG register in Table 199
[2] O: output, I: input, Z: high-Z

Bit ENABLE in Table 199 acts as a qualifier. If an output function and ENABLE = 0, the GPIO pin will be LOW. If an input function is selected and ENABLE = 1, the GPIO pin will also be LOW.

If GPIOx_FUNC_CONFIG[FUNC_SELECT] is set to 'reserved', the GPIO is configured as an input and the pin is tristated.

If multiple GPIOs are assigned to the same function/signal, the inputs are ORed.

Note: *In order to disable RX_ER and TX_ER MII/RMII functionality and free these pins for GPIO operation, bits RXER_GPIO_SWAP and TXER_GPIO_SWAP in Table 249 must be set. After a device reset, the MII/RMII function defaults to TX_ER and RX_ER enabled.*

6.16.3 IO driver configuration

MDIO, xMII, and GPIO CMOS drivers are software configurable. The slew rate and drive strength can be adjusted. Table 29 provides an overview of the registers used to configure the slew rate and drive strength (via bits SLEW_RATE and DRIVE_STRENGTH) for specific pins.

Table 29. IO driver configuration

Register	Pins / Function
GPIO_IO_CONFIG (Table 197)	All other GPIO function
GPIO_IO_CLK_CONFIG (Table 198)	GPIO configured for REF_CLK_OUT, TX_CLK_OUT modes
SMI_DATA_IO_CONFIG (Table 92)	MDIO pin
XMII_CLK_IO_CONFIG (Table 248)	MII: TX_CLK, RX_CLK revRMII: REF_CLK RGMII: RXC
XMII_DATA_IO_CONFIG (Table 250)	MII/RMII/RGMII RXD and TXD pins

The device selects the drive characteristics automatically for the selected xMII/VDDIO combination. Using default settings, it can drive a 25 pF capacitive load. If the MAC device is physically close to the PHY and trace length is short (< 15 pF capacitive load), an optimized driver configuration can be used. This option is selected by setting bit ALTERNATE_CONFIG in Table 250. This function changes the configuration for all xMII data and control pins.

The default configuration can be overridden by setting bit MANUAL_CONFIG in the respective register. The slew rate can be to set to a value between 0 (slowest) and 7 (fastest). The drive strength can be set to a value between 0 (weakest) and 7 (strongest).

Pins INT_N, INH, WAKE_IN_OUT cannot be configured.

Note: *Changing the slew rate and/or drive strength impacts the xMII/MDIO timing. Custom settings do not guarantee compliance with MDIO/MII/RMII/RGMII standards.*

7 Registers

Ignore reserved register fields on read. For reserved fields in write-access registers, the reset value is indicated in the Value column or, in the case of fields for which all possible values are enumerated, by an * after the value.

Registers are mapped into five groups.

- CL22: MDIO interface registers (IEEE 802.3 Clause 22 and Clause 45)
- PMA registers (MMD 01)
- PCS registers (MMD 03)
- NXP vendor-specific registers (MMD 30)
- Shared registers

7.1 CL22

See Section 6.7.5 for an explanation of C22 register mapping and how to access these registers using either Clause 22 or Clause 45 access.

7.1.1 Register description

Table 30. Register overview: C22

Address	Name	Access	Reset	Description
8002h	PHY_ID_1	R	1Bh	PHY Identification 1 register
8003h	PHY_ID_2	R	B013h	PHY Identification 2 register
800Dh	CL45_ACCESS_CONTROL	RW	0h	CL45 access control register
800Eh	CL45_ADDRESS_DATA	RW	0h	CL45 address data register
8014h	FAVORITE_IRQS	RW	0h	Favorite IRQs register
801Eh	CL45_ADDRESS	RW	0h	CL45 address register
801Fh	ALWAYS_ACCESSIBLE	RW	0h	Always-accessible global functions register. This register is accessible also in sleep mode, assuming the VDDIO is powered.

7.1.1.1 PHY_ID_1 register

Table 31. PHY_ID_1 register - PHY Identification 1 register (address 8002h)

Bit	Symbol	Access	Value	Description
15:0	OUI_BITS_3_TO_18	R	1Bh	OUI bits [3:18] OUI = 00:60:37

7.1.1.2 PHY_ID_2 register

Table 32. PHY_ID_2 register - PHY Identification 2 register (address 8003h)

Bit	Symbol	Access	Value	Description
15:10	OUI_BITS_19_TO_24	R	2Ch	OUI bits [19:24] OUI = 00:60:37
9:4	MODEL	R	1h	6-bit PHY model number
3:0	REVISION	R	3h	4-bit PHY revision number

7.1.1.3 CL45_ACCESS_CONTROL register

Table 33. CL45_ACCESS_CONTROL register - CL45 access control register (address 800Dh)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:14	OP	RW		MDIO operation
			00*	address
			01	data, no post increment
			10	data, post increment on reads and writes
			11	data, post increment on writes only
13:5	*reserved*	R	0h	Always write all 0s, ignore on read.
4:0	MMD	RW		MMD selection
			1Eh	NXP-specific
			1h	PMA/PMD
			3h	PCS
			others	Reserved

7.1.1.4 CL45_ADDRESS_DATA register

Table 34. CL45_ADDRESS_DATA register - CL45 address data register (address 800Eh)

Bit	Symbol	Access	Value	Description
15:0	ADDRESS_DATA	RW	0h	Address or data of the CL45 transaction, depending on OP selection.

7.1.1.5 FAVORITE_IRQS register

Table 35. FAVORITE_IRQS register - Favorite IRQs register (address 8014h)

Bit	Symbol	Access	Value	Description
15:9	*reserved*	R	0h	always write all 0s, ignore on read.
8	SGMII_LINK_ EVENT	RW	0h	set to flag a change in SGMII Link Status
7	*reserved*	R	0h	always write 0, ignore on read.
6	INGRESS_TS_IRQ	R	0h	If set, time-stamp(s) available of received PTP frame(s) in INGRESS buffer.
5	EGRESS_TS_IRQ	R	0h	If set, time-stamp(s) available of transmitted PTP frame(s) in EGRESS buffer.
4	WAKE_SLEEP_ EVENT	RW	0h	If set, change of PHY Wake-Sleep status bit(s)
3	LINK_AVAILABLE_ EVENT	RW	0h	If set, change of LINK_AVAILABLITY
2	*reserved*	R	0h	Always write 0, ignore on read.
1	PORT_IRQ	R	0h	If set, Interrupts pending for this PORT
0	GLOBAL_IRQS	R	0h	If set, Interrupts pending in Global interrupt tree

7.1.1.6 CL45_ADDRESS register

Table 36. CL45_ADDRESS register - CL45 address register (address 801Eh)

Bit	Symbol	Access	Value	Description
15:0	ADDRESS	RW	0h	Current address pointer of the MMD selected by CL45_ACCESS_CONTROL[MMD]

7.1.1.7 ALWAYS_ACCESSIBLE register

Table 37. ALWAYS_ACCESSIBLE register - Always-accessible global functions register (address 801Fh)[1]

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	WU_SMI	RW	0h	If set, Wake-up the device/sub-system by SMI. VDDIO must be present
14:6	*reserved*	R	0h	Always write all 0s, ignore on read.
5	REFCLK_WARN	R	0h	If this bit is set, a warning is present in OP_CONDITIONS_IRQ_MSTATUS[OSC_WARN] or in PORT_LEVEL_IRQ_MSTATUS[TXC_CLK_WARN] in case of RMII-clkmode. To clear this bit, the respective source IRQs must be cleared.
4	FUSA_PASS_IRQ	RW	0h	If set, FUSA check has successfully passed.
3	CORE_SUPPLY_WARN	RW	0h	This bit is asserted upon detection of a fault condition by the core supply monitor. Status register MMD30.CORE_SUPPLY_STATUS located in MMD30 contains details about the fault type. Note that reading register MMD30.CORE_SUPPLY_STATUS requires CORE_SUPPLY_STATUS=1. The IRQ is edge triggered. If the trigger condition persist the IRQ will not be immediately refired when cleared.
2	CORE_SUPPLY_STATUS	R	0h	This bit shows the actual status of the core supply voltage. If the bit is asserted, the voltage is within the tolerated voltage range.
1	LIMITED_ACCESS	R		Indicates whether there is limited device access because the device is sleeping.
			0*	All registers are available for read and write
			1	If CORE_SUPPLY_STATUS=0, registers (except the ALWAYS_ACCESSIBLE) are inaccessible and read zero. If CORE_SUPPLY_STATUS=1 and device is not in sleep with INH deasserted, all registers are readable, the ALWAYS_ACCESSIBLE register is writable.
0	INHIBIT_STATUS	R	0h	This bit indicates the overall inhibit status, that determines if this device drives the INH pin high.

[1] This register is accessible also in sleep mode, assuming the VDDIO is powered.

7.2 MMD1

7.2.1 Register description

Table 38. Register overview: MMD1

Address	Name	Access	Reset	Description
0h	PMA_CONTROL1	RW	2000h	PMA control 1 register
1h	PMA_STATUS1	R	2h	PMA status 1 register
4h	PMA_SPEED_ABILITY	R	20h	PMA speed ability register
7h	PMA_CONTROL2	R	3Dh	PMA control 2 register
8h	PMA_STATUS2	R	9301h	PMA status 2 register
9h	PMD_TRANSMIT_DISABLE	RW	0h	PMD transmit disable register
Ah	PMD_RCV_DETECT	R	0h	PMD receive signal detect register
Bh	PMA_EXTENDED_ ABILITIES	R	800h	PMA extended abilities
12h	BASE_T1_PMA_XTD_ ABILITY	R	1h	BASE-T1 PMA extended abilities register
834h	BASE_T1_PMA_CONTROL	RW	8000h	BASE-T1 PMA control register
836h	E100BT1_PMA_TEST_ CONTROL	RW	0h	100BASE-T1 PMA test control register

7.2.1.1 PMA_CONTROL1 register

Table 39. PMA_CONTROL1 register - PMA control 1 register (address 0h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	RESET	RW		Reset This bit is self-clearing.
			0*	Normal operation
			1	On write a PHY reset is asserted. On read this indicates that a reset is still in progress
14	*reserved*	R	0h	Always write 0, ignore on read.
13	SPEED_SELECT_ LSB	R	1h	see SPEED_SELECT_MSB
12	*reserved*	R	0h	Always write 0, ignore on read.
11	LOW_POWER	RW	0h	If set, the PMA enters low power mode Note: PMA LOW_POWER (MMD1) and PCS LOW_POWER (MMD3) controls have mirrored behaviour. If one is written the other follows.
10:7	*reserved*	R	0h	Always write 0000, ignore on read.
6	SPEED_SELECT_ MSB	R		Speed selection [SPEED_SELECT_MSB, SPEED_SELECT_LSB] are encoded as follows:
			00*	10 Mbit/s (not supported)

Table 39. PMA_CONTROL1 register - PMA control 1 register (address 0h)*...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
			01	100 Mbit/s
			10	1000 Mbit/s (not supported)
			11	Reserved
5:2	SPEED_SELECT_XTD	R		Always write 0000, ignore on read.
			0000*	10 Gbit/s
			0001	10PASS-TS/2BASE-TL
			0010	40 Gbit/s
			0011	100 Gbit/s
			0100	25 Gbit/s
			0101	Reserved
			0110	2.5 Gbit/s
			0111	5 Gbit/s
			1000	200 Gbit/s
			1001	400 Gbit/s
			101x	Reserved
			11xx	Reserved
1	REMOTE_LOOPBACK	RW	0h	Enable PMA remote loopback mode.
0	LOCAL_LOOPBACK	RW	0h	Enable PMA loopback mode.

7.2.1.2 PMA_STATUS1 register

Table 40. PMA_STATUS1 register - PMA status 1 register (address 1h)

Bit	Symbol	Access	Value	Description
15:10	*reserved*	R	0h	Ignore on read.
9	PIASA	R	0h	PMA ingress AUI stop ability
8	PEASA	R	0h	PMA egress AUI stop ability
7	FAULT	R	0h	If set, fault condition detected
6:3	*reserved*	R	0h	Ignore on read.
2	RECEIVE_LINK_STATUS	R	0h	If set, PMA/PMD receive link up. This bit is latched low. This bit is latched-low.
1	LOW_POWER_ABILITY	R	1h	If set, PCS supports low-power mode
0	*reserved*	R	0h	Ignore on read.

7.2.1.3 PMA_SPEED_ABILITY register

Table 41. PMA_SPEED_ABILITY register - PMA speed ability register (address 4h)

Bit	Symbol	Access	Value	Description
15:6	*reserved*	R	0h	Ignore on read.
5	ABILITY_100M	R	1h	If set, PMA/PMD is capable of operating at 100 Mbit/s
4:0	*reserved*	R	0h	Ignore on read.

7.2.1.4 PMA_CONTROL2 register

Table 42. PMA_CONTROL2 register - PMA control 2 register (address 7h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:7	*reserved*	R	0h	Ignore on read.
6:0	TYPE_SELECT	R		Type selection
			0111101*	BASE-T1 PMA/PMD
			others	Reserved, ignore on read

7.2.1.5 PMA_STATUS2 register

Table 43. PMA_STATUS2 register - PMA status 2 register (address 8h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:14	DEVICE_PRESENT	R		Device present
			0x	No device responding at this address
			10*	Device responding at this address
			x1	No device responding at this address
13	TRANSMIT_FAULT_ABILITY	R	0h	If set, PMA/PMD has the ability to detect a fault condition on the transmit path
12	RECEIVE_FAULT_ABILITY	R	1h	If set, PMA/PMD has the ability to detect a fault condition on the receive path
11	*reserved*	R	0h	Ignore on read.
10	RECEIVE_FAULT	R	0h	If set, fault condition on receive path This flag is cleared on read. This bit is latched-high.
9	EXTENDED_ABILITIES	R	1h	If set, PMA/PMD has extended abilities listed in PMA_EXTENDED_ABILITIES
8	PMD_TRANSMIT_DISABLE	R	1h	If set, PMD has the ability to disable the transmit path
7:1	*reserved*	R	0h	Ignore on read.
0	PMA_LOCAL_LOOPBACK_ABILITY	R	1h	If set, PMA has the ability to perform a local loopback function

7.2.1.6 PMD_TRANSMIT_DISABLE register

Table 44. PMD_TRANSMIT_DISABLE register - PMD transmit disable register (address 9h)

Bit	Symbol	Access	Value	Description
15:1	*reserved*	R	0h	Always write all 0s, ignore on read.
0	TX_DISABLE	RW	0h	Transmit disable This setting is test protected.

7.2.1.7 PMD_RCV_DETECT register

Table 45. PMD_RCV_DETECT register - PMD receive signal detect register (address Ah)

Bit	Symbol	Access	Value	Description
15:1	*reserved*	R	0h	Ignore on read.
0	RCV_SIGNAL_ DETECT	R	0h	If set, signal detected on receive

7.2.1.8 PMA_EXTENDED_ABILITIES register

Table 46. PMA_EXTENDED_ABILITIES register - PMA extended abilities (address Bh)

Bit	Symbol	Access	Value	Description
15	XTD_ABILITIES_ BASE_H	R	0h	If set, PMA/PMD has BASE-H extended abilities
14	XTD_ABILITIES_2 G5_5G	R	0h	If set, PMA/PMD has 2.5G/5G extended abilities
13	XTD_ABILITIES_ 200G_400G	R	0h	If set, PMA/PMD has 200G/400G extended abilities
12	XTD_ABILITIES_25 G	R	0h	f set, PMA/PMD has 25G extended abilities
11	XTD_ABILITIES_ BASE_T1	R	1h	If set, PMA/PMD has BASE-T1 extended abilities
10	XTD_ABILITIES_40 G_100G	R	0h	If set, PMA/PMD has 40G/100G extended abilities
9	ABILITY_P2MP	R	0h	If set, PMA/PMD has P2MP abilities
8	ABILITY_10BASE_T	R	0h	If set, PMA/PMD is able to perform 10BASE-T
7	ABILITY_100BASE_ TX	R	0h	If set, PMA/PMD is able to perform 100BASE-TX
6	ABILITY_1000 BASE_KX	R	0h	If set, PMA/PMD is able to perform 1000BASE-KX
5	ABILITY_1000 BASE_T	R	0h	If set, PMA/PMD is able to perform 1000BASE-T
4	ABILITY_10 GBASE_KR	R	0h	If set, PMA/PMD is able to perform 10GBASE-KR
3	ABILITY_10 GBASE_KX4	R	0h	If set, PMA/PMD is able to perform 10GBASE-KX4
2	ABILITY_10 GBASE_T	R	0h	If set, PMA/PMD is able to perform 10GBASE-T

Table 46. PMA_EXTENDED_ABILITIES register - PMA extended abilities (address Bh)*...continued*

Bit	Symbol	Access	Value	Description
1	ABILITY_10 GBASE_LRM	R	0h	If set, PMA/PMD is able to perform 10GBASE-LRM
0	ABILITY_10 GBASE_CX4	R	0h	If set, PMA/PMD is able to perform 10GBASE-CX4

7.2.1.9 BASE_T1_PMA_XTD_ABILITY register

Table 47. BASE_T1_PMA_XTD_ABILITY register - BASE-T1 PMA extended abiltities register (address 12h)

Bit	Symbol	Access	Value	Description
15:2	*reserved*	R	0h	Ignore on read.
1	ABILITY_1000 BASE_T1	R	0h	If set, PMA/PMD is able to perform 1000BASE-T1
0	ABILITY_100BASE_ T1	R	1h	If set, PMA/PMD is able to perform 100BASE-T1

7.2.1.10 BASE_T1_PMA_CONTROL register

Table 48. BASE_T1_PMA_CONTROL register - BASE-T1 PMA control register (address 834h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	MANUAL_LEADER_ FOLLOWER_ CONFIG	R	1h	Returns a one to indicate that Leader or Follower configuration is set manually. This value is always 1
14	LEADER_ FOLLOWER	RW		Leader/Follower selection This setting is preserved during deep sleep. This setting is configuration protected.
			0*	Follower
			1	Leader
13:4	*reserved*	R	0h	Always write all 0s, ignore on read.
3:0	MODE	R		only 100BASE-T1 is supported
			0000*	100BASE-T1
			0001	1000BASE-T1
			others	reserved

7.2.1.11 E100BT1_PMA_TEST_CONTROL register

Table 49. E100BT1_PMA_TEST_CONTROL register - 100BASE-T1 PMA test control register (address 836h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:13	PMA_TEST_MODE	RW		Selects the PMA test mode. Ignore PHY_STATUS if a test mode is enabled. This setting is configuration protected.
			000*	Normal operation

Table 49. E100BT1_PMA_TEST_CONTROL register - 100BASE-T1 PMA test control register (address 836h)*...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
			001	Test mode 1
			010	Test mode 2
			100	Test mode 4
			101	Test mode 5
			111	Drive SEND_Z
			others	reserved
12:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.3 MMD3

7.3.1 Register description

Table 50. Register overview: MMD3

Address	Name	Access	Reset	Description
0h	PCS_CONTROL1	RW	2000h	PCS control 1 register
1h	PCS_STATUS1	R	2h	PCS status 1 register
4h	PCS_SPEED_ABILITY	R	0h	PCS speed ability register
8h	PCS_STATUS2	R	8000h	PCS status 2 register

7.3.1.1 PCS_CONTROL1 register

Table 51. PCS_CONTROL1 register - PCS control 1 register (address 0h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	RESET	RW	[1]	Reset This bit is self-clearing.
			0*	Normal operation
			1	On write a PHY reset is asserted. On read this indicates that a reset is still in progress
14	LOOPBACK	RW	0h	If set, Enable loopback mode Note, PCS loopback will overrule all PMA loopback modes
13	SPEED_SELECT_LSB	R	1h	see SPEED_SELECT_MSB
12	*reserved*	R	0h	Always write 0, ignore on read.
11	LOW_POWER	RW	0h	If set, the PCS enters low power mode Note: PMA LOW_POWER (MMD1) and PCS LOW_POWER (MMD3) controls have mirrored behaviour. If one is written the other follows.
10:7	*reserved*	R	0h	Always write 0000, ignore on read.

Table 51. PCS_CONTROL1 register - PCS control 1 register (address 0h)*...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
6	SPEED_SELECT_MSB	R		Speed selection [SPEED_SELECT_MSB, SPEED_SELECT_LSB] are encoded as follows:
			00	10 Mbit/s (not supported)
			01*	100 Mbit/s
			10	1000 Mbit/s (not supported)
			11	Reserved
5:2	Reserved	R		Extended speed selection Always write 0000, ignore on read.
			0000*	10Gbit/s
			0001	10PASS-TS/2BASE-TL
			others	Reserved
1:0	*reserved*	R	0h	Always write 00, ignore on read.

[1] In follower mode with polarity detection and correction enabled, use PMA reset instead.

7.3.1.2 PCS_STATUS1 register

Table 52. PCS_STATUS1 register - PCS status 1 register (address 1h)

Bit	Symbol	Access	Value	Description
15:8	*reserved*	R	0h	Ignore on read.
7	FAULT_CONDITION	R	0h	If set, fault condition detected
6:3	*reserved*	R	0h	Ignore on read.
2	RCV_LINK_STATUS_LL	R	0h	If set, PCS receive link up. Latched low This bit is latched-low.
1	LOW_POWER_ABILITY	R	1h	If set, PCS supports low-power mode
0	*reserved*	R	0h	Ignore on read.

7.3.1.3 PCS_SPEED_ABILITY register

Table 53. PCS_SPEED_ABILITY register - PCS speed ability register (address 4h)

Bit	Symbol	Access	Value	Description
15:10	*reserved*	R	0h	Ignore on read.
9	ABILITY_400G	R	0h	If set, PCS is capable of operating at 400 Gbit/s
8	ABILITY_200G	R	0h	If set, PCS is capable of operating at 200 Gbit/s
7	ABILITY_5G	R	0h	If set, PCS is capable of operating at 5 Gbit/s
6	ABILITY_2500M	R	0h	If set, PCS is capable of operating at 2.5 Gbit/s
5	*reserved*	R	0h	Ignore on read.
4	ABILITY_25G	R	0h	If set, PCS is capable of operating at 25 Gbit/s

Table 53. PCS_SPEED_ABILITY register - PCS speed ability register (address 4h)*...continued*

Bit	Symbol	Access	Value	Description
3	ABILITY_100G	R	0h	If set, PCS is capable of operating at 100 Gbit/s
2	ABILITY_40G	R	0h	If set, PCS is capable of operating at 40 Gbit/s
1	ABILITY_10P_2B	R	0h	If set, PCS is capable of operating as the 10P/2B PCS
0	ABILITY_10G	R	0h	If set, PCS is capable of operating at 10 Gbit/s

7.3.1.4 PCS_STATUS2 register

Table 54. PCS_STATUS2 register - PCS status 2 register (address 8h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:14	DEVICE_PRESENT	R		Device present
			10*	Device responding at this address
			others	No device responding at this address
13:12	*reserved*	R	0h	Ignore on read.
11	TRANSMIT_FAULT	R	0h	If set, PCS transmit fault conditions detected. Latched high - TX_ER detected HIGH while TX_EN was set HIGH This flag is cleared on read. This bit is latched-high.
10	RECEIVE_FAULT	R	0h	If set, PCS receive fault conditions detected. Latched high - RX_ER was high during RX_DV HIGH period - SSD/ESD error detection - Jab_detect asserted - scrambler lock drop This flag is cleared on read. This bit is latched-high.
9:0	*reserved*	R	0h	Ignore on read.

7.4 MMD30

7.4.1 Register description

Table 55. Register overview: MMD30

Address	Name	Access	Reset	Description
4h	DEVICE_IDENTIFIER3	R	TJF1103A: 1091h	Device identifier register 3
			TJF1103B: 2401h	
8h	MMD30_STATUS	R	8000h	MMD30 status register
40h	DEVICE_CONTROL	RW	0h	Device control register
42h	DEVICE_STATUS	R	0h	Device status register
44h	DEVICE_STATUS_ LATCHED	RW	0h	Device status latched register
46h	DEVICE_ABILITIES	RW	TJF1103A: 0h	Device ability register

Table 55. Register overview: MMD30*...continued*

Address	Name	Access	Reset	Description
			TJF1103B: 808h	
47h	DEVICE_PROPERTIES	R	1h	Device properties register
48h	DEVICE_CONFIG	RW	8000h	Device config register
49h	DEVICE_CONFIG_ EXTENDED	RW	0h	Device configuration extended register
70h	PORT_IRQ_STATUS	R	0h	PHY IRQ status register
72h	PORT_IRQ_ENABLE	RW	3h	PORT IRQ enable register
74h	PORT_IRQ_MSTATUS	R	0h	Port masked IRQ status register
80h	GLOBAL_CAT_IRQ_ STATUS	R	0h	Global category IRQ status register
81h	GLOBAL_CAT_IRQ_ ENABLE	RW	134h	Global category IRQ enable register
82h	GLOBAL_CAT_IRQ_ MSTATUS	R	0h	GLobal category IRQ masked status register
90h	OP_CONDITIONS_IRQ_ SOURCE	RW	0h	Operating conditions IRQ source register
91h	OP_CONDITIONS_IRQ_ ENABLE	RW	0h	Operating conditions IRQ enable register
92h	OP_CONDITIONS_IRQ_ MSTATUS	R	0h	Operating conditions IRQ masked status
A0h	TOP_EPHY_IRQ_SOURCE	RW	0h	Top Ethernet PHY IRQ source register
A1h	TOP_EPHY_IRQ_ENABLE	RW	0h	Top Ethernet PHY IRQ enable register
A2h	TOP_EPHY_IRQ_MSTATUS	R	0h	Top Ethernet PHY IRQ masked status register
B0h	FUNC_SHARED_IRQ_ SOURCE	RW	0h	Global shared function IRQ source register
B1h	FUNC_SHARED_IRQ_ ENABLE	RW	0h	Global shared function IRQ enable register
B2h	FUNC_SHARED_IRQ_ MSTATU	RW	0h	Global shared function IRQ masked status register
C0h	CONFIG_REGXS_IRQ_ SOURCE	RW	0h	Configuration register access IRQ source register
C1h	CONFIG_REGXS_IRQ_ ENABLE	RW	0h	Configuration register access IRQ enable register
C2h	CONFIG_REGXS_IRQ_ MSTATUS	R	0h	Configuration register access IRQ masked status register
100h	BROADCAST	RW	0h	Broadcast control register
101h	PORT1_CONFIG	RW	C001h	Port 1 configuration register
180h	WISE_CONTROL	RW	1h	Wake, inhibit and sleep control register
181h	WISE_STATUS	RW	0h	Wake, inhibit and sleep status register

Table 55. Register overview: MMD30*...continued*

Address	Name	Access	Reset	Description
182h	WISE_CONFIG	RW	3000h	Wake, inhibit and sleep configuration register
184h	WISE_PARAMETERS	RW	1h	Wake, inhibit and sleep parameters register
189h	SMI_STATUS	RW	0h	SMI status register
18Ah	SMI_CONFIG	RW	8000h	SMI config register
18Ch	SMI_DATA_IO_CONFIG	RW	0h	SMI Data IO configuration register
190h	GLOBAL_LED_TRIGGER0	RW	0h	LED trigger 0
191h	GLOBAL_LED_TRIGGER1	RW	0h	LED trigger 1
192h	GLOBAL_LED_TRIGGER2	RW	0h	LED trigger 2
193h	GLOBAL_LED_TRIGGER3	RW	0h	LED trigger 3
1A0h	LED0_CONFIG	RW	C00Ch	LED Controller 0 Configuration
1A1h	LED0_TRIG_SOURCE	RW	21h	LED controller 0 trigger source selection
1A2h	LED0_TRIG01_CONFIG	RW	TJF1103A: 60E0h TJF1103B: E0E0h	LED controller 0 Trigger 0 and 1 configuration
1A3h	LED0_TRIG23_CONFIG	RW	TJF1103A: E060h TJF1103B: 00E0h	LED controller 0 Trigger 2 and 3 configuration
1A4h	LED1_CONFIG	RW	C00Ch	LED Controller 1 Configuration
1A5h	LED1_TRIG_SOURCE	RW	21h	LED controller 1 trigger source selection
1A6h	LED1_TRIG01_CONFIG	RW	E0E0h	LED controller 1 Trigger 0 and 1 configuration
1A7h	LED1_TRIG23_CONFIG	RW	TJF1103A: E0E0h TJF1103B: 00E0h	LED controller 1 Trigger 2 and 3 configuration
1A8h	LED2_CONFIG	RW	C00Ch	LED Controller 2 Configuration
1A9h	LED2_TRIG_SOURCE	RW	21h	LED controller 2 trigger source selection
1AAh	LED2_TRIG01_CONFIG	RW	E0E0h	LED controller 2 Trigger 0 and 1 configuration
1ABh	LED2_TRIG23_CONFIG	RW	TJF1103A: E0E0h TJF1103B: 00E0h	LED controller 2 Trigger 2 and 3 configuration
1ACh	LED3_CONFIG	RW	C00Ch	LED Controller 3 Configuration
1ADh	LED3_TRIG_SOURCE	RW	21h	LED controller 3 trigger source selection
1AEh	LED3_TRIG01_CONFIG	RW	E0E0h	LED controller 3 Trigger 0 and 1 configuration
1AFh	LED3_TRIG23_CONFIG	RW	TJF1103A: E0E0h TJF1103B: 00E0h	LED controller 3 Trigger 2 and 3 configuration
311h	AO_SYSTEM_SUPPLY_STATUS	RW	0h	Always on system supply
313h	CORE_SUPPLY_STATUS	RW	0h	Core supply status

Table 55. Register overview: MMD30*...continued*

Address	Name	Access	Reset	Description
315h	VDDIO_SUPPLY_STATUS	RW	0h	VDDIO supply status
318h	VREGD_SUPPLY_STATUS	RW	0h	VREGD supply status
319h	VREGA_SUPPLY_STATUS	RW	0h	VREGA supply status
31Ah	VDDA_TRX_SUPPLY	RW	0h	VDDA_TRX supply status
31Eh	OSC_STATUS	RW	0h	XO status
31Fh	TEMP_STATUS	RW	A1h	Temperature status
3F4h	COMPL_TEST_INTF	RW	100h	Compliance test interface
1100h	PTP_IDENTIFIER	R	10h	PTP IP identifier register
1101h	PTP_CONTROL	RW	0h	General control
1102h	PTP_CONFIG	RW	0h	General control
1103h	PTP_ABILITY	R	6h	PTP IP Ability registers
1104h	PTP_CLK_PERIOD	RW	8h	Clock period of ptp_clk
1105h	LTC_LOAD_CTRL	RW	0h	LTC load and read control
1106h	LTC_WR_NSEC_0	RW	0h	Loading nanoseconds counter value
1107h	LTC_WR_NSEC_1	RW	0h	Loading nanoseconds counter value
1108h	LTC_WR_SEC_0	RW	0h	Loading seconds counter value
1109h	LTC_WR_SEC_1	RW	0h	Loading seconds counter value
110Ah	LTC_RD_DATA_0	R	0h	Local LTC nanoseconds part. The value read is the saved value of local counter when READ_LTC is set.
110Bh	LTC_RD_DATA_1	R	0h	Local LTC nanoseconds part. The value read is the saved value of local counter when READ_LTC is set.
110Ch	LTC_RD_DATA_2	R	0h	Local LTC seconds part. The value read is the saved value of local counter when READ_LTC is set.
110Dh	LTC_RD_DATA_3	R	0h	Local LTC seconds part. The value read is the saved value of local counter when READ_LTC is set.
110Eh	LTC_RD_DATA_4	R	0h	Local LTC sub-nanoseconds part. The value read is the saved value of local counter when READ_LTC is set.
110Fh	RATE_ADJ_SUBNS_0	RW	0h	SW Rate adjust value
1110h	RATE_ADJ_SUBNS_1	RW	0h	SW Rate adjust value
1111h	TEMP_ADJ_SUBNS_0	RW	0h	SW temporary rate adjust value
1112h	TEMP_ADJ_SUBNS_1	RW	0h	SW temporary rate adjust value
1113h	TEMP_ADJ_DUR_0	RW	0h	Temporary adjustment window
1114h	TEMP_ADJ_DUR_1	RW	0h	Temporary adjustment window
1115h	HW_LTC_LOCK_CTRL	RW	1h	HW LTC self locking.control

Table 55. Register overview: MMD30*...continued*

Address	Name	Access	Reset	Description
1116h	HW_EXT_PPS_NS_0	RW	CA00h	Period of external PPS sync in nanosecond. Used for HW LTC self locking.
1117h	HW_EXT_PPS_NS_1	RW	3B9Ah	Period of external PPS sync in nanosecond. Used for HW LTC self locking.
1118h	HW_LOCK_ER_LMT_0	RW	D090h	Error limitation by HW LTC self locking engine
1119h	HW_LOCK_ER_LMT_1	RW	3h	Error limitation by HW LTC self locking engine
111Ah	LTC_LOOP_CONTROL	RW	303h	This register defines control parameters to adapt behavior of the LTC loop if HW_LTC_LOCK_EN=1
111Bh	EXT_PPS_TS_DATA0	R	0h	Timestamping data on the event of rising edge of external pps signal. Reading this register copied into snapshot register for multiple reads of EXT_PPS_TS_DATA0/1/2/3/4/5 register
111Ch	EXT_PPS_TS_DATA1	R	0h	Timestamping data on the event of rising edge of external pps signal.
111Dh	EXT_PPS_TS_DATA2	R	0h	Timestamping data on the event of rising edge of external pps signal.
111Eh	EXT_PPS_TS_DATA3	R	0h	Timestamping data on the event of rising edge of external pps signal.
111Fh	EXT_PPS_TS_DATA4	R	0h	Timestamping data on the event of rising edge of external pps signal.
1120h	EXT_PPS_TS_CTRL	RW	0h	External PPS timestamp reading done
1121h	EXT_TRG_TS_DATA0	R	0h	Timestamping data on the event of rising edge on external trigger event signal. Reading this register copied into snapshot register for multiple reads of EXT_TRG_TS_DATA0/1/2/3/4/5 register
1122h	EXT_TRG_TS_DATA1	R	0h	Timestamping data of external trigger event signal.
1123h	EXT_TRG_TS_DATA2	R	0h	Timestamping data of external trigger event signal.
1124h	EXT_TRG_TS_DATA3	R	0h	Timestamping data of external trigger event signal.
1125h	EXT_TRG_TS_DATA4	R	0h	Timestamping data of external trigger event signal.
1126h	EXT_TRG_TS_CTRL	RW	0h	External trigger event timestamp reading done
1130h	PTP_IRQ_SOURCE	RW	0h	Interrupt status signals
1131h	PTP_IRQ_ENABLE	RW	0h	Interrupt enable control
1132h	PTP_IRQ_MSTATUS	R	0h	Interrupt status signals

Table 55. Register overview: MMD30*...continued*

Address	Name	Access	Reset	Description
1140h	PKT_FILT_CTRL	RW	0h	Ingress or egress packet filtering
1141h	DA_FILT_CTRL	RW	3h	Ingress or egress packet DA filtering.
1142h	USER_MAC_DA_0	RW	0h	[15:0] of User defined MAC address
1143h	USER_MAC_DA_1	RW	0h	[31:16] of User defined MAC address
1144h	USER_MAC_DA_2	RW	0h	[47:32] of User defined MAC address
1145h	USER_DA_MASK_0	RW	0h	User MAC DA Mask control
1146h	USER_DA_MASK_1	RW	0h	User MAC DA Mask control
1147h	USER_DA_MASK_2	RW	0h	User MAC DA Mask control
1148h	EVENT_MSG_FILT	RW	Fh	PTP event message consideration
1149h	TX_PIPE_DLY_NS	RW	0h	Egress data path latency from timestamping point of SOF signal to mdi (nanoseconds part).
114Ah	TX_PIPEDLY_SUBNS	RW	0h	Egress data path latency from timestamping point of SOF signal to mdi (sub-nanoseconds part)
114Bh	RX_PIPE_DLY_NS	RW	0h	Ingress data path latency of SOF signal from MDI line to timestamping point (nanoseconds part).
114Ch	RX_PIPEDLY_SUBNS	RW	0h	Ingress data path latency of SOF signal from MDI line to timestamping point (sub-nanoseconds part)
114Dh	RX_TS_INSRT_CTRL	RW	11h	Inband timestamp insertion controls at ingress path
114Eh	EGR_RING_DATA_0	R	0h	Timestamping data of egress ptp event message. Reading this register fetches and latches buffered timestamp data set and puts into EGR_RING_DATA_ 0/1/2/3/4/5
114Fh	EGR_RING_DATA_1	R	0h	Timestamping data of egress ptp event message.
1150h	EGR_RING_DATA_2	R	0h	Timestamping data of egress ptp event message.
1151h	EGR_RING_DATA_3	R	0h	Timestamping data of egress ptp event message.
1152h	EGR_RING_DATA_4	R	0h	Timestamping data of egress ptp event message.
1153h	EGR_RING_DATA_5	R	0h	Timestamping data of egress ptp event message.
1154h	EGR_RING_CTRL	RW	0h	Egress timestamp termination control
1155h	ING_RING_DATA_0	R	0h	Timestamping data of egress ptp event message. Reading this register fetches and latches buffered timestamp data set and puts into ING_RING_DATA_ 0/1/2/3/4/5

Table 55. Register overview: MMD30*...continued*

Address	Name	Access	Reset	Description
1156h	ING_RING_DATA_1	R	0h	Timestamping data of Ingress ptp event message.
1157h	ING_RING_DATA_2	R	0h	Timestamping data of Ingress ptp event message.
1158h	ING_RING_DATA_3	R	0h	Timestamping data of Ingress ptp event message.
1159h	ING_RING_DATA_4	R	0h	Timestamping data of Ingress ptp event message.
115Ah	ING_RING_DATA_5	R	0h	Timestamping data of Ingress ptp event message.
115Bh	ING_RING_CTRL	RW	0h	Ingress timestamp termination control
115Fh	PTP_PKT_RCV_CNT	R	0h	Number of received ptp event packet
1160h	PTP_FCS_ERR_CNT	R	0h	Number of received ptp event packet has fcs error.
2C00h	GLOBAL_INFRA_CONTROL	RW	0h	Global infrastructure control
2C20h	GPIO_OUTPUTS	RW	0h	GPIO output
2C21h	GPIO_STATUS	R	0h	GPIO status
2C22h	GPIO_IO_CONFIG	RW	0h	GPIO IO configuration
2C23h	GPIO_IO_CLK_CONFIG	RW	0h	GPIO IO CLK configuration
2C40h	GPIO0_FUNC_CONFIG	RW	8020h	GPIO0 function configuration (GPIOx function registers are identical to this one)
2C41h	GPIO1_FUNC_CONFIG	RW	8000h	see GPIO0_FUNC_CONFIG
2C42h	GPIO2_FUNC_CONFIG	RW	8000h	see GPIO0_FUNC_CONFIG
2C43h	GPIO3_FUNC_CONFIG	RW	8000h	see GPIO0_FUNC_CONFIG
2C44h	GPIO4_FUNC_CONFIG	RW	8000h	see GPIO0_FUNC_CONFIG
2C45h	GPIO5_FUNC_CONFIG	RW	8000h	see GPIO0_FUNC_CONFIG
2C46h	GPIO6_FUNC_CONFIG	RW	8000h	see GPIO0_FUNC_CONFIG
2C47h	GPIO7_FUNC_CONFIG	RW	8000h	see GPIO0_FUNC_CONFIG
2C48h	GPIO8_FUNC_CONFIG	RW	8000h	see GPIO0_FUNC_CONFIG
2C49h	GPIO9_FUNC_CONFIG	RW	8000h	see GPIO0_FUNC_CONFIG
2C4Ah	GPIO10_FUNC_CONFIG	RW	8000h	see GPIO0_FUNC_CONFIG
2C4Bh	GPIO11_FUNC_CONFIG	RW	8000h	see GPIO0_FUNC_CONFIG
9000h	PORT_PTP_CONTROL	RW	800h	Port PTP control
9200h	PTP_TS_CAPABILITY	R	3h	PTP TS capabilities
9201h	PTP_TS_TX_MAX_DELAY_LSB	R	0h	Maximum PTP pcs transmit path data delay LSBs
9202h	PTP_TS_TX_MAX_DELAY_MSB	R	0h	Maximum PTP pcs transmit path data delay MSBs

Table 55. Register overview: MMD30*...continued*

Address	Name	Access	Reset	Description
9203h	PTP_TS_TX_MIN_DELAY_LSB	R	0h	Minimum PTP pcs transmit path data delay MSBs
9204h	PTP_TS_TX_MIN_DELAY_MSB	R	0h	Minimum PTP pcs transmit path data delay MSBs
9205h	PTP_TS_RX_MAX_DELAY_LSB	R	0h	Maximum PTP pcs receive path data delay LSBs
9206h	PTP_TS_RX_MAX_DELAY_MSB	R	0h	Maximum PTP pcs receive path data delay MSBs
9207h	PTP_TS_RX_MIN_DELAY_LSB	R	0h	Minimum PTP pcs receive path data delay MSBs
9208h	PTP_TS_RX_MIN_DELAY_MSB	R	0h	Minimum PTP pcs receive path data delay MSBs
A800h	PORT_BIST_CONTROL	RW	0h	Port BIST control
A807h	BIST_INTERCEPT_CONFIG	RW	0h	BIST intercept config
A880h	BIST_GEN_CTRL	RW	0h	BIST generator control register
A881h	BIST_GEN_STATUS	R	0h	BIST generator status
A887h	PREAMBLE_IPG_SIZE	RW	700Ch	Preamble and IPG lengths
A888h	BIST_DA_0	RW	0h	lower 16 bits of DA value[15:0]
A889h	BIST_DA_1	RW	0h	middle 16 bits of DA value[31:16]
A88Ah	BIST_DA_2	RW	0h	higher 16 bits of DA value[47:32]
A88Bh	BIST_SA_0	RW	0h	lower 16 bits of SA value[15:0]
A88Ch	BIST_SA_1	RW	0h	middle 16 bits of SA value[31:16]
A88Dh	BIST_SA_2	RW	0h	higher 16 bits of SA value[47:32]
A88Fh	BIST_PTP_CONFIG	RW	0h	PTP frame generation configuration
A890h	BIST_ETHER_TYPE	RW	0h	Ethernet type (T/L)
A891h	PAYLOAD_CONFIG	RW	20A5h	Payload data controls
A892h	PAYLOAD_SIZE	RW	2Eh	Length of frame payload data in bytes
A893h	PRBS_DATA_CONFIG	RW	0h	PRBS data configuration
A894h	BIST_LFSR_SEED	RW	7FFFh	LFSR Seed value
A8A2h	GOOD_FRAMES_PLAN	RW	64h	Number of good frames to be generated by BIST generator
A8A4h	G_GOOD_FRAME_CNT	R	0h	Generated good frames in continuous mode.
A8A6h	BAD_FRAMES_PLAN	RW	0h	Number of bad frames to be generated by BIST generator
A8C0h	BIST_CHECK_CTRL	RW	0h	BIST checker control register
A8C1h	BIST_PROD_STATUS	R	0h	BIST status used when BIST is in production mode and NOT valid for continuous mode

Table 55. Register overview: MMD30*...continued*

Address	Name	Access	Reset	Description
A8C4h	BIST_WAIT_TIMER	RW	FFh	Timer timeout value for checking all status in production mode. This timeout is useful when expected number of generated frames is never received.
A8D0h	R_GOOD_FRAME_CNT	R	0h	Received good frame count
A8D2h	R_BAD_FRAME_CNT	R	0h	Received bad frame count
A8D4h	R_RXER_FRAME_CNT	R	0h	RX_ER detected when rx_dv is set.
AC00h	PORT_INFRA_CONTROL	RW	0h	Port infrastructure control register
AC04h	INFRA_ABILITY	R	8000h	Infrastsructure ability register
AC06h	INFRA_CONFIG	RW	0h	Infrastructure configuration register
AC08h	INFRA_IRQ_SOURCE	RW	0h	Infrastructure IRQ source register
AC0Ah	INFRA_IRQ_ENABLE	RW	0h	Infrastructure IRQ enable register
AC0Ch	INFRA_IRQ_MSTATUS	R	0h	Infrastructure IRQ masked status
AFC0h	XMII_CONTROL	RW	0h	XMII control
AFC2h	XMII_STATUS	RW	0h	XMII status
AFC4h	XMII_ABILITIES	R	TJF1103A: CF00h	XMII abilities
			TJF1103B: 0001h	
AFC5h	SERDES_MII_ABILITIES	R	TJF1103A: 0000h	SERDES MII abilities
			TJF1103B: 0002h	
AFC6h	MII_BASIC_CONFIG	RW	0h	MII basic configuration
AFC8h	XMII_CLK_CONFIG	RW	0h	XMII clock configuration
AFC9h	XMII_CLK_IO_CONFIG	RW	0h	XMII CLK IO configuration
AFCAh	XMII_DATA_CONFIG	RW	0h	XMII data configuration
AFCBh	XMII_DATA_IO_CONFIG	RW	0h	XMII Data IO configuration
AFCCh	RGMII_TXC_DELAY_CONFIG	RW	12h	RGMII TXC delay configuration
AFCDh	RGMII_RXC_DELAY_CONFIG	RW	12h	RGMII RXC delay configuration
AFCEh	RX_PREAMBLE_COUNT	RW	0h	RX preamble counter
AFCFh	TX_PREAMBLE_COUNT	RW	0h	TX preamble counter
AFD0h	RX_IPG_LENGTH	RW	0h	RX IPG length capture
AFD1h	TX_IPG_LENGTH	RW	0h	TX IPG length capture
B000h	SGMII_BASIC_CONTROL	RW	3000h	SGMII basic control register
B001h	SGMII_BASIC_STATUS	R	129h	SGMII basic status register
B002h	SGMII_SR_MII_DEV_ID1	RW	0h	SGMII device identifier register
B003h	SGMII_SR_MII_DEV_ID2	RW	0h	SGMII device identifier register
B004h	SGMII_AUTONEG_ADVERTISE	RW	20h	SGMII auto negotiation advertisement register.

Table 55. Register overview: MMD30*...continued*

Address	Name	Access	Reset	Description
B005h	SGMII_AUTONEG_LP_ABILITY	R	0h	SGMII auto negotiation link partner base ability register.
B006h	SGMII_AUTONEG_EXPANSION	R	0h	SGMII auto negotiation expansion register
B00Fh	SGMII_EXTENDED_STATUS	R	C000h	SGMII extended status register
B010h	SGMII_ADVANCED_CONTROL	RW	0h	Advanced control
B011h	SGMII_ADVANCED_STATUS	R	0h	Advanced status
B013h	SGMII_ADVANCED_CONFIG	RW	0h	Advanced configuration
B014h	SGMII_IRQ_SOURCE	RW	0h	SGMII interrupt source
B015h	SGMII_IRQ_ENABLE	RW	4h	SGMII interrupt enable
B016h	SGMII_IRQ_MSTATUS	R	0h	SGMII interrupt mask status. This is AND of IRQ_SOURCE and IRQ_ENABLE.
B040h	SGMII_LED_TRIGGER0	RW	0h	SGMII LED trigger 0
B041h	SGMII_LED_TRIGGER1	RW	0h	see SGMII_LED_TRIGGER0
B042h	SGMII_LED_TRIGGER2	RW	0h	see SGMII_LED_TRIGGER0
B043h	SGMII_LED_TRIGGER3	RW	0h	see SGMII_LED_TRIGGER0
B070h	SGMII_PCS_CONTROL	RW	1h	SGMII PCS control register
B071h	SGMII_PCS_STATUS	R		SGMII PCS status register
B073h	SGMII_PCS_CONFIG1	RW	10h	SGMII PCS configuration register
B074h	SGMII_PCS_CONFIG2	RW	Dh	SGMII PCS configuration register
B075h	SGMII_AUTONEG_STATUS	RW	0h	SGMII auto negotiation status register

7.4.1.1 DEVICE_IDENTIFIER3 register

Table 56. DEVICE_IDENTIFIER3 register for TJF1103A - Device identifier 3 register (address 4h)

Bit	Symbol	Access	Value	Description
15:12	SILICON_VERSION	R	9h	Silicon version
11:8	*reserved*	R	0h	Ignore on read.
7:4	SAMPLE_TYPE	R	9h	R - released silicon
3:0	NVM_VERSION	R	1h	NVM version

Table 57. DEVICE_IDENTIFIER3 register for TJF1103B - Device identifier 3 register (address 4h)

Bit	Symbol	Access	Value	Description
15:12	SILICON_VERSION	R	10h	Silicon version

Table 57. DEVICE_IDENTIFIER3 register for TJF1103B - Device identifier 3 register (address 4h)*...continued*

Bit	Symbol	Access	Value	Description
11:8	SAMPLE_TYPE	R	4h	R - released silicon
7:0	NVM_VERSION	R	1h	NVM version

7.4.1.2 MMD30_STATUS register

Table 58. MMD30_STATUS register - MMD30 status register (address 8h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:14	DEVICE_PRESENT	R		Device present
			10*	Device responding at this address
			others	No device responding at this address
13:0	*reserved*	R	0h	Ignore on read.

7.4.1.3 DEVICE_CONTROL register

Table 59. DEVICE_CONTROL register - Device control register (address 40h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	DEVICE_RESET	RW		Hard device reset. The entire device is reset all settings are lost and the device initializes and executes pin strapping. The behavior is similar to asserting the reset pin. This bit is self-clearing.
			0*	Normal operation
			1	On write a PHY reset is asserted. On read this indicates that a reset is still in progress
14	GLOBAL_CONFIG_ENABLE	RW	0h	If set, the device global configuration registers are unlocked for reconfiguration.
13	SUPER_CONFIG_ENABLE	RW	0h	If set, all configuration registers and bits can be changed for any PHY and the Global sub-system. This bit overrules all respective port CONFIG_ENABLEs and GLOBAL_CONFIG_ENABLE.
12:2	*reserved*	R	0h	Always write all 0s, ignore on read.
1	GOTO_STANDBY	RW	0h	If set, the device is directed to go to STANDBY. This bit is self clearing. On read it returns 1, if the device is still in transition. This bit is self-clearing.
0	START_OPERATION	RW	0h	If set, exit STANDBY state and start device operation. This bit is self clearing. On read it returns 1, if the device is still in transition. This bit is self-clearing.

7.4.1.4 DEVICE_STATUS register

Table 60. DEVICE_STATUS register - Device status register (address 42h)

Bit	Symbol	Access	Value	Description
15	FUSA_STATUS	R	0h	If set, the FUSA startup test has passed sucessfully
14:0	*reserved*	R	0h	Ignore on read.

7.4.1.5 DEVICE_STATUS_LATCHED register

Table 61. DEVICE_STATUS_LATCHED register - Device status latched register (address 44h)

Bit	Symbol	Access	Value	Description
15	PIN_RESET	RW	0h	If set, the device was reset via the RST_N pin. Write one to clear. This bit is latched-high.
14:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.6 DEVICE_ABILITIES register

Table 62. DEVICE_ABILITIES register - register (address 46h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:12	*reserved*	R	0h	Always write all 0s, ignore on read.
11	BIST_ABILITY	R	TJF1103A: 0h* TJF1103B: 1h*	If set, BIST function is available.
10:4	*reserved*	R	0h	Always write all 0s, ignore on read.
3	PTP_ABILITY	R	TJF1103A: 0h* TJF1103B: 1h*	If set, PTP function is available.
2:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.7 DEVICE_PROPERTIES register

Table 63. DEVICE_PROPERTIES register - Device properties register (address 47h)

Bit	Symbol	Access	Value	Description
15:5	*reserved*	R	0h	Ignore on read.
4:0	NUMBER_OF_PORTS	R	1h	Binary value represents number of ports of this device.

7.4.1.8 DEVICE_CONFIG register

Table 64. DEVICE_CONFIG register - Device config register (address 48h)

Bit	Symbol	Access	Value	Description
15	DEVICE_ENABLE	RW	1h	If deasserted, the device is disabled. Re-asserting this bit triggeres a soft reset of all subsystem control logic. The pin strap process is not restarted, previously latched settings are reapplied.
14:2	*reserved*	R	0h	Always write all 0s, ignore on read.

Table 64. DEVICE_CONFIG register - Device config register (address 48h)*...continued*

Bit	Symbol	Access	Value	Description
1	SUPER_TEST_ ENABLE	RW	0h	By default, entering test modes is restricted and guarded by respective TEST_ENABLE bits. This bit enables all test modes of the entire device and all ports. Note, the TEST_ENABLEs through the hierarchy (super, port, port sub-functions) are ORed. This setting is configuration protected.
0	TEST_ENABLE	RW	0h	By default, entering test modes is restricted and guarded by respective TEST_ENABLE bits. This bit enables test modes on device global level only, port test modes remain restricted. This setting is configuration protected.

7.4.1.9 DEVICE_CONFIG_EXTENDED register

Table 65. DEVICE_CONFIG_EXTENDED register - Device configuration extended register (address 49h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	*reserved*	R	0h	Always write 0, ignore on read.
14	OP_IRQ_ RECOVERY	RW		By default operating condition interrupts are only asserted on occurrence of a fault condition. Optionally the recovery from fault conditions can be flagged by the same interrupt bits if this bit is set to one.
			0*	Operating condition interrupts only set on rising edge of trigger signal
			1	Operating condition interrupts get asserted when their trigger signal gets either asserted or de-asserted
13:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.10 PORT_IRQ_STATUS register

Table 66. PORT_IRQ_STATUS register - PHY IRQ status register (address 70h)

Bit	Symbol	Access	Value	Description
15:2	*reserved*	R	0h	Ignore on read.
1	PORT1_IRQ	R	0h	Status bit indicating a non-masked interrupt from PortNr 1.
0	GLOBAL_IRQ	R	0h	Status bit indicating a non-masked interrupt from global functions.

7.4.1.11 PORT_IRQ_ENABLE register

Table 67. PORT_IRQ_ENABLE register - PORT IRQ enables register (address 72h)

Bit	Symbol	Access	Value	Description
15:2	*reserved*	R	0h	Always write all 0s, ignore on read.
1	PORT1_IRQ	RW	1h	Enable for interrupt from PortNr 1. This setting is preserved during deep sleep.

Table 67. PORT_IRQ_ENABLE register - PORT IRQ enables register (address 72h)*...continued*

Bit	Symbol	Access	Value	Description
0	GLOBAL_IRQ	RW	1h	Enable for interrupt from GLOBAL functions This setting is preserved during deep sleep.

7.4.1.12 PORT_IRQ_MSTATUS register

Table 68. PORT_IRQ_MSTATUS register - Port masked IRQ status register (address 74h)

Bit	Symbol	Access	Value	Description
15:2	*reserved*	R	0h	Ignore on read.
1	PORT1_IRQ	R	0h	Masked-status of PortNr 1 interrupt
0	GLOBAL_IRQ	R	0h	Masked-status of GLOBAL interrupt

7.4.1.13 GLOBAL_CAT_IRQ_STATUS register

Table 69. GLOBAL_CAT_IRQ_STATUS register - Global category IRQ status regsiter (address 80h)

Bit	Symbol	Access	Value	Description
15:9	*reserved*	R	0h	Ignore on read.
8	CONFIG_REGXS_IRQ	R	0h	If set, interrupt(s) are pending in the global 'Config & Register Access' interrupts source register
7:6	*reserved*	R	0h	Ignore on read.
5	FUNC_SHARED_IRQ	R	0h	If set, interrupt(s) are pending in the global shared functional Interrupt status
4	PHY_FUNCTION_IRQ	R	0h	If set, interrupt(s) are pending in the global 'Function' interrupt masked-status register
3	*reserved*	R	0h	Ignore on read.
2	OP_CONDITIONS_IRQ	R	0h	If set, interrupt(s) are pending in the global 'Operating condition interrupts' source register
1:0	*reserved*	R	0h	Ignore on read.

7.4.1.14 GLOBAL_CAT_IRQ_ENABLE register

Table 70. GLOBAL_CAT_IRQ_ENABLE register - Global category IRQ enable register (address 81h)

Bit	Symbol	Access	Value	Description
15:9	*reserved*	R	0h	Always write all 0s, ignore on read.
8	CONFIG_REGXS_IRQ	RW	1h	If set, the respective IRQ is enabled This setting is preserved during deep sleep.
7:6	*reserved*	R	0h	Always write 00, ignore on read.
5	FUNC_SHARED_IRQ	RW	1h	If set, the respective IRQ is enabled; this setting is preserved during deep sleep
4	PHY_FUNCTION_IRQ	RW	1h	If set, the respective IRQ is enabled This setting is preserved during deep sleep.
3	*reserved*	R	0h	Always write 0, ignore on read.

Table 70. GLOBAL_CAT_IRQ_ENABLE register - Global category IRQ enable register (address 81h)*...continued*

Bit	Symbol	Access	Value	Description
2	OP_CONDITIONS_IRQ	RW	1h	If set, the respective IRQ is enabled This setting is preserved during deep sleep.
1:0	*reserved*	R	0h	Always write 00, ignore on read.

7.4.1.15 GLOBAL_CAT_IRQ_MSTATUS register

Table 71. GLOBAL_CAT_IRQ_MSTATUS register - GLobal category IRQ masked status (address 82h)

Bit	Symbol	Access	Value	Description
15:9	*reserved*	R	0h	Always write all 0s, ignore on read.
8	CONFIG_REGXS_IRQ	R	0h	Masked-status for the respective IRQ
7:6	*reserved*	R	0h	Always write 00, ignore on read.
5	FUNC_SHARED_IRQ	R	0h	Masked-status for the respective IRQ
4	PHY_FUNCTION_IRQ	R	0h	Masked-status for the respective IRQ
3	*reserved*	R	0h	Always write 0, ignore on read.
2	OP_CONDITIONS_IRQ	R	0h	Masked-status for the respective IRQ
1:0	*reserved*	R	0h	Always write 00, ignore on read.

7.4.1.16 OP_CONDITIONS_IRQ_SOURCE register

Table 72. OP_CONDITIONS_IRQ_SOURCE register - Operating conditions IRQ sources (address 90h)

Bit	Symbol	Access	Value	Description
15	TEMP_WARN	RW	0h	If set, temperature has exceeded the limit. Write one to clear. This bit is latched-high.
14	OSC_WARN	RW	0h	If set, a OSC clock warning is pending Write one to clear. This bit is latched-high.
13:11	*reserved*	R	0h	Always write 000, ignore on read.
10	VDDA_TRX_SUPPLY_WARN	RW	0h	If set, VDDA_TRX supply voltage is not reliable Write one to clear. This bit is latched-high.
9	VREGA_SUPPLY_WARN	RW	0h	If set, VREGA supply voltage is not reliable Write one to clear. This bit is latched-high.
8	VREGD_SUPPLY_WARN	RW	0h	If set, VREGD supply voltage is not reliable Write one to clear. This bit is latched-high.
7:6	*reserved*	R	0h	Always write 00, ignore on read.

Table 72. OP_CONDITIONS_IRQ_SOURCE register - Operating conditions IRQ sources (address 90h)*...continued*

Bit	Symbol	Access	Value	Description
5	VDDIO_SUPPLY_WARN	RW	0h	If set, VDDIO supply voltage is not reliable Write one to clear. This bit is latched-high.
4	*reserved*	R	0h	Always write 0, ignore on read.
3	CORE_SUPPLY_WARN	RW	0h	If set, core supply has crossed limits Write one to clear. This bit is latched-high.
2	*reserved*	R	0h	Always write 0, ignore on read.
1	AO_SYS_SUPPLY_WARN	RW	0h	If set, always-on system supply has crossed limits. This bit is set at whenever a main always-on supply power cycle occurs. Write one to clear. This bit is latched-high.
0	*reserved*	R	0h	Always write 0, ignore on read.

7.4.1.17 OP_CONDITIONS_IRQ_ENABLE register

Table 73. OP_CONDITIONS_IRQ_ENABLE register - Operating conditions IRQ enables (address 91h)

Bit	Symbol	Access	Value	Description
15	TEMP_WARN	RW	0h	If set, enable temperature warning interrupt This setting is preserved during deep sleep.
14	OSC_WARN	RW	0h	If set, enable for OSC clock warning interrupt This setting is preserved during deep sleep.
13:11	*reserved*	R	0h	Always write 000, ignore on read.
10	VDDA_TRX_SUPPLY_WARN	RW	0h	If set, enable for VDDA_TRX supply warning interrupt This setting is preserved during deep sleep.
9	VREGA_SUPPLY_WARN	RW	0h	If set, enable for VREGA supply warning interrupt This setting is preserved during deep sleep.
8	VREGD_SUPPLY_WARN	RW	0h	If set, enable for VREGD supply warning interrupt This setting is preserved during deep sleep.
7:6	*reserved*	R	0h	Always write 00, ignore on read.
5	VDDIO_SUPPLY_WARN	RW	0h	If set, enable for VDDIO supply interrupt This setting is preserved during deep sleep.
4	*reserved*	R	0h	Always write 0, ignore on read.
3	CORE_SUPPLY_WARN	RW	0h	If set, enable Core supply interrupt This setting is preserved during deep sleep.
2	*reserved*	R	0h	Always write 0, ignore on read.
1	AO_SYSTEM_SUPPLY_WARN	RW	0h	If set, enable Always-on system supply interrupt This setting is preserved during deep sleep.
0	*reserved*	RW	0h	Always write 0, ignore on read.

7.4.1.18 OP_CONDITIONS_IRQ_MSTATUS register

Table 74. OP_CONDITIONS_IRQ_MSTATUS register - Operating conditions IRQ masked status (address 92h)

Bit	Symbol	Access	Value	Description
15	TEMP_WARN	R	0h	Masked-status of High-Temp Warning IRQ
14	OSC_WARN	R	0h	Masked-status of OSC clock Monitor warning IRQ
13:11	*reserved*	R	0h	Ignore on read.
10	VDDA_TRX_ SUPPLY_WARN	R	0h	Masked-status of VDDA_TRX supply warning IRQ
9	VREGA_SUPPLY_ WARN	R	0h	Masked-status of VREGA supply warning IRQ
8	VREGD_SUPPLY_ WARN	R	0h	Masked-status of VREGD supply warning IRQ
7:6	*reserved*	R	0h	Always write 0, ignore on read.
5	VDDIO_SUPPLY_ WARN	R	0h	Masked-status of VDDIO supply warning IRQ
4	*reserved*	R	0h	Always write 0, ignore on read.
3	CORE_SUPPLY_ WARN	R	0h	Masked-status of digital core supply warning interrupt
2	*reserved*	R	0h	Ignore on read.
1	AO_SYSTEM_ SUPPLY_WARN	R	0h	Masked-status of Always-on system supply warning interrupt
0	*reserved*	R	0h	Ignore on read.

7.4.1.19 TOP_EPHY_IRQ_SOURCE register

Table 75. TOP_EPHY_IRQ_SOURCE register - Top Ethernet PHY IRQ sources (address A0h)

Bit	Symbol	Access	Value	Description
15:2	*reserved*	R	0h	Always write all 0s, ignore on read.
1	WAKE_SLEEP_ EVENT	RW	0h	If set, an event is detected by WISE_STATUS register. This interrupt does not get asserted by clearing latched-status bits. Write one to clear. This bit is latched-high.
0	*reserved*	R	0h	Always write 0, ignore on read.

7.4.1.20 TOP_EPHY_IRQ_ENABLE register

Table 76. TOP_EPHY_IRQ_ENABLE register - Top Ethernet PHY IRQ enables (address A1h)

Bit	Symbol	Access	Value	Description
15:2	*reserved*	R	0h	Always write ass 0s, ignore on read.
1	WAKE_SLEEP_ EVENT	RW	0h	If set, the wake sleep event IRQ is enabled This setting is preserved during deep sleep.
0	*reserved*	R	0h	Always write 0, ignore on read.

7.4.1.21 TOP_EPHY_IRQ_MSTATUS register

Table 77. TOP_EPHY_IRQ_MSTATUS register - Top Ethernet PHY IRQ masked status (address A2h)

Bit	Symbol	Access	Value	Description
15:2	*reserved*	R	0h	Ignore on read.
1	WAKE_SLEEP_EVENT_IRQ	R	0h	Masked-status of wake sleep event IRQ
0	*reserved*	R	0h	Ignore on read.

7.4.1.22 FUNC_SHARED_IRQ_SOURCE register

Table 78. FUNC_SHARED_IRQ_SOURCE register - Global shared function IRQ sources (address B0h)

Bit	Symbol	Access	Value	Description
15:3	*reserved*	R	0h	Always write all 0s, ignore on read.
2	VREGA_LDO_SHUTOFF_IRQ	RW	0h	If set, VREGA LDO shutoff condition detected due to short circuit on LDO output Write one to clear.
1	VREGD_LDO_SHUTOFF_IRQ	RW	0h	If set, VREGD LDO shutoff condition detected due to short circuit on LDO output Write one to clear.
0	*reserved*	R	0h	Always write 0, ignore on read.

7.4.1.23 FUNC_SHARED_IRQ_ENABLE register

Table 79. FUNC_SHARED_IRQ_ENABLE register - Global shared function IRQ enables (address B1h)

Bit	Symbol	Access	Value	Description
15:3	*reserved*	R	0h	Always write all 0s, ignore on read.
2	VREGA_LDO_SHUTOFF_IRQ	RW	0h	If set, the VREGA_LDO_SHUTOFF_IRQ is enabled; this setting is preserved during deep sleep
1	VREGD_LDO_SHUTOFF_IRQ	RW	0h	If set, the VREGD_LDO_SHUTOFF_IRQ is enabled; this setting is preserved during deep sleep
0	*reserved*	R	0h	Always write 0, ignore on read.

7.4.1.24 FUNC_SHARED_IRQ_MSTATUS register

Table 80. FUNC_SHARED_IRQ_MSTATUS register - Global shared function IRQ masked status (address B2h)

Bit	Symbol	Access	Value	Description
15:3	*reserved*	R	0h	Ignore on read.
2	VREGA_LDO_SHUTOFF_IRQ	RW	0h	Masked status of VREGA_LDO_SHUTOFF_IRQ
1	VREGD_LDO_SHUTOFF_IRQ	RW	0h	Masked status of VREGD_LDO_SHUTOFF_IRQ
0	*reserved*	R	0h	Ignore on read.

7.4.1.25 CONFIG_REGXS_IRQ_SOURCE register

Table 81. CONFIG_REGXS_IRQ_SOURCE register - Configuration register access IRQ sources (address C0h)

Bit	Symbol	Access	Value	Description
15	COLD_RESET	RW	0h	If set, all configuration settings reset to defaults due to RST_N Pin. Write one to clear. This bit is latched-high.
14:2	*reserved*	R	0h	Always write all 0s, ignore on read.
1	SMI_ERROR	RW	0h	If set, invalid SMI transaction. This bit flags syntax errors in SMI commands and invalid SMI transactions to global register addresses, like writing to read-only registers and reading or writing non-existent registers.[1] Write one to clear. This bit is latched-high.
0	*reserved*	R	0h	If set, Additional bits in part b Always write 0, ignore on read.

[1] SMI_ERROR gets set when the ALWAYS_ACCESSIBLE register is read or with a subsequent SMI access after a wrong clause 22 op code. Ignore SMI_ERROR in these cases.

7.4.1.26 CONFIG_REGXS_IRQ_ENABLE register

Table 82. CONFIG_REGXS_IRQ_ENABLE register - Configuration register access IRQ enable (address C1h)

Bit	Symbol	Access	Value	Description
15	COLD_RESET	RW	0h	Enables the COLD_RESET interrupt This setting is preserved during deep sleep.
14:2	*reserved*	R	0h	Always write all 0s, ignore on read.
1	SMI_ERROR	RW	0h	Enables the SMI_ERROR interrupt This setting is preserved during deep sleep.
0	*reserved*	R	0h	Always write 0, ignore on read.

7.4.1.27 CONFIG_REGXS_IRQ_MSTATUS register

Table 83. CONFIG_REGXS_IRQ_MSTATUS register - Configuration register access IRQ masked status (address C2h)

Bit	Symbol	Access	Value	Description
15	COLD_RESET	R	0h	Masked-status of COLD_RESET interrupt
14:2	*reserved*	R	0h	Ignore on read.
1	SMI_ERROR	R	0h	Masked-status of SMI_ERROR interrupt
0	*reserved*	R	0h	Ignore on read.

7.4.1.28 BROADCAST register

Table 84. BROADCAST register - Broadcast control (address 100h)

Bit	Symbol	Access	Value	Description
15:5	*reserved*	R	0h	Always write all 0s, ignore on read.
4:0	ADDRESS	RW	0h	5-bit SMI PHY address used for broadcasting. See SMI_CONFIG register. This setting is preserved during deep sleep.

7.4.1.29 PORT1_CONFIG register

Table 85. PORT1_CONFIG register - Port 1 configuration (address 101h)

Bit	Symbol	Access	Value	Description
15	PRESENT	R	1h	If set, port is present
14	ENABLE	RW	1h	If set, port is enabled This setting is preserved during deep sleep.
13:5	*reserved*	R	0h	Always write all 0s, ignore on read.
4:0	ADDRESS	R	1h	5-bit SMI PHY address assigned to this port This setting is preserved during deep sleep.

7.4.1.30 WISE_CONTROL register

Table 86. WISE_CONTROL register - Wake, inhibit and sleep control (address 180h)

Bit	Symbol	Access	Value	Description
15:1	*reserved*	R	0h	Always write all 0s, ignore on read.
0	INH_OVERRIDE	RW	1h	If asserted, drive inhibit signal high at any time as long as the device is powered. When set to zero, the inhibit pin is HIGH-Z when this does does not requests power.

7.4.1.31 WISE_STATUS register

Table 87. WISE_STATUS register - Wake, inhibit and sleep status (address 181h)

Bit	Symbol	Access	Value	Description
15	*reserved*	R	0h	Always write 0, ignore on read.
14	WU_IO_RECEIVED	RW	0h	If set, wake-up request received on wakeup IO pin Write one to clear. This bit is latched-high.
13	WU_SMI_RECEIVED	RW	0h	If set, a wake-up is received via the WU_SMI bit Write one to clear. This bit is latched-high.
12:1	*reserved*	R	0h	Always write all 0s, ignore on read.
0	DEV_SLEEP_STATUS	R	0h	If set, device in SLEEP

7.4.1.32 WISE_CONFIG register

Table 88. WISE_CONFIG register - Wake, inhibit and sleep configuration (address 182h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	WAKE_SLEEP_ENABLE	RW	0h	If set, Wake-Sleep functionality enabled This setting is preserved during deep sleep. This setting is configuration protected.
14	*reserved*	R	0h	Always write 0, ignore on read.
13:12	WU_IO	RW		Wakeup IO configuration This setting is preserved during deep sleep. This setting is configuration protected.
			00	Wake-Up IO is disabled
			01	Wake-Up IO is input only, output disabled
			10	Wake-Up IO is output only, input disabled
			11*	Wake-Up IO is input and output
11	*reserved*	R	0h	Always write 0, ignore on read.
10	FWD_WU_SMI_TO_IO	RW	0h	If set, forward SMI wakeup request (WU_SMI) to wakeup IO pin This setting is preserved during deep sleep. This setting is configuration protected.
9:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.33 WISE_PARAMETERS register

Table 89. WISE_PARAMETERS register - Wake, inhibit and sleep parameters (address 184h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:5	*reserved*	R	0h	Always write all 0s, ignore on read.
4	WU_IO_DETECT_LIMIT	RW		Wakeup IO detection pulse length This setting is preserved during deep sleep. This setting is configuration protected.
			0*	The detection window for wake-up pulses is 10-40 us. Wake-up pulses shorter than 10 us are ignored and pulses longer than 40us are detected.
			1	If this bit is set to one, the detection window for wake-up pulses is 10-20ms. This higher detection window is meant to support non-TC10 wake-up mechanisms, like a dedicated wake-up wire.
3:0	WU_IO_PULSE_LENGTH	RW	1h	Length of a generated wake-up pulse on the wake-up IO pin in steps of 50us*2^n. If set to 0h, the pulse length is 50 us. If set to Fh, the pulse length is 1.6 s. This setting is preserved during deep sleep. This setting is configuration protected.

7.4.1.34 SMI_STATUS register

Table 90. SMI_STATUS register - SMI status (address 189h)

Bit	Symbol	Access	Value	Description
15	CL45_DETECT	RW	0h	If set, Clause 45 transaction detected. Latched high Write one to clear. This bit is latched-high.
14	CL22_INDIRECT_DETECT	RW	0h	If set, Clause 22 registers 0Dh or 0Eh accessed. Latched high Write one to clear. This bit is latched-high.
13	CL22_DIRECT_DETECT	RW	0h	If set, Regular Clause 22 transaction detected (excluding access to registers 0Dh and 0Eh). Latched high Write one to clear. This bit is latched-high.
12	SMI_TIMEOUT	RW	0h	If set, an SMI transaction did not complete due to timeout. Latched high Write one to clear. This bit is latched-high.
11:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.35 SMI_CONFIG register

Table 91. SMI_CONFIG register - SMI config (address 18Ah)

Bit	Symbol	Access	Value	Description
15	ACCESS_ENABLE	R	1h	Enable register access via SMI. Note that this is read-only, if accessed from SMI side. This register is read-write if accessed internally via APB (only available in switch devices). Note: Broadcasting can be enabled even if this field is set to zero. If set, Enable register access via SMI for all Phys.
14	SIDE_EFFECTS_DISABLE	RW	0h	Side-effects are effects on a register value due to a read action. This include Clear-on-Read for Latch-High, Latch-Low bit and Multi-Word reads. If set, Disable side-effects (for debugging purposes) This setting is configuration protected.
13	IDLE_PRECHARGE	RW	0h	If set, Drive MDIO high before return to idle (high-Z) This setting is preserved during deep sleep. This setting is configuration protected.
12	SYNC_ON_16_ONES	RW	0h	If set, the device does not expect a preamble for SMI synchronization This setting is preserved during deep sleep. This setting is configuration protected.
11:2	*reserved*	R	0h	Always write all 0s, ignore on read.
1	BROADCAST_READ_FUNC	RW		This bit configures the behavior of a read/write SMI transaction to the BROADCAST address. This setting is preserved during deep sleep. This setting is configuration protected.

Table 91. SMI_CONFIG register - SMI config (address 18Ah) *...continued*

Bit	Symbol	Access	Value	Description
			0*	Broadcast write to all present PHYs Broadcast read of full address space Response on reads to PHY address space is a bit-wise OR-function of that register for all present PHYs.
			1	Broadcast write to all present PHYs Broadcast read of shared address space only all-zero response for read of remaining address space
0	BROADCAST_ENABLE	RW	0h	When BROADCAST_ENABLE is set, SMI broadcast is enabled. If enabled, SMI access over the broadcasting mechanism is independent of the value of ACCESS_ENABLE. The broadcast address is configured with BROADCAST[ADDRESS]. This setting is preserved during deep sleep. This setting is configuration protected.

7.4.1.36 SMI_DATA_IO_CONFIG register

Table 92. SMI_DATA_IO_CONFIG register - SMI Data IO configuration (address 18Ch)

Bit	Symbol	Access	Value	Description
15	MANUAL_CONFIG	RW	0h	If set, manual config of MDIO cells; otherwise settings are automatically determined. Caution: a manual override may violate the SMI timing in some or all operating conditions. The timing values in the dynamic characteristics section of the datasheet are valid under default settings only.
14:11	*reserved*	RW	0h	Always write 0000, ignore on read.
10:8	DRIVE_STRENGTH	RW	0h	Select drive strength of MDIO output IO cells 0 = weakest 7 = strongest
7:3	*reserved*	RW	0h	Always write 00000, ignore on read.
2:0	SLEW_RATE	RW	0h	Select slew rate of DATA MDIO output pins. 0 = weakest 7 = strongest

7.4.1.37 GLOBAL_LED_TRIGGER0 register

Table 93. GLOBAL_LED_TRIGGER0 register - LED trigger 0 (address 190h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	0h	Enable the LED trigger output
14:4	*reserved*	RW	0h	Always write all 0s, ignore on read.
3:0	FUNCTION	RW		Selects the function muxed on the device global LED trigger 0
			0*	Safety status

Table 93. GLOBAL_LED_TRIGGER0 register - LED trigger 0 (address 190h)*...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
			1	Supplies valid
			3h	XTAL oscillator running / clock available
			others	Reserved

7.4.1.38 GLOBAL_LED_TRIGGER1 register

Table 94. GLOBAL_LED_TRIGGER1 register - LED trigger 1 (address 191h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	0h	Enable the LED trigger output
14:4	*reserved*	RW	0h	Always write all 0s, ignore on read.
3:0	FUNCTION	RW		Selects the function muxed on the device global LED trigger 1
			0*	Safety status
			1	Supplies valid
			3h	XTAL oscillator running / clock available
			others	Reserved

7.4.1.39 GLOBAL_LED_TRIGGER2 register

Table 95. GLOBAL_LED_TRIGGER2 register - LED trigger 2 (address 192h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	0h	Enable the LED trigger output
14:4	*reserved*	RW	0h	Always write all 0s, ignore on read.
3:0	FUNCTION	RW		Selects the function muxed on the device global LED trigger 2
			0*	Safety status
			1	Supplies valid
			3h	XTAL oscillator running / clock available
			others	Reserved

7.4.1.40 GLOBAL_LED_TRIGGER3 register

Table 96. GLOBAL_LED_TRIGGER3 register - LED trigger 3 (address 193h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	0h	Enable the LED trigger output
14:4	*reserved*	RW	0h	Always write all 0s, ignore on read.

Table 96. GLOBAL_LED_TRIGGER3 register - LED trigger 3 (address 193h)*...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
3:0	FUNCTION	RW		Selects the function muxed on the device global LED trigger 3
			0*	Safety status
			1	Supplies valid
			3h	XTAL oscillator running / clock available
			others	Reserved

7.4.1.41 LED0_CONFIG register

Table 97. LED0_CONFIG register - LED controller 0 Configuration (address 1A0h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	1h	If set, LED controller is enabled.
14	INVERT	RW	1h	If set, LED0A becomes high to drive the LED.[1]
13	SPLIT_UP	RW		Split up
			0*	Control one LED (blink/PWM/multi-color); One output A or two correlated outputs A/B.
			1	Control two LEDs (blink only) with two synchronous, but uncorrelated outputs A/B.
12:4	*reserved*	RW	0h	Always write all 0s, ignore on read.
3:0	BLINKING_PERIOD	RW		Sets the blinking period.
			0000	Reserved
			0001	250 us
			0010	500 us
			0011	1 ms
			0100	2 ms
			0101	4 ms
			0110	8 ms
			0111	16 ms
			1000	32 ms
			1001	64 ms
			1010	128 ms
			1011	256 ms (~0.25 sec)
			1100*	512 ms (~0.5 sec)
			1101	1024 ms (~1 sec)
			1110	2048 ms (~2 sec)
			1111	latched (reset by disable)

[1] For the TJF1103A: consult the application notes for limitations on resetting INVERT.

7.4.1.42 LED0_TRIG_SOURCE register

Table 98. LED0_TRIG_SOURCE register - LED controller 0 trigger source selection (address 1A1h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:13	FUNC_SELECT_B	RW		If FUNC_SELECT_B ≠ 0, the selected PORT subfunction is used from the PortNr as configured by the PORTNR_(OR_TOPFUNC)_B field. If FUNC_SELECT_B = 000 = GLOBAL, the (PORTNR_OR)_TOPFUNC_B field is used to select the desired GLOBAL subfunction.
			0*	Global LED trigger
			1	Port EPHY LED trigger
			2h	Port PTP LED trigger
			7h	Port xMII/SGMII LED trigger
			others	reserved
12:8	PORTNR_OR_TOPFUNC_B	RW	1h	If FUNC_SELECT_A ≠ 0: Select PORT number 1-32 (00000=32) If FUNC_SELECT_ A= 0: Select GLOBAL subfunction, as follows
			00000	global shared resources
			others	reserved
7:5	FUNC_SELECT_A	RW		If FUNC_SELECT_A≠0, the selected PORT subfunction is used from the PortNr as configured by the PORTNR_(OR_TOPFUNC)_A field. If FUNC_SELECT_A=000=GLOBAL, the (PORTNR_OR)_TOPFUNC_A field is used to select the desired GLOBAL subfunction.
			0	Global LED trigger
			1*	Port EPHY LED trigger
			2h	Port PTP LED trigger
			7h	Port xMII/SGMII LED trigger
			others	reserved
4:0	PORTNR_OR_TOPFUNC_A	RW	1h	If FUNC_SELECT_A≠0: Select PORT number 1-32 (00000=32) If FUNC_SELECT_A=0: Select GLOBAL subfunction, as follows
			00000	global shared resources
			others	reserved

7.4.1.43 LED0_TRIG01_CONFIG register

Table 99. LED0_TRIG01_CONFIG register - LED controller 0 Trigger 0 and 1 configuration (address 1A2h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	TRIG1_ENABLE	RW	TJF1103A: 0h TJF1103B: 1h	If set, this trigger is enabled
14	TRIG1_POLARITY	RW	1h	If this bit is deasserted, the polarity of the input signal is inverted after the event detector.
13	TRIG1_HILO_PRIORITY	RW	1h	If this bit is set, the event detector is sensitive to high-level events and short high-level pulses are stretched. Otherwise, the detector is sensitive to low-level events and low-level pulses are stretched.
12	TRIG1_SELECT	RW		Selects if FUNC_SELECT_A or B is selected
			0*	A input is used for the trigger
			1	B input is used for the trigger
11:8	*reserved*	RW	0h	Always write all 0s, ignore on read.
7	TRIG0_ENABLE	RW	1h	If set, this trigger is enabled
6	TRIG0_POLARITY	RW	1h	If this bit is deasserted, the polarity of the input signal is inverted after the event detector.
5	TRIG0_HILO_PRIORITY	RW	1h	If this bit is set, the event detector is sensitive on high-level events and short high-level pulses are stretched. Otherwise, the detector is sensitive on low-level events and low-level pulses are stretched.
4	TRIG0_SELECT	RW		Selects if FUNC_SELECT_A or B is selected
			0*	A input is used for the trigger
			1	B input is used for the trigger
3	TRIG0_RAW	RW	0h	If set the raw trigger signal is used and pulse stretching is disabled.
2:0	*reserved*	RW	0h	Always write 000, ignore on read.

7.4.1.44 LED0_TRIG23_CONFIG register

Table 100. LED0_TRIG23_CONFIG register - LED controller 0 Trigger 2 and 3 configuration (address 1A3h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	TRIG3_ENABLE	RW	TJF1103A: 1h TJF1103B: 0h	If set, this trigger is enabled
14	TRIG3_POLARITY	RW	TJF1103A: 1h TJF1103B: 0h	If this bit is deasserted, the polarity of the input signal is inverted after the event detector.
13	TRIG3_HILO_PRIORITY	RW	TJF1103A: 1h TJF1103B: 0h	If this bit is set, the event detector is sensitive to high-level events and short high-level pulses are stretched. Otherwise, the detector is sensitive on low-level events and low-level pulses are stretched.
12	TRIG3_SELECT	RW		Selects if FUNC_SELECT_A or B is selected

Table 100. LED0_TRIG23_CONFIG register - LED controller 0 Trigger 2 and 3 configuration (address 1A3h) *...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
			0*	A input is used for the trigger
			1	B input is used for the trigger
11:10	TRIG3_FUNCTION	RW	0h	This field has no effect when SPLIT_UP is set and TRIG2/3 determine output-B with similar behavior as TRIG0/1 for output-A. If SPLIT_UP=0: 00 = TRIG3 is AND'ed with TRIG0 event. if TRIG2_MODULATION=1: 01 = Blink color modulation by TRIG2/3 1x = Reserved If TRIG2_MODULATION=0: 01 = ColorB replaces OFF for TRIG3 event 10 = Direct color modulation by TRIG3 11 = Reserved
9:8	*reserved*	RW	0h	Always write all 0s, ignore on read.
7	TRIG2_ENABLE	RW	TJF1103A: 0h TJF1103B: 1h	If set, this trigger is enabled
6	TRIG2_POLARITY	RW	1h	If this bit is deasserted, the polarity of the input signal is inverted after the event detector.
5	TRIG2_HILO_PRIORITY	RW	1h	If this bit is set, the event detector is sensitive on high-level events and short high-level pulses are stretched. Otherwise, the detector is sensitive on low-level events and low-level pulses are stretched.
4	TRIG2_SELECT	RW		Selects if FUNC_SELECT_A or B is selected
			0*	A input is used for the trigger
			1	B input is used for the trigger
3	TRIG2_RAW	RW	0h	If set the raw trigger signal is used and pulse stretching is disabled.
2	TRIG2_MODULATION	RW		If set, enables multi-color blink on ColorA and ColorB. This bit has no effect when SPLIT_UP=1 or TRIG2_RAW=1. If SPLIT_UP=1, TRIG2/3 determine output-B with similar behavior as TRIG0/1 for output-A.
			0*	Blink time modulation
			1	Blink color modulation
1:0	*reserved*	RW	0h	Always write 00, ignore on read.

7.4.1.45 LED1_CONFIG register

Table 101. LED1_CONFIG register - LED Controller 1 Configuration (address 1A4h)[1]

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	1h	see LED0_CONFIG[ENABLE]
14	INVERT	RW	1h	see LED0_CONFIG[INVERT]

Table 101. LED1_CONFIG register - LED Controller 1 Configuration (address 1A4h)[1]*...continued*

Bit	Symbol	Access	Value	Description
13	SPLIT_UP	RW	0h	see LED0_CONFIG[SPLIT_UP]
12:4	*reserved*	RW	0h	Always write all 0s, ignore on read.
3:0	BLINKING_PERIOD	RW	Ch	see LED0_CONFIG[BLINKING_PERIOD]

[1] See LED controller 0

7.4.1.46 LED1_TRIG_SOURCE register

Table 102. LED1_TRIG_SOURCE register - LED controller 1 trigger source selection (address 1A5h)[1]

Bit	Symbol	Access	Value	Description
15:13	FUNC_SELECT_B	RW	0h	see LED0_TRIG_SOURCE[FUNC_SELECT_B]
12:8	PORTNR_OR_TOPFUNC_B	RW	0h	see LED0_TRIG_SOURCE[PORTNR_OR_TOPFUNC_B]
7:5	FUNC_SELECT_A	RW	1h	see LED0_TRIG_SOURCE[FUNC_SELECT_A]
4:0	PORTNR_OR_TOPFUNC_A	RW	1h	see LED0_TRIG_SOURCE[PORTNR_OR_TOPFUNC_A]

[1] See LED controller 0

7.4.1.47 LED1_TRIG01_CONFIG register

Table 103. LED1_TRIG01_CONFIG register - LED controller 1 Trigger 0 and 1 configuration (address 1A6h)[1]

Bit	Symbol	Access	Value	Description
15	TRIG1_ENABLE	RW	1h	see LED0_TRIG01_CONFIG[TRIG1_ENABLE]
14	TRIG1_POLARITY	RW	1h	see LED0_TRIG01_CONFIG[TRIG1_POLARITY]
13	TRIG1_HILO_PRIORITY	RW	1h	see LED0_TRIG01_CONFIG[TRIG1_PRIORITY]
12	TRIG1_SELECT	RW	0h	see LED0_TRIG01_CONFIG[TRIG1_SELECT]
11:8	*reserved*	RW	0h	Always write all 0s, ignore on read.
7	TRIG0_ENABLE	RW	1h	see LED0_TRIG01_CONFIG[TRIG0_ENABLE]
6	TRIG0_POLARITY	RW	1h	see LED0_TRIG01_CONFIG[TRIG0_POLARITY]
5	TRIG0_HILO_PRIORITY	RW	1h	see LED0_TRIG01_CONFIG[TRIG0_HILO_PRIORITY]
4	TRIG0_SELECT	RW	0h	see LED0_TRIG01_CONFIG[TRIG0_SELECT]
3	TRIG0_RAW	RW	0h	see LED0_TRIG01_CONFIG[TRIG0_RAW]
2:0	*reserved*	RW	0h	Always write all 0s, ignore on read.

[1] See LED controller 0

7.4.1.48 LED1_TRIG23_CONFIG register

Table 104. LED1_TRIG23_CONFIG register - LED controller 1 Trigger 2 and 3 configuration (address 1A7h)[1]

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	TRIG3_ENABLE	RW	TJF1103A: 1h TJF1103B: 0h	see LED0_TRIG23_CONFIG[TRIG3_ENABLE]
14	TRIG3_POLARITY	RW	TJF1103A: 1h TJF1103B: 0h	see LED0_TRIG23_CONFIG[TRIG3_POLARITY]
13	TRIG3_HILO_PRIORITY	RW	TJF1103A: 1h TJF1103B: 0h	see LED0_TRIG23_CONFIG[TRIG3_HILO_PRIORITY]
12	TRIG3_SELECT	RW	0h	see LED0_TRIG23_CONFIG[TRIG3_SELECT]
11:10	TRIG3_FUNCTION	RW	0h	see LED0_TRIG23_CONFIG[TRIG3_FUNCTION]
9:8	*reserved*	RW	0h	Always write 00, ignore on read.
7	TRIG2_ENABLE	RW	1h	see LED0_TRIG23_CONFIGTRIG2_ENABLE]
6	TRIG2_POLARITY	RW	1h	see LED0_TRIG23_CONFIG[TRIG2_POLARITY]
5	TRIG2_HILO_PRIORITY	RW	1h	see LED0_TRIG23_CONFIG[TRIG2_HILO_PRIORITY]
4	TRIG2_SELECT	RW	0h	see LED0_TRIG23_CONFIG[TRIG2_SELECT]
3	TRIG2_RAW	RW	0h	see LED0_TRIG23_CONFIG[TRIG2_RAW]
2	TRIG2_MODULATION	RW	0h	see LED0_TRIG23_CONFIG[TRIG2_MODULATION]
1:0	*reserved*	RW	0h	Always write 00, ignore on read.

[1] See LED controller 0

7.4.1.49 LED2_CONFIG register

Table 105. LED2_CONFIG register - LED Controller 2 Configuration (address 1A8h)[1]

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	1h	see LED0_CONFIG[ENABLE]
14	INVERT	RW	1h	see LED0_CONFIG[INVERT]
13	SPLIT_UP	RW	0h	see LED0_CONFIG[SPLIT_UP]
12:4	*reserved*	RW	0h	Always write all 0s, ignore on read.
3:0	BLINKING_PERIOD	RW	Ch	see LED0_CONFIG[BLINKING_PERIOD]

[1] See LED controller 0

7.4.1.50 LED2_TRIG_SOURCE register

Table 106. LED2_TRIG_SOURCE register - LED controller 2 trigger source selection (address 1A9h)[1]

Bit	Symbol	Access	Value	Description
15:13	FUNC_SELECT_B	RW	0h	see LED0_TRIG_SOURCE[FUNC_SELECT_B]

Table 106. LED2_TRIG_SOURCE register - LED controller 2 trigger source selection (address 1A9h)[1] *...continued*

Bit	Symbol	Access	Value	Description
12:8	PORTNR_OR_TOPFUNC_B	RW	0h	see LED0_TRIG_SOURCE[PORTNR_OR_TOPFUNC_B]
7:5	FUNC_SELECT_A	RW	1h	see LED0_TRIG_SOURCE[FUNC_SELECT_A]
4:0	PORTNR_OR_TOPFUNC_A	RW	1h	see LED0_TRIG_SOURCE[PORTNR_OR_TOPFUNC_A]

[1] See LED controller 0

7.4.1.51 LED2_TRIG01_CONFIG register

Table 107. LED2_TRIG01_CONFIG register - LED controller 2 Trigger 0 and 1 configuration (address 1AAh)[1]

Bit	Symbol	Access	Value	Description
15	TRIG1_ENABLE	RW	1h	see LED0_TRIG01_CONFIG[TRIG1_ENABLE]
14	TRIG1_POLARITY	RW	1h	see LED0_TRIG01_CONFIG[TRIG1_POLARITY]
13	TRIG1_HILO_PRIORITY	RW	1h	see LED0_TRIG01_CONFIG[TRIG1_PRIORITY]
12	TRIG1_SELECT	RW	0h	see LED0_TRIG01_CONFIG[TRIG1_SELECT]
11:8	*reserved*	RW	0h	Always write all 0s, ignore on read.
7	TRIG0_ENABLE	RW	1h	see LED0_TRIG01_CONFIG[TRIG0_ENABLE]
6	TRIG0_POLARITY	RW	1h	see LED0_TRIG01_CONFIG[TRIG0_POLARITY]
5	TRIG0_HILO_PRIORITY	RW	1h	see LED0_TRIG01_CONFIG[TRIG0_HILO_PRIORITY]
4	TRIG0_SELECT	RW	0h	see LED0_TRIG01_CONFIG[TRIG0_SELECT]
3	TRIG0_RAW	RW	0h	see LED0_TRIG01_CONFIG[TRIG0_RAW]
2:0	*reserved*	RW	0h	Always write 000, ignore on read.

[1] See LED controller 0

7.4.1.52 LED2_TRIG23_CONFIG register

Table 108. LED2_TRIG23_CONFIG register - LED controller 2 Trigger 2 and 3 configuration (address 1ABh)[1]

Bit	Symbol	Access	Value	Description
15	TRIG3_ENABLE	RW	TJF1103A: 1h TJF1103B: 0h	see LED0_TRIG23_CONFIG[TRIG3_ENABLE]
14	TRIG3_POLARITY	RW	TJF1103A: 1h TJF1103B: 0h	see LED0_TRIG23_CONFIG[TRIG3_POLARITY]
13	TRIG3_HILO_PRIORITY	RW	TJF1103A: 1h TJF1103B: 0h	see LED0_TRIG23_CONFIG[TRIG3_HILO_PRIORITY]
12	TRIG3_SELECT	RW	0h	see LED0_TRIG23_CONFIG[TRIG3_SELECT]
11:10	TRIG3_FUNCTION	RW	0h	see LED0_TRIG23_CONFIG[TRIG3_FUNCTION]
9:8	*reserved*	RW	0h	Always write 00, ignore on read.

Table 108. LED2_TRIG23_CONFIG register - LED controller 2 Trigger 2 and 3 configuration (address 1ABh)[1] *...continued*

Bit	Symbol	Access	Value	Description
7	TRIG2_ENABLE	RW	1h	see LED0_TRIG23_CONFIGTRIG2_ENABLE]
6	TRIG2_POLARITY	RW	1h	see LED0_TRIG23_CONFIG[TRIG2_POLARITY]
5	TRIG2_HILO_ PRIORITY	RW	1h	see LED0_TRIG23_CONFIG[TRIG2_HILO_PRIORITY]
4	TRIG2_SELECT	RW	0h	see LED0_TRIG23_CONFIG[TRIG2_SELECT]
3	TRIG2_RAW	RW	0h	see LED0_TRIG23_CONFIG[TRIG2_RAW]
2	TRIG2_ MODULATION	RW	0h	see LED0_TRIG23_CONFIG[TRIG2_MODULATION]
1:0	*reserved*	RW	0h	Always write 00, ignore on read.

[1] See LED controller 0

7.4.1.53 LED3_CONFIG register

Table 109. LED3_CONFIG register - LED Controller 3 Configuration (address 1ACh)[1]

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	1h	see LED0_CONFIG[ENABLE]
14	INVERT	RW	1h	see LED0_CONFIG[INVERT]
13	SPLIT_UP	RW	0h	see LED0_CONFIG[SPLIT_UP]
12:4	*reserved*	RW	0h	Always write all 0s, ignore on read.
3:0	BLINKING_PERIOD	RW	Ch	see LED0_CONFIG[BLINKING_PERIOD]

[1] See LED controller 0

7.4.1.54 LED3_TRIG_SOURCE register

Table 110. LED3_TRIG_SOURCE register - LED controller 3 trigger source selection (address 1ADh)[1]

Bit	Symbol	Access	Value	Description
15:13	FUNC_SELECT_B	RW	0h	see LED0_TRIG_SOURCE[FUNC_SELECT_B]
12:8	PORTNR_OR_ TOPFUNC_B	RW	0h	see LED0_TRIG_SOURCE[PORTNR_OR_TOPFUNC_B]
7:5	FUNC_SELECT_A	RW	1h	see LED0_TRIG_SOURCE[FUNC_SELECT_A]
4:0	PORTNR_OR_ TOPFUNC_A	RW	1h	see LED0_TRIG_SOURCE[PORTNR_OR_TOPFUNC_A]

[1] See LED controller 0

7.4.1.55 LED3_TRIG01_CONFIG register

Table 111. LED3_TRIG01_CONFIG register - LED controller 3 Trigger 0 and 1 configuration (address 1AEh)[1]

Bit	Symbol	Access	Value	Description
15	TRIG1_ENABLE	RW	1h	see LED0_TRIG01_CONFIG[TRIG1_ENABLE]

Table 111. LED3_TRIG01_CONFIG register - LED controller 3 Trigger 0 and 1 configuration (address 1AEh)[1]*...continued*

Bit	Symbol	Access	Value	Description
14	TRIG1_POLARITY	RW	1h	see LED0_TRIG01_CONFIG[TRIG1_POLARITY]
13	TRIG1_HILO_ PRIORITY	RW	1h	see LED0_TRIG01_CONFIG[TRIG1_PRIORITY]
12	TRIG1_SELECT	RW	0h	see LED0_TRIG01_CONFIG[TRIG1_SELECT]
11:8	*reserved*	RW	0h	Always write 0000, ignore on read.
7	TRIG0_ENABLE	RW	1h	see LED0_TRIG01_CONFIG[TRIG0_ENABLE]
6	TRIG0_POLARITY	RW	1h	see LED0_TRIG01_CONFIG[TRIG0_POLARITY]
5	TRIG0_HILO_ PRIORITY	RW	1h	see LED0_TRIG01_CONFIG[TRIG0_HILO_PRIORITY]
4	TRIG0_SELECT	RW	0h	see LED0_TRIG01_CONFIG[TRIG0_SELECT]
3	TRIG0_RAW	RW	0h	see LED0_TRIG01_CONFIG[TRIG0_RAW]
2:0	*reserved*	RW	0h	Always write 000, ignore on read.

[1] See LED controller 0

7.4.1.56 LED3_TRIG23_CONFIG register

Table 112. LED3_TRIG23_CONFIG register - LED controller 3 Trigger 2 and 3 configuration (address 1AFh)[1]

Bit	Symbol	Access	Value	Description
15	TRIG3_ENABLE	RW	TJF1103A: 1h TJF1103B: 0h	see LED0_TRIG23_CONFIG[TRIG3_ENABLE]
14	TRIG3_POLARITY	RW	TJF1103A: 1h TJF1103B: 0h	see LED0_TRIG23_CONFIG[TRIG3_POLARITY]
13	TRIG3_HILO_ PRIORITY	RW	TJF1103A: 1h TJF1103B: 0h	see LED0_TRIG23_CONFIG[TRIG3_HILO_PRIORITY]
12	TRIG3_SELECT	RW	0h	see LED0_TRIG23_CONFIG[TRIG3_SELECT]
11:10	TRIG3_FUNCTION	RW	0h	see LED0_TRIG23_CONFIG[TRIG3_FUNCTION]
9:8	*reserved*	RW	0h	always write 00, ignore on read.
7	TRIG2_ENABLE	RW	1h	see LED0_TRIG23_CONFIGTRIG2_ENABLE]
6	TRIG2_POLARITY	RW	1h	see LED0_TRIG23_CONFIG[TRIG2_POLARITY]
5	TRIG2_HILO_ PRIORITY	RW	1h	see LED0_TRIG23_CONFIG[TRIG2_HILO_PRIORITY]
4	TRIG2_SELECT	RW	0h	see LED0_TRIG23_CONFIG[TRIG2_SELECT]
3	TRIG2_RAW	RW	0h	see LED0_TRIG23_CONFIG[TRIG2_RAW]
2	TRIG2_ MODULATION	RW	0h	see LED0_TRIG23_CONFIG[TRIG2_MODULATION]
1:0	*reserved*	RW	0h	always write 00, ignore on read.

[1] See LED controller 0

7.4.1.57 AO_SYSTEM_SUPPLY_STATUS register

Table 113. AO_SYSTEM_SUPPLY_STATUS register - Always on system supply (address 311h)

Bit	Symbol	Access	Value	Description
15	*reserved*	R	0h	Always write 0, ignore on read.
14	UV_EVENT	RW	0h	If set, an under-voltage event occurred since last clear Write one to clear. This bit is latched-high.
13:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.58 CORE_SUPPLY_STATUS register

Table 114. CORE_SUPPLY_STATUS register - Core supply status (address 313h)

Bit	Symbol	Access	Value	Description
15	OV_EVENT	RW	0h	This bit is asserted if a voltage monitor for this supply detects an over-voltage. Write one to clear. This bit is latched-high.
14	UV_EVENT	RW	0h	This bit is asserted if a voltage monitor for this supply detects an under-voltage. Write one to clear. This bit is latched-high.
13	OV_STATUS	R	0h	This bit shows the actual over-voltage status as measured by the voltage monitor of this supply. If set, there is an over-voltage condition present. If there is no voltage monitor implemented for this supply, this bit reads zero.
12	UV_STATUS	R	0h	This bit shows the actual under-voltage status as measured by the voltage monitor of this supply. If set, there is an under-voltage condition present. If there is no voltage monitor implemented for this supply, this bit reads zero.
11	OV_LATENT_FAULT	RW	0h	This bit is asserted if no over-voltage is detected by an over-voltage latent-fault test. This bit can only get asserted during the FuSa test procedure at device power-up or wake-up from sleep. A detected latent-fault creates an interrupt trigger pulse Write one to clear. This bit is latched-high.
10	UV_LATENT_FAULT	RW	0h	This bit is asserted if no under-voltage is detected by an under-voltage latent fault test. This bit can only get asserted during the FuSa test procedure at device power-up or wake-up from sleep. A detected latent-fault creates an interrupt trigger pulse Write one to clear. This bit is latched-high.
9:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.59 VDDIO_SUPPLY_STATUS register

Table 115. VDDIO_SUPPLY_STATUS register - VDDIO supply status (address 315h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	*reserved*	R	0h	Always write 0, ignore on read.
14	UV_EVENT	RW	0h	If set, an under-voltage occurred. Write one to clear. This bit is latched-high.
13:2	*reserved*	R	0h	Always write all 0s, ignore on read.
1:0	VDDIO_LEVEL	R		Detected IO supply level
			00*	Reserved
			01	1.8 V
			10	2.5 V
			11	3.3 V

7.4.1.60 VREGD_SUPPLY_STATUS register

Table 116. VREGD_SUPPLY_STATUS register - VREGD supply status (address 318h)

Bit	Symbol	Access	Value	Description
15	OV_EVENT	RW	0h	This bit is asserted if a voltage monitor for this supply detects an under-voltage. This bit is asserted if a voltage monitor for this supply detects an over-voltage. Write one to clear. This bit is latched-high.
14	*reserved*	R	0h	Always write 0, ignore on read.
13	OV_STATUS	R	0h	This bit shows the actual over-voltage status as measured by the voltage monitor of this supply. If set, there is an over-voltage condition present. If there is no voltage monitor implemented for this supply, this bit reads zero.
12	*reserved*	R	0h	Always write 0, ignore on read.
11	OV_LATENT_FAULT	RW	0h	This bit gets asserted if no over-voltage is detected by an over-voltage latent-fault test. This bit can only get asserted during the FuSa test procedure at device power-up or wake-up from sleep. A detected latent-fault creates an interrupt trigger pulse Write one to clear. This bit is latched-high.
10:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.61 VREGA_SUPPLY_STATUS register

Table 117. VREGA_SUPPLY_STATUS register - VREGA supply status (address 319h)

Bit	Symbol	Access	Value	Description
15	OV_EVENT	RW	0h	This bit is asserted if a voltage monitor for this supply detects an under-voltage. This bit is asserted if a voltage monitor for this supply detects an over-voltage.

Table 117. VREGA_SUPPLY_STATUS register - VREGA supply status (address 319h)*...continued*

Bit	Symbol	Access	Value	Description
				Write one to clear. This bit is latched-high.
14	*reserved*	R	0h	Always write 0, ignore on read.
13	OV_STATUS	R	0h	This bit shows the actual over-voltage status as measured by the voltage monitor of this supply. If set, there is an over-voltage condition present. If there is no voltage monitor implemented for this supply, this bit reads zero.
12	*reserved*	R	0h	Always write 0, ignore on read.
11	OV_LATENT_FAULT	RW	0h	This bit gets asserted if no over-voltage is detected by an over-voltage latent-fault test. This bit can only get asserted during the FuSa test procedure at device power-up or wake-up from sleep. A detected latent-fault creates an interrupt trigger pulse Write one to clear. This bit is latched-high.
10:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.62 VDDA_TRX_SUPPLY register

Table 118. VDDA_TRX_SUPPLY register - VDDA_TRX supply status (address 31Ah)

Bit	Symbol	Access	Value	Description
15	OV_EVENT	RW	0h	This bit is asserted if a voltage monitor for this supply detects an under-voltage. This bit is asserted if a voltage monitor for this supply detects an over-voltage. Write one to clear. This bit is latched-high.
14	UV_EVENT	RW	0h	This bit is asserted if a voltage monitor for this supply detects an over-voltage. Write one to clear. This bit is latched-high.
13	OV_STATUS	R	0h	This bit shows the actual over-voltage status as measured by the voltage monitor of this supply. If set, there is an over-voltage condition present. If there is no voltage monitor implemented for this supply, this bit reads zero.
12	UV_STATUS	R	0h	This bit shows the actual under-voltage status as measured by the voltage monitor of this supply. If set, there is an under-voltage condition present. If there is no voltage monitor implemented for this supply, this bit reads zero.
11	OV_LATENT_FAULT	RW	0h	This bit gets asserted if no over-voltage is detected by an over-voltage latent-fault test. This bit can only get asserted during the FuSa test procedure at device power-up or wake-up from sleep. A detected latent-fault creates an interrupt trigger pulse Write one to clear. This bit is latched-high.
10	UV_LATENT_FAULT	RW	0h	This bit gets asserted if no under-voltage is detected by an under-voltage latent fault test. This bit can only get asserted during the FuSa test procedure at device power-up or wake-

Table 118. VDDA_TRX_SUPPLY register - VDDA_TRX supply status (address 31Ah)*...continued*

Bit	Symbol	Access	Value	Description
				up from sleep. A detected latent-fault creates an interrupt trigger pulse Write one to clear. This bit is latched-high.
9:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.63 OSC_STATUS register

Table 119. OSC_STATUS register - XO status (address 31Eh)

Bit	Symbol	Access	Value	Description
15	HIGH_FQ_EVENT	RW	0h	If set, ratio between the oscillator and FRO frequencies was too high. Write one to clear. This bit is latched-high.
14	LOW_FQ_EVENT	RW	0h	If set, ratio between the oscillator and FRO frequencies was too low. Write one to clear. This bit is latched-high.
13	HIGH_FQ_NOW	R	0h	If set, current ratio between oscillator and FRO frequencies is too high
12	LOW_FQ_NOW	R	0h	If set, current ratio between oscillator and FRO frequencies is too low
11	CLK_PRESENT	R	0h	Set if oscillator clock is detected to be present
10:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.64 TEMP_STATUS register

Table 120. TEMP_STATUS register - Tempature status (address 31Fh)

Bit	Symbol	Access	Value	Description
15	HIGH_TEMP_ EVENT	RW	0h	If set, a temperature beyond TEMP_LIMIT has occured since last clear. Write one to clear. This bit is latched-high.
14	*reserved*	R	0h	Always write 0, ignore on read.
13	HIGH_TEMP_NOW	R	0h	If set, the die temperature is above TEMP_LIMIT now
12	*reserved*	R	0h	Always write 0, ignore on read.
11	HIGH_TEMP_ LATENT_FAULT	RW	0h	If set, the temperature sensor latent-fault test failed Write one to clear. This bit is latched-high.
10:8	*reserved*	R	0h	Always write 000, ignore on read.
7:0	TEMP_LIMIT	RW	A1h	Sets the current temperature warning limit in degrees Celsius. The temperature needs to be converted as follows: Temperature Warning Limit = 7.22*x^2 + 38.8*x + 65.3 with x = TEMP_LIMIT/100 Note: valid range is from 41h to BFh (93 °C to 165 °C)

Table 120. TEMP_STATUS register - Tempature status (address 31Fh)*...continued*

Bit	Symbol	Access	Value	Description
				See application note (section 5.6) for further details

7.4.1.65 COMPL_TEST_INTF register

Table 121. COMPL_TEST_INTF register - Compliance test interface (address 3F4h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	TEST_INTF_EN	RW	0h	If set, enables device test interface
14	*reserved*	RW	0h	Always write 0, ignore on read.
11:8	FUNC_SEL	RW		Test function select
			0001*	Selects Ethernet PHY for test
			others	Reserved
7:6	*reserved*	R	0h	Always write 00, ignore on read.
5	COMPL_TCLK_EN	RW	0h	If set, TCLK outout is enabled on the test interface
4:0	TEST_PORT_NR	RW	1h	Selected port number for the test. This must be set to 1.

7.4.1.66 PTP_IDENTIFIER register

Table 122. PTP_IDENTIFIER register - PTP IP identifier register (address 1100h)

Bit	Symbol	Access	Value	Description
15:8	*reserved*	R	0h	Ignore on read.
7:4	PTP_VERSION	R	1h	PTP IP version.
3:0	PTP_REVISION	R	0h	PTP module revision

7.4.1.67 PTP_CONTROL register

Table 123. PTP_CONTROL register - General control (address 1101h)

Bit	Symbol	Access	Value	Description
15:1	*reserved*	R	0h	Always write all 0s, ignore on read.
0	SOFT_RESET	RW	0h	If asserted, the PTP block is reset. This is self-clearing bit.

7.4.1.68 PTP_CONFIG register

Table 124. PTP_CONFIG register - General control (address 1102h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:5	*reserved*	R	0h	Always write all 0s, ignore on read.
4	PPS_SYNC_RETURN	RW		Return external PPS_SYNC on PPS_OUT
			0*	Synchronized (ptp_clk) external pps_sync is not routed back on PPS_OUT
			1	Synchronized (ptp_clk) external pps_sync is routed back on PPS_OUT

Table 124. PTP_CONFIG register - General control (address 1102h)*...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
3	PPS_OUT_EN	RW		Enable the PPS_OUT signal generation
			0*	PPS_OUT is not generated
			1	PPS_OUT is generated
2	PPS_OUT_POL	RW		Inverts the polarity of generated output 1 PPS signal.
			0*	No inversion
			1	Invert a 1 PPS out
1	EXT_TRG_EDGE_SEL	RW		Inversion control of external trigger event
			0*	Rising edge of external trigger event is timestamped
			1	Falling edge of external trigger event is timestamped
0	EXT_PPS_EDGE_SEL	RW		When switching this bit, inverted PPS Sync may be disturbed for first pulse after bit is switched. However switching this bit will not have any disturbance on PPS sync timestamping. This bit is not dynamically changing bit.
			0*	Rising edge of external PPS sync is timestamped and used in all places
			1	Falling edge of external PPS sync is timestamped and inverted PPS sync is used in all places

7.4.1.69 PTP_ABILITY register

Table 125. PTP_ABILITY register - PTP IP Ability registers (address 1103h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:3	*reserved*	R	0h	Ignore on read.
2	INGRESS_IN_BAND	R		Indicates PTP IP supports insertion of timestamping information in "reserved" field.
			0	Does not support in-band deliver
			1*	Supports in-band deliver
1	PTP_TWO_STEP	R		Indicates PTP IP supports two-step operation.
			0	Does not support two-step operation
			1*	Supports TWO-step operation
0	PTP_ONE_STEP	R		Indicates PTP IP supports one-step operation.
			0*	Does not support one-step operation
			1	Supports one-step operation

7.4.1.70 PTP_CLK_PERIOD register

Table 126. PTP_CLK_PERIOD register - Clock period of ptp_clk (address 1104h)

Bit	Symbol	Access	Value	Description
15:8	*reserved*	R	0h	Always write all 0s, ignore on read.

Table 126. PTP_CLK_PERIOD register - Clock period of ptp_clk (address 1104h)*...continued*

Bit	Symbol	Access	Value	Description
7:0	PTP_CLK_PERIOD	RW	8h	Clock period of ptp_clk. Local LTC increment its counters by this value for every ptp clock tick. In 100BT1, it is 15ns (66.66MHz). In 1000BT1, it is 8ns (125MHz)

7.4.1.71 LTC_LOAD_CTRL register

Table 127. LTC_LOAD_CTRL register - LTC load and read control (address 1105h)

Bit	Symbol	Access	Value	Description
15:3	*reserved*	R	0h	Always write all 0s, ignore on read.
2	READ_LTC	RW	0h	When set, captures the current internal LTC clock time in LTC_RD_NSEC_0/1, LTC_RD_SEC_0/1 & LTC_RD_SUB_NS_0/1 register. This bit is cleared on capture.
1	LOAD_LTC_PPS	RW	0h	When this bit is set and on next rising edge of external PPS_SYNC signal, LTC_WR_SEC_0/1 & LTC_WR_NSEC_0/1 is loaded into the LTC. This bit is cleared after the loading at PPS edge(with additional 4-5 APB clocks (CDC latency)) This bit should be programmed only after LTC_WR_SEC_0/1 & LTC_WR_NSEC_0/1 is written.
0	LOAD_LTC	RW	0h	Self-clearing when LTC_WR_SEC_0/1 & LTC_WR_NSEC_0/1 is loaded into the LTC. This should be set only after LTC_WR_SEC_0/1 & LTC_WR_NSEC_0/1 is written.

7.4.1.72 LTC_WR_NSEC_0 register

Table 128. LTC_WR_NSEC_0 register - Loading nanoseconds counter value (address 1106h)

Bit	Symbol	Access	Value	Description
15:0	LTC_WR_NSEC_0	RW	0h	[15:0] of LTC_WR_NSEC. This is nanoseconds part of clock time loaded into the internal LTC.

7.4.1.73 LTC_WR_NSEC_1 register

Table 129. LTC_WR_NSEC_1 register - Loading nanoseconds counter value (address 1107h)

Bit	Symbol	Access	Value	Description
15:14	*reserved*	R	0h	Always write 00, ignore on read.
13:0	LTC_WR_NSEC_1	RW	0h	[29:16] of LTC_WR_NSEC. This is nanoseconds part of clock time loaded into the internal LTC.

7.4.1.74 LTC_WR_SEC_0 register

Table 130. LTC_WR_SEC_0 register - Loading seconds counter value (address 1108h)

Bit	Symbol	Access	Value	Description
15:0	LTC_WR_SEC_0	RW	0h	[15:0] of LTC_WR_SEC. This is seconds part of clock time loaded into the internal LTC.

7.4.1.75 LTC_WR_SEC_1 register

Table 131. LTC_WR_SEC_1 register - Loading seconds counter value (address 1109h)

Bit	Symbol	Access	Value	Description
15:0	LTC_WR_SEC_1	RW	0h	[31:16] of LTC_WR_SEC. This is seconds part of clock time loaded into the internal LTC.

7.4.1.76 LTC_RD_DATA_0 register

Table 132. LTC_RD_DATA_0 register - Local LTC nanoseconds part (address 110Ah)[1]

Bit	Symbol	Access	Value	Description
15:0	LTC_RD_NSEC_0	R	0h	[15:0] of LTC_RD_NSEC. This reads the value of internal nanoseconds counter.

[1] The value read is the saved value of local counter when READ_LTC is set.

7.4.1.77 LTC_RD_DATA_1 register

Table 133. LTC_RD_DATA_1 register - Local LTC nanoseconds part (address 110Bh)[1]

Bit	Symbol	Access	Value	Description
15:14	*reserved*	R	0h	Always write 00, ignore on read.
13:0	LTC_RD_NSEC_1	R	0h	[29:16] of LTC_RD_NSEC. This reads the value of internal nanoseconds counter.

[1] The value read is the saved value of local counter when READ_LTC is set.

7.4.1.78 LTC_RD_DATA_2 register

Table 134. LTC_RD_DATA_2 register - Local LTC seconds part (address 110Ch)[1]

Bit	Symbol	Access	Value	Description
15:0	LTC_RD_SEC_0	R	0h	[15:0] of LTC_RD_SEC. This reads the value of internal seconds counter.

[1] The value read is the saved value of local counter when READ_LTC is set.

7.4.1.79 LTC_RD_DATA_3 register

Table 135. LTC_RD_DATA_3 register - Local LTC seconds part (address 110Dh)[1]

Bit	Symbol	Access	Value	Description
15:0	LTC_RD_SEC_1	R	0h	[31:16] of LTC_RD_SEC. This reads the value of internal seconds counter.

[1] The value read is the saved value of local counter when READ_LTC is set.

7.4.1.80 LTC_RD_DATA_4 register

Table 136. LTC_RD_DATA_4 register - Local LTC sub-nanoseconds part (address 110Eh)[1]

Bit	Symbol	Access	Value	Description
15:0	LTC_RD_SUBNS	R	0h	[31:16] of sub-ns counter. This reads the value of internal sub-nanoseconds counter.

[1] The value read is the saved value of local counter when READ_LTC is set.

7.4.1.81 RATE_ADJ_SUBNS_0 register

Table 137. RATE_ADJ_SUBNS_0 register - SW Rate adjust value (address 110Fh)

Bit	Symbol	Access	Value	Description
15:0	RATE_ADJ_ SUBNS_0	RW	0h	[15:0] of RATE_ADJ_SUBNS. For every clock ticks, this value is added to the sub-nanoseconds counter. When the sub-nanoseconds counter rolls over past zero, then value 1 will be added or subtracted to the nanoseconds counter based on direction bit.

7.4.1.82 RATE_ADJ_SUBNS_1 register

Table 138. RATE_ADJ_SUBNS_1 register - SW Rate adjust value (address 1110h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	CLK_RATE_ADJ_ LD	RW	0h	Loads new value of rate correction by SW. For every clock ticks, value in RATE_ADJ_SUBNS is applied for rate correction. This bit is cleared after 4-5 APB clocks (CDC latency). This bit should be programmed after all required configuration registers has been programmed including SW adjustment is selected.
14	CLK_RATE_ADJ_ DIR	RW		Clock rate adjust direction
			0*	For every clock ticks, value in RATE_ADJ_SUBNS is added to the sub-nanoseconds counter. Value 1 is subtracted from the nanoseconds counter when sub-nanoseconds counter rolls over past zero.
			1	For every clock ticks, value in RATE_ADJ_SUBNS is added to the sub-nanoseconds counter. Value 1 is added to the nanoseconds counter when sub-nanoseconds counter rolls over past zero.
13:0	RATE_ADJ_ SUBNS_1	RW	0h	[29:16] of RATE_ADJ_SUBNS. For every clock ticks, this value is added to the sub-nanoseconds counter. When the sub-nanoseconds counter rolls over past zero, then value 1 will be added or subtracted to the nanoseconds counter based on direction bit.

7.4.1.83 TEMP_ADJ_SUBNS_0 register

Table 139. TEMP_ADJ_SUBNS_0 register - SW temporary rate adjust value (address 1111h)

Bit	Symbol	Access	Value	Description
15:0	TEMP_ADJ_SUBNS_0	RW	0h	[15:0] of TEMP_ADJ_SUBNS. For a programmable clock duration, this value is added to the sub-nanoseconds counter. When the sub-nanoseconds counter rolls over past zero, then value 1 will be added or subtracted to the nanoseconds counter based on direction bit.

7.4.1.84 TEMP_ADJ_SUBNS_1 register

Table 140. TEMP_ADJ_SUBNS_1 register - SW temporary rate adjust value (address 1112h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	CLK_LD_TEMP_ADJ	RW	0h	Setting a bit triggers the temporary adjustment for a programmed duration (TEMP_ADJ_DUR). This bit is cleared after the programmed duration is elapsed (with additional 4-5 APB clocks (CDC latency)). This bit should be programmed after all required configuration registers has been programmed including SW adjustment is selected.
14	CLK_TEMP_ADJ_DIR	RW		Clock temporaray adjustment direction
			0*	Value 1 is subtracted from the nanoseconds counter when sub-nanoseconds counter rolls over past zero.
			1	Value 1 is added to the nanoseconds counter when sub-nanoseconds counter rolls over past zero.
13:0	TEMP_ADJ_SUBNS_1	RW	0h	[29:16] of TEMP_ADJ_SUBNS. For a programmable clock duration, this value is added to the sub-nanoseconds counter. When the sub-nanoseconds counter rolls over past zero, then value 1 will be added or subtracted to the nanoseconds counter based on direction bit.

7.4.1.85 TEMP_ADJ_DUR_0 register

Table 141. TEMP_ADJ_DUR_0 register - Temporary adjustment window (address 1113h)

Bit	Symbol	Access	Value	Description
15:0	TEMP_ADJ_DUR_0	RW	0h	[15:0] of TEMP_ADJ_DUR. Number of clock ticks during which temporary adjustment is applied.

7.4.1.86 TEMP_ADJ_DUR_1 register

Table 142. TEMP_ADJ_DUR_1 register - Temporary adjustment window (address 1114h)

Bit	Symbol	Access	Value	Description
15:0	TEMP_ADJ_DUR_1	RW	0h	[31:16] of TEMP_ADJ_DUR. Number of clock ticks during which temporary adjustment is applied.

7.4.1.87 HW_LTC_LOCK_CTRL register

Table 143. HW_LTC_LOCK_CTRL register - HW LTC self locking.control (address 1115h)

Bit	Symbol	Access	Value	Description
15:1	*reserved*	R	0h	Always write all 0s, ignore on read.
0	HW_LTC_LOCK_EN	RW	1h	Rate correction and offset correction is handled by HW. This takes the precedence over SW adjustment.

7.4.1.88 HW_EXT_PPS_NS_0 register

Table 144. HW_EXT_PPS_NS_0 register - Period of external PPS sync in nanosecond. Used for HW LTC self locking. (address 1116h)

Bit	Symbol	Access	Value	Description
15:0	HW_EXT_PPS_NS_0	RW	CA00h	[15:0] of period of external PPS sync in terms of nanosecond.

7.4.1.89 HW_EXT_PPS_NS_1 register

Table 145. HW_EXT_PPS_NS_1 register - Period of external PPS sync in nanosecond. Used for HW LTC self locking. (address 1117h)

Bit	Symbol	Access	Value	Description
15:14	*reserved*	R	0h	Always write 00, ignore on read.
13:0	HW_EXT_PPS_NS_1	RW	3B9Ah	[29:16] of period of external PPS sync in terms of nanosecond.

7.4.1.90 HW_LOCK_ER_LMT_0 register

Table 146. HW_LOCK_ER_LMT_0 register - Error limitation by HW LTC self locking engine (address 1118h)

Bit	Symbol	Access	Value	Description
15:0	HW_LOCK_ER_LMT_0	RW	D090h	[15:0] of HW_LOCK_ER_LMT. This register limits the number of nanoseconds beyond which HW can not self-lock with external PPS sync. Interrupt is asserted if the error correction limit is exceeded.

7.4.1.91 HW_LOCK_ER_LMT_1 register

Table 147. HW_LOCK_ER_LMT_1 register - Error limitation by HW LTC self locking engine (address 1119h)

Bit	Symbol	Access	Value	Description
15:8	*reserved*	R	0h	Always write all 0s, ignore on read.
7:0	HW_LOCK_ER_LMT_1	RW	3h	[23:16] of HW_LOCK_ER_LMT. This register limits the number of nanoseconds beyond which HW can not self-lock with external PPS sync. Interrupt is asserted if the error correction limit is exceeded.

7.4.1.92 LTC_LOOP_CONTROL register

Table 148. LTC_LOOP_CONTROL register (address 111Ah)[1]

Bit	Symbol	Access	Value	Description
15:12	*reserved*	R	0h	Always write 0000, ignore on read.
11:8	PROP_GAIN	RW	3h	Proportional path gain as 2^-PROP_GAIN
7:5	*reserved*	R	0h	Always write 000, ignore on read.
4:0	INTEGRAL_GAIN	RW	3h	Integrating path gain as 2^-INTEGRAL_GAIN

[1] This register defines control parameters to adapt behavior of the LTC loop if HW_LTC_LOCK_EN=1.

7.4.1.93 EXT_PPS_TS_DATA0 register

Table 149. EXT_PPS_TS_DATA0 register - Timestamping data on the event of rising edge of external pps signal (address 111Bh)[1]

Bit	Symbol	Access	Value	Description
15:0	EXT_PPS_TS_ DATA0	R	0h	[15:0] of EXT_PPS_TS_NSEC. Holds nanoseconds part of clock time at the event of rising edge of external pps sync.

[1] Reading this register copied into snapshot register for multiple reads of EXT_PPS_TS_DATA0/1/2/3/4/5 register.

7.4.1.94 EXT_PPS_TS_DATA1 register

Table 150. EXT_PPS_TS_DATA1 register - Timestamping data on the event of rising edge of external pps signal (address 111Ch)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:14	*reserved*	R	0h	Always write 00, ignore on read.
13:0	EXT_PPS_TS_ DATA1	R	0h	[29:16] of EXT_PPS_TS_NSEC. Holds nanoseconds part of clock time at the event of rising edge of external pps sync.

7.4.1.95 EXT_PPS_TS_DATA2 register

Table 151. EXT_PPS_TS_DATA2 register - Timestamping data on the event of rising edge of external pps signal (address 111Dh)

Bit	Symbol	Access	Value	Description
15:0	EXT_PPS_TS_ DATA2	R	0h	[15:0] of PTP_EXT_PPS_TS_SEC. Holds seconds part of clock time at the event of rising edge of external pps sync.

7.4.1.96 EXT_PPS_TS_DATA3 register

Table 152. EXT_PPS_TS_DATA3 register - Timestamping data on the event of rising edge of external pps signal (address 111Eh)

Bit	Symbol	Access	Value	Description
15:0	EXT_PPS_TS_ DATA3	R	0h	[31:16] of PTP_EXT_PPS_TS_SEC. Holds seconds part of clock time at the event of rising edge of external pps sync.

7.4.1.97 EXT_PPS_TS_DATA4 register

Table 153. EXT_PPS_TS_DATA4 register - Timestamping data on the event of rising edge of external pps signal (address 111Fh)

Bit	Symbol	Access	Value	Description
15:0	EXT_PPS_TS_DATA4	R	0h	[31:16] of sub-ns counter. Holds sub-nanoseconds part of clock time at the event of rising edge of external pps sync.

7.4.1.98 EXT_PPS_TS_CTRL register

Table 154. EXT_PPS_TS_CTRL register - External PPS timestamp reading done (address 1120h)

Bit	Symbol	Access	Value	Description
15:1	*reserved*	R	0h	Always write all 0s, ignore on read.
0	EXT_PPS_TS_DONE	RW	0h	Once EXT_PPS_TS_DATA is read and there is no need to further re-read the same data set, then this bit should be set to '1'. This is self-clearing bit.

7.4.1.99 EXT_TRG_TS_DATA0 register

Table 155. EXT_TRG_TS_DATA0 register - Timestamping data on the eventof rising edge of external trigger event signal (address 1121h)[1]

Bit	Symbol	Access	Value	Description
15:0	EXT_TRG_TS_DATA0	R	0h	[15:0] of EXT_TRG_TS_NSEC Holds nanoseconds part of clock time at the event of rising edge of external trigger event signal.

[1] Reading this register copied into snapshot register for multiple reads of EXT_TRG_TS_DATA0/1/2/3/4/5 register.

7.4.1.100 EXT_TRG_TS_DATA1 register

Table 156. EXT_TRG_TS_DATA1 register - Timestamping data of external trigger event signal (address 1122h)

Bit	Symbol	Access	Value	Description
15:14	*reserved*	R	0h	Always write 00, ignore on read.
13:0	EXT_TRG_TS_DATA1	R	0h	[29:16] of EXT_TRG_TS_NSEC Holds nanoseconds part of clock time at the event of rising edge of external trigger event signal.

7.4.1.101 EXT_TRG_TS_DATA2 register

Table 157. EXT_TRG_TS_DATA2 register - Timestamping data of external trigger event signal (address 1123h)

Bit	Symbol	Access	Value	Description
15:0	EXT_TRG_TS_DATA2	R	0h	[15:0] of EXT_TRG_TS_SEC. Holds seconds part of clock time at the event of rising edge of external trigger event signal.

7.4.1.102 EXT_TRG_TS_DATA3 register

Table 158. EXT_TRG_TS_DATA3 register - Timestamping data of external trigger event signal (address 1124h)

Bit	Symbol	Access	Value	Description
15:0	EXT_TRG_TS_DATA3	R	0h	[31:16] of EXT_TRG_TS_SEC. Holds seconds part of clock time at the event of rising edge of external trigger event signal.

7.4.1.103 EXT_TRG_TS_DATA4 register

Table 159. EXT_TRG_TS_DATA4 register - Timestamping data of external trigger event signal (address 1125h)

Bit	Symbol	Access	Value	Description
15:0	EXT_TRG_TS_DATA4	R	0h	[31:16] of sub-ns counter. Holds sub-nanoseconds part of clock time at the event of rising edge of external trigger event signal.

7.4.1.104 EXT_TRG_TS_CTRL register

Table 160. EXT_TRG_TS_CTRL register - External trigger event timestamp reading done (address 1126h)

Bit	Symbol	Access	Value	Description
15:1	*reserved*	R	0h	Always write all 0s, ignore on read.
0	EXT_TRG_TS_DONE	RW	0h	Once EXT_TRG_TS_DATA is read and no need to further read the same data set, then this bit should be set to '1'. This is self-clearing bit.

7.4.1.105 PTP_IRQ_SOURCE register

Table 161. PTP_IRQ_SOURCE register - Interrupt status signals (address 1130h)

Bit	Symbol	Access	Value	Description
15:11	*reserved*	R	0h	Always write 00000, ignore on read.
10	RX_SOF_LOST	RW	0h	RX SOF is not detected when ptp event packet is received. Interrupt status is cleared when it is written to 1 (self-clear bit).
9	TX_SOF_LOST	RW	0h	TX SOF is not detected when ptp event packet is received. Interrupt status is cleared when it is written to 1 (self-clear bit).
8	FRAME_ERROR	RW	0h	Detected errors in ingress path: 1) Detected pre-amble, but no detection of an SFD. 2) Prematurely ended PTP frame before all required fields for the time-stamp have been received. Interrupt status is cleared when it is written to 1 (self-clear bit).
7	FCS_ERROR	RW	0h	Incorrect FCS value observed on a received PTP frame. Note that this is only available if ingress in-band time-stamping is enabled. Interrupt status is cleared when it is written to 1 (self-clear bit).

Table 161. PTP_IRQ_SOURCE register - Interrupt status signals (address 1130h)*...continued*

Bit	Symbol	Access	Value	Description
6	ING_TS_LOST	RW	0h	New ingress time-stamp has overwritten the oldest unread time-stamp in the buffer. Interrupt status is cleared when it is written to 1 (self-clear bit).
5	EGR_TS_LOST	RW	0h	New egress time-stamp has overwritten the oldest unread time-stamp in the buffer. Interrupt status is cleared when it is written to 1 (self-clear bit).
4	PDIFF_EXCEED	RW	0h	Interrupt status when harware measured phase diff between external PPS sync and local LTC is exceeded the limit. (250us is limit if 1 PPS period is 1 second time). Interrupt status is cleared when it is written to 1 (self-clear bit).
3	PPSOUT	RW	0h	Interrupt status when PPS out is generated. Interrupt status is cleared when it is written to 1 (self-clear bit)
2	SEC_CNT_OVF	R	0h	Interrupt status when 32 bit seconds counter is saturated. Interrupt status is cleared when LTC counters are re-initialized or soft reset is applied.
1	ING_TS	R	0h	This bit is signaling the presence of time-stamps in the ingress buffer. It has been intentionally made non-latching as otherwise a new stamp could be taken between emptying the buffer and resetting this interrupt bit, in which case the new time-stamp wouldn't be flagged. This bit indicating the actual presence of time-stamps in the buffer doesn't require a reset as it will automatically disappear when the buffer becomes empty, and it will be set again when a new time-stamp is taken.
0	EGR_TS	R	0h	This bit is signaling the presence of time-stamps in the egress buffer. It has been intentionally made non-latching as otherwise a new stamp could be taken between emptying the buffer and resetting this interrupt bit, in which case the new time-stamp wouldn't be flagged. This bit indicating the actual presence of time-stamps in the buffer doesn't require a reset as it will automatically disappear when the buffer becomes empty, and it will be set again when a new time-stamp is taken.

7.4.1.106 PTP_IRQ_ENABLE register

Table 162. PTP_IRQ_ENABLE register - Interrupt enable control (address 1131h)

Bit	Symbol	Access	Value	Description
15:11	*reserved*	R	0h	Always write 00000, ignore on read.
10	RX_SOF_LOST	RW	0h	Enable for respective interrupt
9	TX_SOF_LOST	RW	0h	Enable for respective interrupt
8	FRAME_ERROR	RW	0h	Enable for respective interrupt
7	FCS_ERROR	RW	0h	Enable for respective interrupt
6	ING_TS_LOST	RW	0h	Enable for respective interrupt
5	EGR_TS_LOST	RW	0h	Enable for respective interrupt
4	PDIFF_EXCEED	RW	0h	Enable for respective interrupt
3	PPSOUT	RW	0h	Enable for respective interrupt

Table 162. PTP_IRQ_ENABLE register - Interrupt enable control (address 1131h)*...continued*

Bit	Symbol	Access	Value	Description
2	SEC_CNT_OVF	RW	0h	Enable for respective interrupt
1	ING_TS	RW	0h	Enable for respective interrupt
0	EGR_TS	RW	0h	Enable for respective interrupt

7.4.1.107 PTP_IRQ_MSTATUS register

Table 163. PTP_IRQ_MSTATUS register - Interrupt status signals (address 1132h)

Bit	Symbol	Access	Value	Description
15:11	*reserved*	R	0h	Ignore on read.
10	RX_SOF_LOST	R	0h	Masked status of the respective interrupt
9	TX_SOF_LOST	R	0h	Masked status of the respective interrupt
8	FRAME_ERROR	R	0h	Masked status of the respective interrupt
7	FCS_ERROR	R	0h	Masked status of the respective interrupt
6	ING_TS_LOST	R	0h	Masked status of the respective interrupt
5	EGR_TS_LOST	R	0h	Masked status of the respective interrupt
4	PDIFF_EXCEED	R	0h	Masked status of the respective interrupt
3	PPSOUT	R	0h	Masked status of the respective interrupt
2	SEC_CNT_OVF	R	0h	Masked status of the respective interrupt
1	ING_TS	R	0h	Masked status of the respective interrupt
0	EGR_TS	R	0h	Masked status of the respective interrupt

7.4.1.108 PKT_FILT_CTRL register

Table 164. PKT_FILT_CTRL register - Ingress or egress packet filtering (address 1140h)

Bit	Symbol	Access	Value	Description
15	*reserved*	R	0h	Always write 0, ignore on read.
14	VLAN_TAG_ALLOW	RW	0h	Controls whether VLAN tagged PTP frame is are considered for timestamp. If set, VLAN tagged frames are alllowed.
13:6	DOMAIN_NUM	RW	0h	Domain number to be compared with received versionPTP field to qualify PTP frame.
5	DOMAIN_FILT_EN	RW	0h	Controls whether domainNumber to be checked against DOMAIN_NUM.
4:1	VERSION	RW	0h	This value is compared against received versionPTP field to qualify PTP frame.
0	VERSION_FILT_EN	RW	0h	Controls whether received versionPTP to be checked against programmed version to qualify PTP frame. If set, the version PTP field is checked against VERSION.

7.4.1.109 DA_FILT_CTRL register

Table 165. DA_FILT_CTRL register - Ingress or egress packet DA filtering. (address 1141h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:3	*reserved*	R	0h	Always write all 0s, ignore on read.
2	DA_FILT_EN_USR	RW		Controls whether user DA can be used for honoring PTP message.
			0*	If any DA filter bits are set, then the received DA should match either one of the specified DA of the respective DA filter bit is set. If none of the DA filter bits are set, then all PTP messages are honored.
			1	Match the received DA with programmed user DA. If matched, then honor the PTP message.
1	DA_FILT_EN_FIX2	RW		Controls whether fixed DA (01:1B:19:00:00:00) can be used for honoring PTP message.
			0	If any DA filter bits are set, then the received DA should match either one of the specified DA of the respective DA filter bit is set. If none of the DA filter bits are set, then all PTP messages are honored.
			1*	Match the received DA with (01:1B:19:00:00:00). If matched, then honor the PTP message.
0	DA_FILT_EN_FIX1	RW		Controls whether fixed DA (01:80:C2:00:00:0E) can be used for honoring PTP message.
			0	If any DA filter bits are set, then the received DA should match either one of the specified DA of the respective DA filter bit is set. If none of the DA filter bits are set, then all PTP messages are honored.
			1*	Match the received DA with (01:80:C2:00:00:0E). If matched, then honor the PTP message.

7.4.1.110 USER_MAC_DA_0 register

Table 166. USER_MAC_DA_0 register - [15:0] of User defined MAC address (address 1142h)

Bit	Symbol	Access	Value	Description
15:0	USER_MAC_DA_0	RW	0h	[15:0] of User defined MAC address

7.4.1.111 USER_MAC_DA_1 register

Table 167. USER_MAC_DA_1 register - [31:16] of User defined MAC address (address 1143h)

Bit	Symbol	Access	Value	Description
15:0	USER_MAC_DA_1	RW	0h	[31:16] of User defined MAC address

7.4.1.112 USER_MAC_DA_2 register

Table 168. USER_MAC_DA_2 register - [47:32] of User defined MAC address (address 1144h)

Bit	Symbol	Access	Value	Description
15:0	USER_MAC_DA_2	RW	0h	[47:32] of User defined MAC address

7.4.1.113 USER_DA_MASK_0 register

Table 169. USER_DA_MASK_0 register - User MAC DA Mask control (address 1145h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:0	USER_DA_MASK_0	RW		Controls [15:0] of User MAC DA Mask bits
			0*	DA bits are compared for matching.
			1	DA bits are ignored from being matched. Hence DA range comparison is possible.

7.4.1.114 USER_DA_MASK_1 register

Table 170. USER_DA_MASK_1 register - User MAC DA Mask control (address 1146h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:0	USR_DA_MASK_1	RW		Controls [31:16] of User MAC DA Mask bits
			0*	DA bits are compared for matching.
			1	DA bits are ignored from being matched. Hence DA range comparison is possible.

7.4.1.115 USER_DA_MASK_2 register

Table 171. USER_DA_MASK_2 register - User MAC DA Mask control (address 1147h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:0	USR_DA_MASK_2	RW		Controls [47:32] of User MAC DA Mask bits
			0*	DA bits are compared for matching.
			1	DA bits are ignored from being matched. Hence DA range comparison is possible.

7.4.1.116 EVENT_MSG_FILT register

Table 172. EVENT_MSG_FILT register - PTP event message consideration (address 1148h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:4	*reserved*	R	0h	Always write all 0s, ignore on read.
3	PDLY_RES_FILT	RW		Controls whether Pdelay_Resp event should be considered for timestamping or not.
			0	Don't timestamp Pdelay_Resp event message.
			1*	Consider Pdelay_Resp event message to be timestamped.
2	PDLY_REQ_FILT	RW		Controls whether Pdelay_Request event should be considered for timestamping or not.
			0	Don't timestamp Pdelay_Request event message.
			1*	Consider Pdelay_Request event message to be timestamped.

Table 172. EVENT_MSG_FILT register - PTP event message consideration (address 1148h)*...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
1	DLY_REQ_FILT	RW		Controls whether Delay_Request event should be considered for timestamping or not.
			0	Don't timestamp Delay_Request event message.
			1*	Consider Delay_Request event message to be timestamped.
0	SYNC_FILT	RW		Controls whether sync event should be considered for timestamping or not.
			0	Don't timestamp Sync event message.
			1*	Consider Sync event message to be timestamped.

7.4.1.117 TX_PIPE_DLY_NS register

Table 173. TX_PIPE_DLY_NS register - Egress data path latency from timestamping point of SOF signal to mdi (nanoseconds part) (address 1149h)

Bit	Symbol	Access	Value	Description
15:0	TX_PIPE_DLY_NS	RW	0h	Egress data path latency from timestamping point of SOF signal to mdi. This is nanoseconds part.

7.4.1.118 TX_PIPEDLY_SUBNS register

Table 174. TX_PIPEDLY_SUBNS register - Egress data path latency from timestamping point of SOF signal to mdi (sub-nanoseconds part) (address 114Ah)

Bit	Symbol	Access	Value	Description
15:4	*reserved*	R	0h	Always write all 0s, ignore on read.
3:0	TX_PIPEDLY_SUBNS	RW	0h	Egress data path latency from timestamping point of SOF signal to mdi. This is sub-nanoseconds part

7.4.1.119 RX_PIPE_DLY_NS register

Table 175. RX_PIPE_DLY_NS register - Ingress data path latency of SOF signal from MDI line to timestamping point (nanoseconds part) (address 114Bh)

Bit	Symbol	Access	Value	Description
15:0	RX_PIPE_DLY_NS	RW	0h	Ingress data path latency of SOF signal from MDI line to timestamping point. This is nanoseconds part.

7.4.1.120 RX_PIPEDLY_SUBNS register

Table 176. RX_PIPEDLY_SUBNS register - Ingress data path latency of SOF signal from MDI line to timestamping point (sub-nanoseconds part) (address 114Ch)

Bit	Symbol	Access	Value	Description
15:4	*reserved*	R	0h	Always write all 0s, ignore on read.

Table 176. RX_PIPEDLY_SUBNS register - Ingress data path latency of SOF signal from MDI line to timestamping point (sub-nanoseconds part) (address 114Ch)*...continued*

Bit	Symbol	Access	Value	Description
3:0	RX_PIPEDLY_SUBNS	RW	0h	Ingress data path latency of SOF signal from MDI line to timestamping point. This is sub-nanoseconds part.

7.4.1.121 RX_TS_INSRT_CTRL register

Table 177. RX_TS_INSRT_CTRL register - Inband timestamp insertion controls at ingress path (address 114Dh)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:9	*reserved*	R	0h	Always write all 0s, ignore on read.
8	ING_TS_INS_BYPS	RW		Ingress timestamp insertion bypass
			0*	Ingress timestamp is inserted into the “reserved” field of ptp header.
			1	Ingress timestamp is not inserted into the “reserved” field of ptp header.
7	ENDIANNESS	RW		Sequence of insertion of calculated timestamp into the “reserved” field
			0*	Little endian: MSByte first, LSByte last
			1	Big endian: LSByte first, MSByte last
6:2	ING_MSG_TS_PTR	RW	4h	A register holds the binary pointer position of the timestamp. Pointer register defines number of bits of subnanoseconds is inserted along with nanosecond. Max is 20.
1:0	ING_TS_INS_FRMT	RW		Defines the format of timestamp to be inserted in reserved 4 octets in the PTP message header.
			0	64-bit nanoseconds counter format1: Inserted timestamp holds lower 32-bit of NANOSECONDS. 64-bit NANOSE CONDS is derived from base counters 32-bit seconds counter and 30-bit nanoseconds counter. Base 32bit seconds counter is converted to nanoseconds format and this value is added to base 30bit nanoseconds counter. The end result is in 64-bit NANOSECONDS value. [4.29s rollover] For ex: seconds counter = 32'h0005; nanoseconds counter = 30'h12 3456 Seconds counter value in nanoseconds = 5 * 30'h3B9A CA00 = 62'h1 2A05 F200 Hence, 64-bit NANOSECONDS = 62'h1 2A05 F200 + 30'h12 3456 = 64'h1 2A18 2656 INSERTED TIMESTAMP = 32'h2A18 2656
			1*	64-bit nanoseconds counter format2: Inserted timestamp holds lower 32-N bits of NANOSECONDS and MSB N bits of sub-ns counter value. 64-bit NANOSECONDS is derived from base counters 32-bit seconds counter and 30-bit nanoseconds counter. Base 32bit seconds counter is converted to nanoseconds format and this value is added to base 30bit nanoseconds counter. The end result is in 64-bit NANOSECONDS value.

Table 177. RX_TS_INSRT_CTRL register - Inband timestamp insertion controls at ingress path (address 114Dh)*...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
				A dedicated register holds the binary pointer position of the timestamp (N). For example if the register value is 0, then inserted timestamp would be lower 32bits of NANOSECONDS; if N=4 then inserted timestamp would be 28 bits of NANOSECONDS and MSB 4-bits of sub-ns counter. [0.268s rollover]. For ex: 64-bit NANOSECONDS = 64'h1 2A18 2656; 32-bit sub-ns counters = 32'h8000; N = 4 INSERTED TIMESTAMP = 32'hA18 2656 8
			2h	32-bit seconds counter and 30-bit nanoseconds counter format: Inserted timestamp holds lower 2 bits of seconds counter field and 30 bits nanoseconds counter field. (Timestamp = {SEC[1:0], NSEC[29:0]})
			3h	Not used

7.4.1.122 EGR_RING_DATA_0 register

Table 178. EGR_RING_DATA_0 register - Timestamping data of egress ptp event message (address 114Eh)[1]

Bit	Symbol	Access	Value	Description
15:0	EGR_RING_DATA_0	R	0h	[7:0] - Domain number corresponding to the reading TS ring buffer. [11:8] - Message type corresponding to the reading TS ring buffer. [14:12] - [4:2] of seconds counter value of a corresponding reading TS ring buffer. [15] - Indicates valid timestamp information is present in reading TS ring buffer.

[1] Reading this register fetches and latches buffered timestamp data set and puts into EGR_RING_DATA_0/1/2/3/4/5.

7.4.1.123 EGR_RING_DATA_1 register

Table 179. EGR_RING_DATA_1 register - Timestamping data of egress ptp event message (address 114Fh)

Bit	Symbol	Access	Value	Description
15:0	EGR_RING_DATA_1	R	0h	SequenceId corresponding to the reading TS ring buffer.

7.4.1.124 EGR_RING_DATA_2 register

Table 180. EGR_RING_DATA_2 register - Timestamping data of egress ptp event message (address 1150h)

Bit	Symbol	Access	Value	Description
15:0	EGR_RING_DATA_2	R	0h	[15:0] of a nanoseconds counter value of a corresponding reading TS ring buffer.

7.4.1.125 EGR_RING_DATA_3 register

Table 181. EGR_RING_DATA_3 register - Timestamping data of egress ptp event message (address 1151h)

Bit	Symbol	Access	Value	Description
15:0	EGR_RING_DATA_3	R	0h	[13:0] - [29:16] of a nanoseconds counter value of a corresponding reading TS ring buffer. [15:14] - [1:0] of a seconds counter value of a corresponding reading TS ring buffer.

7.4.1.126 EGR_RING_DATA_4 register

Table 182. EGR_RING_DATA_4 register - Timestamping data of egress ptp event message (address 1152h)

Bit	Symbol	Access	Value	Description
15:0	EGR_RING_DATA_4	R	0h	[31:16] of a sub-nanoseconds counter value of a corresponding reading TS ring buffer.

7.4.1.127 EGR_RING_DATA_5 register

Table 183. EGR_RING_DATA_5 register - Timestamping data of egress ptp event message (address 1153h)

Bit	Symbol	Access	Value	Description
15:0	EGR_RING_DATA_5	R	0h	[3:0] - [15:12] of a sub-nanoseconds counter value of a corresponding reading TS ring buffer. [15:4] - [16:5] of a seconds counter value of a corresponding reading TS ring buffer.

7.4.1.128 EGR_RING_CTRL register

Table 184. EGR_RING_CTRL register - Egress timestamp termination control (address 1154h)

Bit	Symbol	Access	Value	Description
15:1	*reserved*	R	0h	Always write all 0s, ignore on read.
0	EGR_RING_DONE	RW	0h	Once EGR_RING_DATA is read and no need to further read the same data set, then this bit should be set to '1'. This is self-clearing bit.

7.4.1.129 ING_RING_DATA_0 register

Table 185. ING_RING_DATA_0 register - Timestamping data of egress ptp event message (address 1155h)[1]

Bit	Symbol	Access	Value	Description
15:0	ING_RING_DATA_0	R	0h	[7:0] - Domain number corresponding to the reading TS ring buffer. [11:8] - Message type corresponding to the reading TS ring buffer. [14:12] - [4:2] of seconds counter value of a corresponding reading TS ring buffer. [15] - Indicates valid timestamp information is present in reading TS ring buffer.

[1] Reading this register fetches and latches buffered timestamp data set and puts into ING_RING_DATA_0/1/2/3/4/5.

7.4.1.130 ING_RING_DATA_1 register

Table 186. ING_RING_DATA_1 register - Timestamping data of Ingress ptp event message (address 1156h)

Bit	Symbol	Access	Value	Description
15:0	ING_RING_DATA_1	R	0h	SequenceId corresponding to the reading TS ring buffer.

7.4.1.131 ING_RING_DATA_2 register

Table 187. ING_RING_DATA_2 register - Timestamping data of Ingress ptp event message (address 1157h)

Bit	Symbol	Access	Value	Description
15:0	ING_RING_DATA_2	R	0h	[15:0] of a nanoseconds counter value of a corresponding reading TS ring buffer.

7.4.1.132 ING_RING_DATA_3 register

Table 188. ING_RING_DATA_3 register - Timestamping data of Ingress ptp event message (address 1158h)

Bit	Symbol	Access	Value	Description
15:0	ING_RING_DATA_3	R	0h	[13:0] - [29:16] of a nanoseconds counter value of a corresponding reading TS ring buffer. [15:14] - [1:0] of a seconds counter value of a corresponding reading TS ring buffer.

7.4.1.133 ING_RING_DATA_4 register

Table 189. ING_RING_DATA_4 register - Timestamping data of Ingress ptp event message (address 1159h)

Bit	Symbol	Access	Value	Description
15:0	ING_RING_DATA_4	R	0h	[31:16] of a sub-nanoseconds counter value of a corresponding reading TS ring buffer.

7.4.1.134 ING_RING_DATA_5 register

Table 190. ING_RING_DATA_5 register - Timestamping data of Ingress ptp event message (address 115Ah)

Bit	Symbol	Access	Value	Description
15:0	ING_RING_DATA_5	R	0h	[3:0] - [15:12] of a sub-nanoseconds counter value of a corresponding reading TS ring buffer. [15:4] - [16:5] of a seconds counter value of a corresponding reading TS ring buffer.

7.4.1.135 ING_RING_CTRL register

Table 191. ING_RING_CTRL register - Ingress timestamp termination control (address 115Bh)

Bit	Symbol	Access	Value	Description
15:1	*reserved*	R	0h	Always write all 0s, ignore on read.
0	ING_RING_DONE	RW	0h	Once ING_RING_DATA is read and no need to further read the same data set, then this bit should be set to '1'. This is self-clearing bit.

7.4.1.136 PTP_PKT_RCV_CNT register

Table 192. PTP_PKT_RCV_CNT register - Number of received ptp event packet (address 115Fh)

Bit	Symbol	Access	Value	Description
15:8	*reserved*	R	0h	Ignore on read.
7:0	PTP_PKT_RCV_CNT	R	0h	Number of received ptp event packet

7.4.1.137 PTP_FCS_ERR_CNT register

Table 193. PTP_FCS_ERR_CNT register - Number of received ptp event packet has fcs error (address 1160h)

Bit	Symbol	Access	Value	Description
15:8	*reserved*	R	0h	Ignore on read.
7:0	PTP_FCS_ERR_CNT	R	0h	Number of received ptp event packet has fcs error. Note that this is only available if ingress in-band time-stamping is enabled.

7.4.1.138 GLOBAL_INFRA_CONTROL register

Table 194. GLOBAL_INFRA_CONTROL register - Global infrastructure control (address 2C00h)

Bit	Symbol	Access	Value	Description
15	RESET	RW	0h	This resets GPIO controller and LED controller This bit is self-clearing.
14	CONFIG_ENABLE	RW	0h	When this bit is zero (default), the GLOBAL INFRA configuration registers are write-protected. Note that if bit 30.0040h.13 is set to one, this bit overruled and all GLOBAL configuration registers can be changed.
13:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.139 GPIO_OUTPUTS register

Table 195. GPIO_OUTPUTS register - GPIO output (address 2C20h)

Bit	Symbol	Access	Value	Description
15:12	*reserved*	R	0h	Always write all 0s, ignore on read.
11:0	GPIO_OUTS	RW	0h	GPIO output register. Bit driven to if FUNC_SELECT=MISC=111 and SIGNAL_SELECT=REGISTER_OUT=10000 for the corresponding GPIO. If the GPIO is configured to any other function, the corresponding bit in this register is ignored. This register determins the logical value drivin on on of the GPIOS in GPIO_OUTS[11:0]. A GPIO is driven from this register if FUNC_SELECT is set to MISC and SIGNAL_SELECT is set to REGISTER_OUT

7.4.1.140 GPIO_STATUS register

Table 196. GPIO_STATUS register - GPIO status (address 2C21h)

Bit	Symbol	Access	Value	Description
15:12	*reserved*	R	0h	Ignore on read.
0	GPIO_STATUS	R	0h	This register reflects, the current logic level as read from the GPIO pins. Bit GPIO_STATUS[n] corresponds to GPIOn

7.4.1.141 GPIO_IO_CONFIG register

Table 197. GPIO_IO_CONFIG register - GPIO IO configuration (address 2C22h)

Bit	Symbol	Access	Value	Description
15	MANUAL_CONFIG	RW	0h	If set, SLEW_RATE and DRIVE_STRENGTH are used to set the IO configuration. Otherwise default values are used.
14:11	*reserved*	RW	0h	Always write 0000, ignore on read.
10:8	DRIVE_STRENGTH	RW	0h	Select drive strength 0 = weakest 7 = strongest
7:3	*reserved*	RW	0h	Always write 00000, ignore on read.
2:0	SLEW_RATE	RW	0h	Select slew rate of IOs configured for GPIO mode output. 0 = weakest 7 = strongest

7.4.1.142 GPIO_IO_CLK_CONFIG register

Table 198. GPIO_IO_CLK_CONFIG register - GPIO IO CLK configuration (address 2C23h)

Bit	Symbol	Access	Value	Description
15	MANUAL_CONFIG	RW	0h	If set, SLEW_RATE and DRIVE_STRENGTH are used to set the IO configuration. Otherwise default values are used.
14:11	*reserved*	RW	0h	Always write 0000, ignore on read.
10:8	DRIVE_STRENGTH	RW	0h	Select drive strength 0 = weakest 7 = strongest
7:3	*reserved*	RW	0h	Always write 00000, ignore on read.
2:0	SLEW_RATE	RW	0h	Select slew rate of IOs configured for GPIO CLK mode. 0 = weakest 7 = strongest

7.4.1.143 GPIO0_FUNC_CONFIG register

Table 199. GPIO0_FUNC_CONFIG register - GPIO0 function configuration (address 2C40h)[1]

*Legend: *reset value; for GPIO1 to GPIO11 (registers 2C41h to 2C4Bh), the same parameters and reset values apply*

Bit	Symbol	Access	Value	Description
15	ENABLE	RW		If set, GPIO is enabled
			0	For registers GPIO1_FUNC_CONFIG to GPIO11_FUNC_CONFIG, consult description of GPIO0_FUNC_CONFIG

Table 199. GPIO0_FUNC_CONFIG register - GPIO0 function configuration (address 2C40h)[1]*...continued*

*Legend: *reset value; for GPIO1 to GPIO11 (registers 2C41h to 2C4Bh), the same parameters and reset values apply*

Bit	Symbol	Access	Value	Description
14	INVERT	RW	0h	If set, the input and output is invertered
13	PIN_SNIF	RW	0h	If set, pin status readable from register GPIO_STATUS
12:8	*reserved*	R	0h	Always write 00000, ignore on read.
7:5	FUNC_SELECT	RW		Function select
			000	According to default PIN assignment
			001*	LED (output)
			010	PTP
			011	TJF1103A: REG_IN[2] TJF1103B: reserved
			111	MISC
			others	reserved
4:0	SIGNAL_SELECT	RW	0h	Signal select If FUNC_SELECT = LED: xx000 = LED0_A xx001 = LED0_B xx010 = LED1_A xx011 = LED1_B xx100 = LED2_A xx101 = LED2_B xx110 = LED3_A xx111 = LED3_B If FUNC_SELECT = PTP: 0xx00 = PPS_SYNC 0xx01 = PTP_TRIGGER 0xx1x = reserved 1xx00 = TX_SOF 1xx01 = RX_SOF 1xx10 = PPS_OUT 1xx11 = reserved If FUNC_SELECT = MISC: 0xx00 = reserved (TJF1103A)/SNIF (TJF1103B) 1xx00 = REGISTER_OUT 1xx01 = REF_CLK_OUT (only GPIO9) 1xx10 = TX_CLK_OUT otherwise = reserved

[1] All GPIOx function configuration registers are identical.
[2] For REG_IN use case, bit 13 (PIN_SNIF) should be set to corresponding GPIO.

7.4.1.144 PORT_PTP_CONTROL register

Table 200. PORT_PTP_CONTROL register - Port PTP control (address 9000h)

Bit	Symbol	Access	Value	Description
15	RESET	RW	0h	If set the PTP block is reset

Table 200. PORT_PTP_CONTROL register - Port PTP control (address 9000h)*...continued*

Bit	Symbol	Access	Value	Description
				This bit is self-clearing.
14:12	*reserved*	RW	0h	Always write 000, ignore on read.
11	BYPASS	RW	1h	If set, PTP of this port is in bypass
10:0	*reserved*	RW	0h	Always write all 0s, ignore on read.

7.4.1.145 PTP_TS_CAPABILITY register

Table 201. PTP_TS_CAPABILITY register - PTP TS capabilities (address 9200h)

Bit	Symbol	Access	Value	Description
15:2	*reserved*	R	0h	Ignore on read.
1	TX_DELAY_PATH_CAP	R	1h	If set, PHY provides information on transmit path data delay in registers 3.9201 through 3.9204
0	RX_DELAY_PATH_CAP	R	1h	If set, PHY provides information on receive path data delay in registers 3.9205 through 3.9208

7.4.1.146 PTP_TS_TX_MAX_DELAY_LSB register

Table 202. PTP_TS_TX_MAX_DELAY_LSB register - Maximum PTP pcs transmit path data delay LSBs (address 9201h)

Bit	Symbol	Access	Value	Description
15:0	TX_MAX_DELAY_LSB	R	0h	Maximum PCS transmit path data delay in ns, lower

7.4.1.147 PTP_TS_TX_MAX_DELAY_MSB register

Table 203. PTP_TS_TX_MAX_DELAY_MSB register - Maximum PTP pcs transmit path data delay MSBs (address 9202h)

Bit	Symbol	Access	Value	Description
15:0	TX_MAX_DELAY_MSB	R	0h	Maximum PCS transmit path data delay in ns, upper

7.4.1.148 PTP_TS_TX_MIN_DELAY_LSB register

Table 204. PTP_TS_TX_MIN_DELAY_LSB register - Minimum PTP pcs transmit path data delay MSBs (address 9203h)

Bit	Symbol	Access	Value	Description
15:0	TX_MIN_DELAY_LSB	R	0h	Minimum PCS transmit path data delay in ns, lower

7.4.1.149 PTP_TS_TX_MIN_DELAY_MSB register

Table 205. PTP_TS_TX_MIN_DELAY_MSB register - Minimum PTP pcs transmit path data delay MSBs (address 9204h)

Bit	Symbol	Access	Value	Description
15:0	TX_MIN_DELAY_MSB	R	0h	Minimum PCS transmit path data delay in ns, upper

7.4.1.150 PTP_TS_RX_MAX_DELAY_LSB register

Table 206. PTP_TS_RX_MAX_DELAY_LSB register - Maximum PTP pcs receive path data delay LSBs (address 9205h)

Bit	Symbol	Access	Value	Description
15:0	RX_MAX_DELAY_LSB	R	0h	Maximum PCS receive path data delay in ns, lower

7.4.1.151 PTP_TS_RX_MAX_DELAY_MSB register

Table 207. PTP_TS_RX_MAX_DELAY_MSB register - Maximum PTP pcs receive path data delay MSBs (address 9206h)

Bit	Symbol	Access	Value	Description
15:0	RX_MAX_DELAY_MSB	R	0h	Maximum PCS receive path data delay in ns, upper

7.4.1.152 PTP_TS_RX_MIN_DELAY_LSB register

Table 208. PTP_TS_RX_MIN_DELAY_LSB register - Minimum PTP pcs receive path data delay MSBs (address 9207h)

Bit	Symbol	Access	Value	Description
15:0	RX_MIN_DELAY_LSB	R	0h	Minimum PCS receive path data delay in ns, lower

7.4.1.153 PTP_TS_RX_MIN_DELAY_MSB register

Table 209. PTP_TS_RX_MIN_DELAY_MSB register - Minimum PTP pcs receive path data delay MSBs (address 9208h)

Bit	Symbol	Access	Value	Description
15:0	RX_MIN_DELAY_MSB	R	0h	Minimum PCS receive path data delay in ns, Upper

7.4.1.154 PORT_BIST_CONTROL register

Table 210. PORT_BIST_CONTROL register - Port BIST control (address A800h)

Bit	Symbol	Access	Value	Description
15	RESET	RW	0h	Reset This bit is self-clearing.
14	CONFIG_ENABLE	RW	0h	If set BIST configuration can be changed. Otherwise the BIST configuration is write protected.
13:0	*reserved*	RW	0h	Always write all 0s, ignore on read.

7.4.1.155 BIST_INTERCEPT_CONFIG register

Table 211. BIST_INTERCEPT_CONFIG register - BIST intercept config (address A807h)

Bit	Symbol	Access	Value	Description
15:12	*reserved*	RW	0h	Always write 0000, ignore on read.

Table 211. BIST_INTERCEPT_CONFIG register - BIST intercept config (address A807h)*...continued*

Bit	Symbol	Access	Value	Description
11	CHECK_EPHY_OR_XMII	RW	0h	If set, EPHY received data to PORT BIST RXD This setting is configuration protected.
10:6	*reserved*	R	0h	Always write all 0s, ignore on read.
5:4	TX_INTERCEPT	RW		TX intercept This setting is configuration protected.
			00*	Normal operation(Default)
			10	Intercept EPHY TXD-path with PORT BIST TXD
			others	Reserved
3:2	*reserved*	R	0h	Always write 00, ignore on read.
1:0	RX_INTERCEPT	RW		RX intercept This setting is configuration protected.
			00*	Normal operation(Default)
			10	Intercept XMII RXD-path with PORT BIST TXD
			others	Reserved

7.4.1.156 BIST_GEN_CTRL register

Table 212. BIST_GEN_CTRL register - BIST generator control register (address A880h)

Bit	Symbol	Access	Value	Description
15	*reserved*	R	0h	Always write 0, ignore on read.
14	BIST_GEN_EN	RW	0h	If set, BIST generator is enabled
13	BIST_GEN_MODE	RW		Controls whether BIST is operating in continuous mode or production mode.
			0*	Production mode. BIST generator generates number of programmed good frame and number of programmed bad frames.
			1	BIST generator continuously generate good frames only. Hence, GOOD_FRAMES_PLAN and BAD_FRAMES_PLAN are ignored.
12	STOP	RW	0h	STOP control. Stop generating new frames after the currently generated one has completed. This is self-clearing bit.
11:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.157 BIST_GEN_STATUS register

Table 213. BIST_GEN_STATUS register - BIST generator status (address A881h)

Bit	Symbol	Access	Value	Description
15	BIST_GEN_DONE	R	0h	This status flag is set when programmed number of good frame and bad frame are completely generated and sent. This bit will not get asserted when continuous mode is enabled.
14:0	*reserved*	R	0h	Ignore on read.

7.4.1.158 PREAMBLE_IPG_SIZE register

Table 214. PREAMBLE_IPG_SIZE register - Preamble and IPG lengths (address A887h)

Bit	Symbol	Access	Value	Description
15:12	PREAMBLE_ LENGTH	RW	7h	Length of preamble in bytes.
11:10	*reserved*	R	0h	Always write all 0s, ignore on read.
9:8	IPG_LENGTH_ TYPE	RW		Selection of type of IPG length
			0*	IPG length is fixed to IPG_LENGTH
			1	IPG length starts with IPG_LENGTH bytes, incrementing by one every next IPG until 255 is reached. The IPG length rolls-over to IPG_LENGTH bytes after reaching an IPG length of 255 bytes, and starts incrementing from there again.
			2h	IPG length is determined by an 8-bit LFSR. If the LFSR value is less than IPG_LENGTH, then IPG length would be IPG_ LENGTH. If the LFSR value is greater than or equal to IPG_ LENGTH, then IPG length would be the LFSR value. IPG_ LENGTH also acts as seed for the 8-bit LFSR.
7:0	IPG_LENGTH	RW	Ch	Defines minimum length of IPG in bytes and maximum length is decided by an 8-bit LFSR. If the LFSR value is less than IPG_LENGTH, then IPG length would be IPG_LENGTH. If the LFSR value is greater than or equal to IPG_LENGTH, then IPG length would be LFSR value. IPG_LENGTH also acts as seed for the LFSR.

7.4.1.159 BIST_DA_0 register

Table 215. BIST_DA_0 register - lower 16 bits of DA value[15:0] (address A888h)

Bit	Symbol	Access	Value	Description
15:0	BIST_DA_0	RW	0h	[15:0] of DA

7.4.1.160 BIST_DA_1 register

Table 216. BIST_DA_1 register - middle 16 bits of DA value[31:16] (address A889h)

Bit	Symbol	Access	Value	Description
15:0	BIST_DA_1	RW	0h	[31:16] of DA

7.4.1.161 BIST_DA_2 register

Table 217. BIST_DA_2 register - higher 16 bits of DA value[47:32] (address A88Ah)

Bit	Symbol	Access	Value	Description
15:0	BIST_DA_2	RW	0h	[47:32] of DA

7.4.1.162 BIST_SA_0 register

Table 218. BIST_SA_0 register - lower 16 bits of SA value[15:0] (address A88Bh)

Bit	Symbol	Access	Value	Description
15:0	BIST_SA_0	RW	0h	[15:0] of SA

7.4.1.163 BIST_SA_1 register

Table 219. BIST_SA_1 register - middle 16 bits of SA value[31:16] (address A88Ch)

Bit	Symbol	Access	Value	Description
15:0	BIST_SA_1	RW	0h	[31:16] of SA

7.4.1.164 BIST_SA_2 register

Table 220. BIST_SA_2 register - higher 16 bits of SA value[47:32] (address A88Dh)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:0	BIST_SA_2	RW	0h	[47:32] of SA

7.4.1.165 BIST_PTP_CONFIG register

Table 221. BIST_PTP_CONFIG register - PTP frame generation configuration (address A88Fh)

Bit	Symbol	Access	Value	Description
15:8	PTP_MSG_ INTERVAL	RW	0h	Configures the interval of ptp event message to be transmitted. For every programmed N frame, one PTP event frame is generated. (N = PTP_MSG_INTERVAL). For ex: for every 10 frames, 9 normal frames are sent and 1 ptp frame is sent. 16'h88F7 is sent as ether type during ptp frame.
7:4	*reserved*	R	0h	Always write 0000, ignore on read.
3:0	PTP_MSG_TYPE	RW	0h	PTP message type as per IEEE 1588 PTP header. This configuration enables flexibility of selecting ptp message type. When all condition is met to send PTP frame over Ethernet frame, PTP_MSG_TYPE replaces the first nibble of selected data(constant data/incremental pattern/prbs data) after ether type is sent. PTP frame generation enables basic functional checks of PTP IP and to exercise PTP IP esp. for HTOL testing.

7.4.1.166 BIST_ETHER_TYPE register

Table 222. BIST_ETHER_TYPE register - Ethernet type (T/L) (address A890h)

Bit	Symbol	Access	Value	Description
15:0	ETHER_TYPE	RW	0h	Ethernet type (T/L).

7.4.1.167 PAYLOAD_CONFIG register

Table 223. PAYLOAD_CONFIG register - Payload data controls (address A891h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:14	*reserved*	R	0h	Always write 00, ignore on read.
13:12	PAYLOAD_DATA_TYPE	RW		Payload data type
			0h	Programmable fixed data is sent
			1h	Ramp data is sent (increment by 1)
			2h*	PRBS output is sent (see BIST_PRBS_SELECT)
			3h	Not used
11:10	*reserved*	R	0h	Always write 00, ignore on read.
9:8	PAYLOAD_SIZE_TYPE	RW		Indicates the increment in payload size.
			0h*	No increment in payload size (Always PAYLOAD_SIZE)
			1h	Increment always from PAYLOAD_SIZE[7:0] until {PAYLOAD_SIZE[13:8], 8'hFF} and rolls-over to PAYLOAD_SIZE[7:0] again. The limit is between PAYLOAD_SIZE[7:0] & {PAYLOAD_SIZE[13:8], 8'hFF} – where PAYLOAD_SIZE is programmable
			2h	For PAYLOAD_SIZE_TYPE= '10'=RANDOM, the payload data length is determined by a 14-bit LFSR (x^14+x^13+x^12+x^2+1). PAYLOAD_SIZE is used as seed. PAYLOAD_SIZE[7:0] sets the minimum payload size. PAYLOAD[13:8] determined the maximum payload size. If LFSR[13:8} =< PAYLOAD_SIZE[13:8], the LFSR[13:0] value determines the payload size. If LFSR[13:8}> PAYLOAD_SIZE[13:8], the payload size is determined by LFSR[9:0]. For PAYLOAD_SIZE[13:8] =05h, the max payload size is 1535 bytes (5FFh). The number of payload data bytes equals PAYLOAD_SIZE[7:0] if LFSR[13:0]<={00h & PAYLOAD_SIZE[7:0]}. This generates frames with a pseudo-random payload size ranging from PAYLOAD_SIZE[7:0] to {PAYLOAD_SIZE[13:8] & FFh} bytes. If PAYLOAD_SIZE[13:8]>05h, jumbo frames will be generated. Jumbo frames up to the max size of 16383 bytes will be generated if PAYLOAD_SIZE[13:8]=3Fh. PAYLOAD_SIZE is used as seed for 14-bit LFSR which is used to derive random payload length.
			3h	Not used
7:0	FIXED_PAYLOAD_DATA	RW	A5h	Byte value that will repeatedly send as frame payload.

7.4.1.168 PAYLOAD_SIZE register

Table 224. PAYLOAD_SIZE register - Length of frame payload data in bytes (address A892h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:14	*reserved*	R	0h	Always write 00, ignore on read.

Table 224. PAYLOAD_SIZE register - Length of frame payload data in bytes (address A892h) *...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
13:0	PAYLOAD_SIZE	RW	2Eh	Maximum of 1500d = 5DCh according to Ethernet standard and 9216d = 2400h for jumbo-frames. This 14-bit field allows a payload of up to 3FFFh = 16383 payload bytes to be sent in a frame. The minimum number of payload data bytes for Ethernet is 46d = 2Eh. If a value smaller than 2Eh is programmed the generator will work, but runt frames will be generated. The usage of this field depends on PAYLOAD_SIZE_TYPE: PAYLOAD_SIZE_TYPE=FIXED: this field sets a fixed payload size. PAYLOAD_SIZE_TYPE=INCREMENT or RANDOM: bits[7:0] determine the minimum payload size, and bits[13:8] determine the maximum payload size.

7.4.1.169 PRBS_DATA_CONFIG register

Table 225. PRBS_DATA_CONFIG register - PRBS data configuration (address A893h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:13	BIST_PRBS_SELECT	RW		Different type of PRBS is selected
			0h*	PRBS7
			1h	PRBS9
			2h	PRBS11
			3h	PRBS15
			4h	Not used all other conditions
12	*reserved*	R	0h	Always write 0, ignore on read.
11	LFSR_SEED_USAGE	RW		This bit selects the seed value of the LFSR.
			0*	The seed of the LFSR returns to the programmed value for every packet. Seed value is taken from BIST_LFSR_SEED register
			1	First generated ethernet frame uses the programmed seed, and the seed keeps progressing for next frames.
10:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.170 BIST_LFSR_SEED register

Table 226. BIST_LFSR_SEED register - LFSR Seed value (address A894h)

Bit	Symbol	Access	Value	Description
15	*reserved*	R	0h	Always write 0, ignore on read.
14:0	BIST_LFSR_SEED	RW	7FFFh	Initial value to be loaded into the LSFR for PRBS data.

7.4.1.171 GOOD_FRAMES_PLAN register

Table 227. GOOD_FRAMES_PLAN register - Number of good frames to be generated by BIST generator (address A8A2h)

Bit	Symbol	Access	Value	Description
15:0	GOOD_FRAMES_PLAN	RW	64h	Number of good frames to be generated by BIST generator.

7.4.1.172 G_GOOD_FRAME_CNT register

Table 228. G_GOOD_FRAME_CNT register - Generated good frames in continuous mode. (address A8A4h)

Bit	Symbol	Access	Value	Description
15:0	G_GOOD_FRAME_CNT	R	0h	Number of generated 'good frames' with a correct FCS value. This register stores the number of generated good frames when the packet generator is stopped by the STOP bit. This register wraps on overflow. In production mode, this register counts all frames (good and bad).

7.4.1.173 BAD_FRAMES_PLAN register

Table 229. BAD_FRAMES_PLAN register - Number of bad frames to be generated by BIST generator (address A8A6h)

Bit	Symbol	Access	Value	Description
15:0	BAD_FRAMES_PLAN	RW	0h	Number of bad frames to be generated by BIST generator

7.4.1.174 BIST_CHECK_CTRL register

Table 230. BIST_CHECK_CTRL register - BIST checker control register (address A8C0h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	*reserved*	R	0h	Always write 0, ignore on read.
14	BIST_CHECKER_EN	RW		BIST checker enable
			0*	BIST checker is disabled
			1	BIST checker is enabled
13	STATISTIC_CNT_RST	RW	0h	If this bit is set, status bits are reset – BIST_STATUS, GOOD_FRAME_CNT, BAD_FRAME_CNT. This bit resets good frame counter, bad frame counter and rx_er (TJF1103B only) detected frame counter. After reset, all status registers hold fresh values. This bit is self-clearing[1]. This bit is used only when BIST is in continuous mode.
12:1	*reserved*	R	0h	Always write all 0s, ignore on read.
0	BIST_CHECK_MODE	RW		Controls whether BIST is operating in continuous mode or production mode.
			0*	Production mode. BIST checker checks for BIST done and BIST fail status.

Table 230. BIST_CHECK_CTRL register - BIST checker control register (address A8C0h)*...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
			1	Continuous mode. BIST checker keeps checking the good frames, bad frames and rx_er when rx_dv is set. Results are available in statistical registers.

[1] For TJF1103A: this is does not set the rx_er counter.

7.4.1.175 BIST_PROD_STATUS register

Table 231. BIST_PROD_STATUS register - BIST status used when BIST is in production mode and NOT valid for continuous mode (address A8C1h)

Bit	Symbol	Access	Value	Description
15	BIST_CHECK_DONE	R	0h	This bit indicates BIST status is ready for reading. This bit is set when expected good number of frames and bad number of frames is received or timed out.
14:5	*reserved*	R	0h	Ignore on read.
4	BIST_CHECK_FAIL	R	0h	Indicates at least one of the following errors was detected: 1. Good frame error: If the expected number of good frames are not received, then bit flag is set. 2. Bad frame error: If the expected number of bad frames are not received, then bit flag is set (Error is injected, but not received) 3. rx_dv is not detected: If RX_DV is not received by the BIST checker, then this status is set. 4. RX_ER detected: This status is set when rx_er is set with rx_dv is high If BIST_CHECK_DONE is set and BIST_CHECK_FAIL is logic zero, then it is said to be PASSED. If BIST_CHECK_DONE is set and BIST_CHECK_FAIL is logic high, then it is said to be FAIL.
3	RX_ER_DETECT_ER	R	0h	This status is set when rx_er is set with rx_dv is high
2	RXDV_DETECT_ER	R	0h	If RX_DV is not received by the BIST checker, then this status is set.
1	BAD_FRAME_ERROR	R	0h	If the expected number of bad frames are not received, then bit flag is set.
0	GOOD_FRAME_ERROR	R	0h	If the expected number of good frames are not received, then bit flag is set

7.4.1.176 BIST_WAIT_TIMER register

Table 232. BIST_WAIT_TIMER register - Timer timeout value for checking all status in production mode (address A8C4h)[1]

Bit	Symbol	Access	Value	Description
15:0	BIST_WAIT_TIMER	RW	FFh	Timer timeout value for checking all status in production mode. This count begins when the BIST checker is enabled. Hence this register should be programed before the BIST checker is enabled.

Table 232. BIST_WAIT_TIMER register - Timer timeout value for checking all status in production mode (address A8C4h)[1]

Bit	Symbol	Access	Value	Description
				Ideally this value should be the time taken by the BIST generator to send all frames plus latency from BIST generator to BIST checker plus additional time to program BIST generator and checker enable bit. This is time out register and is useful when expected good number of frames and bad number of frames is not received. In this condition, time out asserts BIST_CHECK_DONE status. This count is in terms of microseconds. Note: This is a 16-bit value; so only up to 65 ms supported.

[1] This timeout is useful when expected number of generated frames is never received.

7.4.1.177 R_GOOD_FRAME_CNT register

Table 233. R_GOOD_FRAME_CNT register - Received good frame count (address A8D0h)

Bit	Symbol	Access	Value	Description
15:0	R_GOOD_FRAME_CNT	R	0h	Counts the number received frames for which CRC magic number is matched. This can be used in both production mode and continuous mode. This counter can be reset by programmable bit to count fresh good frame (in continuous mode).

7.4.1.178 R_BAD_FRAME_CNT register

Table 234. R_BAD_FRAME_CNT register - Received bad frame count (address A8D2h)

Bit	Symbol	Access	Value	Description
15:0	R_BAD_FRAME_CNT	R	0h	Counts the number received frames for which CRC magic number is NOT matched. This can be used in both production mode and continuous mode. This counter can be reset by programmable bit to count fresh bad frame (in continuous mode)

7.4.1.179 R_RXER_FRAME_CNT register

Table 235. R_RXER_FRAME_CNT register - RX_ER detected when rx_dv is set. (address A8D4h)

Bit	Symbol	Access	Value	Description
15:0	R_RXER_FRAME_CNT	R	0h	Counts the number received frames for which rx_er is detected when rx_dv is high. This can be used in both production mode and continuous mode. This counter can be reset by programmable bit to count fresh bad frame (in continuous mode).

7.4.1.180 PORT_INFRA_CONTROL register

Table 236. PORT_INFRA_CONTROL register - Port infrastructure control (address AC00h)

Bit	Symbol	Access	Value	Description
15	RESET	RW	0h	Resets CMOS xMII. Registers which are set by pin strap values, are set to what was latched during the initial pin strap sequence. This bit is self-clearing.
14	CONFIG_ENABLE	RW	0h	If set, the infrastructure configuration can be changed. Otherwise writes are ignored.
13:0	*reserved*	RW	0h	Always write all 0s, ignore on read.

7.4.1.181 INFRA_ABILITY register

Table 237. INFRA_ABILITY register - Infrastsructure ability (address AC04h)

Bit	Symbol	Access	Value	Description
15	XMII_ABILITY	R	1h	InfraStruture xMII Ability
14:0	*reserved*	R	0h	Ignore on read.

7.4.1.182 INFRA_CONFIG register

Table 238. INFRA_CONFIG register - Infrastructure configuration (address AC06h)

Bit	Symbol	Access	Value	Description
15:1	*reserved*	R	0h	Always write all 0s, ignore on read.
0	TEST_ENABLE	RW	0h	If enabled, Infrasstructure related test modes can be enabled This setting is configuration protected.

7.4.1.183 INFRA_IRQ_SOURCE register

Table 239. INFRA_IRQ_SOURCE register - Infrastructure IRQ sources (address AC08h)

Bit	Symbol	Access	Value	Description
15	*reserved*	R	0h	Always write 0, ignore on read.
14	FIFO_ERROR	RW	0h	If set, elastic FIFO underflow or overflow. Write one to clear. This bit is latched-high.
13	RGMII_ID_LOCK_ERROR	RW	0h	If set, Lock-error of internal delay(s) of RGMII. Write one to clear. This bit is latched-high.
12:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.184 INFRA_IRQ_ENABLE register

Table 240. INFRA_IRQ_ENABLE register - Infrastructure IRQ enables (address AC0Ah)

Bit	Symbol	Access	Value	Description
15	*reserved*	R	0h	Always write 0, ignore on read.
14	FIFO_ERROR	RW	0h	If set, the respective IRQ is enabled

Table 240. INFRA_IRQ_ENABLE register - Infrastructure IRQ enables (address AC0Ah)*...continued*

Bit	Symbol	Access	Value	Description
				This setting is preserved during deep sleep.
13	RGMII_ID_LOCK_ERROR	RW	0h	If set, the respective IRQ is enabled This setting is preserved during deep sleep.
12:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.185 INFRA_IRQ_MSTATUS register

Table 241. INFRA_IRQ_MSTATUS register - Infrastructure IRQ masked status (address AC0Ch)

Bit	Symbol	Access	Value	Description
15	*reserved*	R	0h	Ignore on read.
14	FIFO_ERROR	R	0h	Masked status of the respective interrupt
13	RGMII_ID_LOCK_ERROR	R	0h	Masked status of the respective interrupt
12:0	*reserved*	R	0h	Ignore on read.

7.4.1.186 XMII_CONTROL register

Table 242. XMII_CONTROL register - XMII control (address AFC0h)

Bit	Symbol	Access	Value	Description
15	RESET	RW	0h	Reset xMII block. Reloads all OTP configuration and reads pin strapping settings This bit is self-clearing.
14:2	*reserved*	R	0h	Always write all 0s, ignore on read.
1	MAC_LOOPBACK	RW	0h	If set, data received on external xMII port is looped on internal (G)MII, and re-transmitted on external xMII port. This setting is test protected.
0	PHY_LOOPBACK	RW	0h	If set, data received on internal (G)MII is looped on xMII, and re-transmitted on internal (G)MII. This setting is test protected.

7.4.1.187 XMII_STATUS register

Table 243. XMII_STATUS register - XMII status (address AFC2h)

Bit	Symbol	Access	Value	Description
15	TXD_FIFO_OVERFLOW	RW	0h	If set, Overflow of transmit path FIFO Write one to clear. This bit is latched-high.
14	TXD_FIFO_UNDERFLOW	RW	0h	If set, Underflow of transmit path FIFO Write one to clear. This bit is latched-high.
13	RXD_FIFO_OVERFLOW	RW	0h	If set, Overflow of receive path FIFO Write one to clear. This bit is latched-high.

Table 243. XMII_STATUS register - XMII status (address AFC2h)*...continued*

Bit	Symbol	Access	Value	Description
12	RXD_FIFO_ UNDERFLOW	RW	0h	If set, Underflow of receive path FIFO Write one to clear. This bit is latched-high.
11	RGMII_TXID_ LOCK_ERROR	RW	0h	If set, Lock-error of integrated delay in TXC Write one to clear. This bit is latched-high.
10	RGMII_RXID_ LOCK_ERROR	RW	0h	If set, Lock-error of integrated delay in RXC Write one to clear. This bit is latched-high.
9:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.188 XMII_ABILITIES register

Table 244. XMII_ABILITIES register - XMII abilities (address AFC4h)

Bit	Symbol	Access	Value	Description
15	RGMII_ID_ABILITY	R	TJF1103A: 1h TJF1103B: 0h	If set, Ability to add Internal Delay in RXC/TXC clock signals for RGMII This setting is preserved during deep sleep.
14	RGMII_ABILITY	R	TJF1103A: 1h TJF1103B: 0h	If set, Ability to support RGMII for this PORT This setting is preserved during deep sleep.
13:12	*reserved*	R	0h	Ignore on read.
11	RMII_LEADER_ ABILITY	R	TJF1103A: 1h TJF1103B: 0h	If set, Ability to support RMII with clock output (MAC-leader) for this PORT This setting is preserved during deep sleep.
10	RMII_FOLLOWER_ ABILITY	R	TJF1103A: 1h TJF1103B: 0h	If set, Ability to support RMII with clock input (PHY or MAC-follower) for this PORT This setting is preserved during deep sleep.
9	MII_FOLLOWER_ ABILITY	R	TJF1103A: 1h TJF1103B: 0h	If set, Ability to support MII with clock input (clock-follower, MAC-mode) for this PORT This setting is preserved during deep sleep.
8	MII_LEADER_ ABILITY	R	TJF1103A: 1h TJF1103B: 0h	If set, Ability to support MII with clock outputs (clock-leader, PHY-mode) for this PORT This setting is preserved during deep sleep.
7:1	*reserved*	R	0h	Ignore on read
0	SGMII_ABILITY	R	TJF1103A: 0h TJF1103B: 1h	If set, SGMII is available on this port.

7.4.1.189 SERDES_MII_ABILITIES register

Table 245. SERDES_MII_ABILITIES register - SERDES MII abilities (address AFC5h)

Bit	Symbol	Access	Value	Description
15:2	*reserved*	R	0h	Ignore on read.
1	SGMII_ABILITY	R	TJF1103A: 0h TJF1103B: 1h	If set, SGMII is available on this PORT This setting is preserved during deep sleep.

Table 245. SERDES_MII_ABILITIES register - SERDES MII abilities (address AFC5h)*...continued*

Bit	Symbol	Access	Value	Description
0	*reserved*	R	0h	Ignore on read.

7.4.1.190 MII_BASIC_CONFIG register

Table 246. MII_BASIC_CONFIG register - MII basic configuration (address AFC6h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:9	*reserved*	R	0h	Always write all 0s, ignore on read.
8	JUMBO_EN	RW	0h	If set, enable support for jumbo packets (16K) This setting is configuration protected.
7:5	*reserved*	RW	0h	Always write 000, ignore on read.
4	ROLE	RW	0h	If set, the device will operate in 'reverse' role mode. If XMII_MODE is set to MII, and ROLE is set, the device operates in revMII mode (TXCLK and RXCLK are input). If XMII_MODE is set to RMII, and ROLE is set, the device operates in revRMII mode (REF_CLK is output). This setting is preserved during deep sleep. This setting is configuration protected. TJF1103B: if set, SGMII operates in MAC mode; otherwise PHY mode
3	CMOS_OR_SERDES	R		CMOS or SERDES
			0*	CMOS
			1	SERDES
2:0	XMII_MODE	RW		The value of the fields CMOS_OR_SERDES, XMII_MODE determine the XMII mode of operation. All possible mode encodings are listed below (concatenated bits MOS_OR_SERDES, XMII_MODE). This setting is preserved during deep sleep. This setting is configuration protected. All possible mode settings are listed in Table 4 and Table 5; do not write undefined values.
			100	MII
			101	RMII
			111	RGMII
			000	SGMII
			others	reserved

7.4.1.191 XMII_CLK_CONFIG register

Table 247. XMII_CLK_CONFIG register - XMII clock configuration (address AFC8h)

Bit	Symbol	Access	Value	Description
15	*reserved*	RW	0h	Always write 0, ignore on read.
14	CLOCK_DISABLE	RW	0h	If set, xMII clock output(s) disabled

Table 247. XMII_CLK_CONFIG register - XMII clock configuration (address AFC8h)*...continued*

Bit	Symbol	Access	Value	Description
				This setting is configuration protected.
13:12	*reserved*	R	0h	Always write 00, ignore on read.
11	RMII_CLK_REF	RW	0h	If RMII and ROLE=1, the output clock signal is synchronous with the device REF_CLK input (XTAL or externally provided reference clock) If set, If RMII and and ROLE=1, the input clock signal is also used as clock reference for the transceiver. If RMII in MAC-mode, the output clock signal is synchronous with transceiver communication (PHY-locked) This setting is preserved during deep sleep. This setting is configuration protected.
10:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.4.1.192 XMII_CLK_IO_CONFIG register

Table 248. XMII_CLK_IO_CONFIG register - XMII CLK IO configuration (address AFC9h)

Bit	Symbol	Access	Value	Description
15	MANUAL_CONFIG	RW	0h	If set, SLEW_RATE and DRIVE_STRENGTH are used to set the xMII clock output IO configuration. Otherwise default values are used. Caution: a manual override may violate the xMII timing in some or all operating conditions. The timing values in the dynamic characteristics section of the data sheet are valid under default or ALTERNATE=1 settings, only. This setting is configuration protected.
14:11	*reserved*	RW	0h	Always write 0000, ignore on read.
10:8	DRIVE_STRENGTH	RW	0h	Select drive strength selection This setting is configuration protected.
7:3	*reserved*	RW	0h	Always write 00000, ignore on read.
2:0	SLEW_RATE	RW	0h	Select slew rate selection 0 = weakest 7 = strongest This setting is configuration protected.

7.4.1.193 XMII_DATA_CONFIG register

Table 249. XMII_DATA_CONFIG register - XMII data configuration (address AFCAh)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	*reserved*	RW	0h	Always write 0, ignore on read.
14	TXD30_SWAP	RW	0h	TXD swap. If set, the TXD nibble is reversed to TXD[0:3] This setting is preserved during deep sleep. This setting is configuration protected.
13:11	*reserved*	R	0h	Always write all 000, ignore on read.
10	TXER_GPIO_SWAP	RW		Controls TX_ER pin function

Table 249. XMII_DATA_CONFIG register - XMII data configuration (address AFCAh)*...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
				This setting is configuration protected.
			0*	classic TX_ER functionality
			1	TX_ER is available as GPIO9
9:8	*reserved*	RW	0h	Always write 00, ignore on read.
7	RXD_DISABLE	RW	0h	If set, RXD and XMII RXCTL,RXER outputs drive a low value except RXC This setting is configuration protected.
6	*reserved*	R	0h	Always write 0, ignore on read.
5:4	RXCTL_SELECT	RW		Alternate RXCTL selection This setting is preserved during deep sleep. This setting is configuration protected.
			00*	Default RXCTL pin position. RXCTL next to RXC
			11	Alternate RXCTL position. RXCTL at other side of RXD[3:0]
			others	Reserved
3	*reserved*	R	0h	Always write 0, ignore on read.
2	RXER_GPIO_SWAP	RW		Controls RX_ER pin function This setting is configuration protected.
			0*	classic RX_ER functionality
			1	RX_ER pin is available as GPIO 2
1:0	*reserved*	RW	0h	Always write 00, ignore on read.

7.4.1.194 XMII_DATA_IO_CONFIG register

Table 250. XMII_DATA_IO_CONFIG register - XMII Data IO configuration (address AFCBh)

Bit	Symbol	Access	Value	Description
15	MANUAL_CONFIG	RW	0h	If set, SLEW_RATE and DRIVE_STRENGTH are used to set the xMII data output IO configuration. Otherwise default values are used. Caution: a manual override may violate the xMII timing in some or all operating conditions. The timing values in the dynamic characteristics section of the datasheet are valid under default or ALTERNATE=1 settings, only. This setting is configuration protected.
14	ALTERNATE_ CONFIG	RW	0h	If set, reduced emission selection for XMII data and clock pads (up to 15 pF load) This setting is configuration protected.
13:11	*reserved*	RW	0h	Always write 000, ignore on read.
10:8	DRIVE_STRENGTH	RW	0h	Select drive strength of DATA output IO cells used for the configured CMOS xMII mode This setting is configuration protected.
7:3	*reserved*	RW	0h	Always write 00000, ignore on read.

Table 250. XMII_DATA_IO_CONFIG register - XMII Data IO configuration (address AFCBh)*...continued*

Bit	Symbol	Access	Value	Description
2:0	SLEW_RATE	RW	0h	Select slew rate of IOs configured for CMOS xMII mode. 0 = weakest 7 = strongest This setting is configuration protected.

7.4.1.195 RGMII_TXC_DELAY_CONFIG register

Table 251. RGMII_TXC_DELAY_CONFIG register - RGMII TXC delay configuration (address AFCCh)

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	0h	If set, internal TXC delay enabled This setting is preserved during deep sleep. This setting is configuration protected.
14:5	*reserved*	R	0h	Always write all 0s, ignore on read.
4:0	PHASE_SHIFT	RW	12h	The Phase shift or Internal delay is as per below equation Phase-shift = 73.8 + 0.9*PHASE_SHIFT[4:0] degrees This setting is preserved during deep sleep. This setting is configuration protected.

7.4.1.196 RGMII_RXC_DELAY_CONFIG register

Table 252. RGMII_RXC_DELAY_CONFIG register - RGMII RXC delay configuration (address AFCDh)

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	0h	If set, internal RXC delay enabled This setting is preserved during deep sleep. This setting is configuration protected.
14:5	*reserved*	R	0h	Always write all 0s, ignore on read.
4:0	PHASE_SHIFT	RW	12h	The Phase shift or Internal delay is as per below equation Phase-shift = 73.8 + 0.9*PHASE_SHIFT[4:0] degrees This setting is preserved during deep sleep. This setting is configuration protected.

7.4.1.197 RX_PREAMBLE_COUNT register

Table 253. RX_PREAMBLE_COUNT register - RX preamble counter (address AFCEh)

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	0h	Enable for capturing RX Preamble Count This setting is configuration protected.
14:6	*reserved*	R	0h	Always write all 0s, ignore on read.
5:0	COUNT	R	0h	Captures Lowest Preamble count on receive side of the PHY's PCS interface. If read, the counter gets cleared, and again starts looking for lowest preamble count. The count is in terms of number of nibbles for 100Base-T1 This flag is cleared on read.

7.4.1.198 TX_PREAMBLE_COUNT register

Table 254. TX_PREAMBLE_COUNT register - TX preamble counter (address AFCFh)

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	0h	Enable for capturing TX Preamble Count This setting is configuration protected.
14:6	*reserved*	R	0h	Always write all 0s, ignore on read.
5:0	COUNT	R	0h	Captures Lowest Preamble count on transmit side of the PHY's PCS interface. If read, the counter gets cleared, and again starts looking for lowest preamble count. The count is in terms of number of nibbles for 100Base-T1 This flag is cleared on read.

7.4.1.199 RX_IPG_LENGTH register

Table 255. RX_IPG_LENGTH register - RX IPG length capture (address AFD0h)

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	0h	Enable for capturing RX IPG Length This setting is configuration protected.
14:9	*reserved*	R	0h	Always write all 0s, ignore on read.
8:0	LENGTH	R	0h	Captures Lowest IPG Length on receive side of the PHY's PCS interface. If read, the IPG length gets cleared, and again starts looking for lowest IPG length. The length is reported in multiple of 4bits. This flag is cleared on read.

7.4.1.200 TX_IPG_LENGTH register

Table 256. TX_IPG_LENGTH register - TX IPG length capture (address AFD1h)

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	0h	Enable for capturing TX IPG Length This setting is configuration protected.
14:9	*reserved*	R	0h	Always write all 0s, ignore on read.
8:0	LENGTH	R	0h	Captures Lowest IPG Length on transmit side of the PHY's PCS interface. If read, the IPG length gets cleared, and again starts looking for lowest IPG Length. The length is in terms of The length is reported in multiple of 4bits. This flag is cleared on read.

7.4.1.201 SGMII_BASIC_CONTROL register

Table 257. SGMII_BASIC_CONTROL register - SGMII PCS register (address B000h)

Bit	Symbol	Access	Value	Description
15	RST	RW	0h	Soft Reset.

Table 257. SGMII_BASIC_CONTROL register - SGMII PCS register (address B000h)*...continued*

Bit	Symbol	Access	Value	Description
				When the host sets this bit, this triggers the software reset process in which all internal blocks are reset, except the APB interface block. The registers are reset to their default values. When this bit is set, it also resets the PMA & PMD. This bit is self-cleared after 32 clock cycles of the APB bus clock. Type: Self Clearing.
14	LBE	RW	0h	Not used
13	SS13	RW	1h	Speed Selection (LSB). This bit, along with the SS6 bit of this register, indicates the speed. • SS6 SS13 -> Speed • 1 0 -> 1000 Mbps • 0 1 -> 100 Mbps • 0 0 -> 10 Mbps
12	AN_ENABLE	RW	1h	Enable Auto-Negotiation. When set to 1, this bit enables the Clause 37 auto-negotiation process.
11	LPM	RW	0h	Power-Down Mode. This bit controls the powerdown mode of the PCS. • 0: Normal operation • 1: The PCS goes to the powerdown mode When the host clears this bit, the PCS resumes the normal operation.
10	*reserved*	R	0h	Always write 0, ignore on read.
9	RESTART_AN	RW	0h	Restart Auto-Negotiation. When the host writes this bit, the PCS initiates the auto-negotiation process. This bit is used to restart the auto-negotiation which is already initiated by setting AN_ENABLE. The PCS clears this bit after restarting the autonegotiation. Type: Self Clearing.
8	DUPLEX_MODE	RW	0h	Duplex Mode. This bit specifies the duplex mode of the PCS. • 0: Half duplex • 1: Full duplex If AN_ENABLE is set to 0, this bit determines the PHY link duplex mode. If AN_ENABLE is set to 1, then the PHY link duplex mode is independent of this bit (although the host can write any value) and is determined by the outcome of the Clause 37 auto-negotiation process. Note that only full duplex mode is supported.
7	*reserved*	R	0h	Always write 0, ignore on read.
6	SS6	RW	0h	Speed Selection (MSB). This bit, along with the SS13 bit of this register, indicates the speed. For more information, see description of the SS13 bit.
5:0	*reserved*	R	0h	ignore on read.

7.4.1.202 SGMII_BASIC_STATUS register

Table 258. SGMII_BASIC_STATUS register - SGMII PCS register (address B001h)

Bit	Symbol	Access	Value	Description
15	ABL100T4	R	0h	100BASE-T4 Ability. Always returns 0 because this functionality is not supported.
14	FD100ABL	R	0h	100BASE-X Full-Duplex Ability. Always returns 0 because this functionality is not supported.
13	HD100ABL	R	0h	100BASE-X Half-Duplex Ability. Always returns 0 because this functionality is not supported.
12	FD10ABL	R	0h	10 Mbps Full-Duplex Ability. Always returns 0 because this functionality is not supported.
11	HD10ABL	R	0h	10 Mbps Half-Duplex Ability. Always returns 0 because this functionality is not supported.
10	FD100T	R	0h	100BASE-T2 Full-Duplex Ability. Always returns 0 because this functionality is not supported.
9	HD100T	R	0h	100BASE-T2 Half-Duplex Ability. Always returns 0 because this functionality is not supported.
8	EXT_STS_ABL	R	1h	Extended Status Information. • 0: No Extended Status information is present at register address 0x000F of this MMD device • 1: Extended Status information is present at register address 0x000F of this MMD device Always returns 1.
7	UN_DIR_ABL	R	0h	Unidirectional Ability. • 0: The PCS is able to transmit frames only when the device has determined the valid link • 1: The PCS is able to transmit frames irrespective of whether device has determined the valid link or not
6	*reserved*	R	0h	Ignore on read.
5	AN_CMPL	R	0h	Auto-negotiation Complete. • 0: The AN process is not completed • 1: The AN process is completed When this bit is set to 1, the contents of the AN MMD Advertizement, AN MMD Link partner Ability, and AN MMD Expansion registers are valid. This bit returns 0 if AN_ENABLE is set to 0.
4	RF	R	0h	Remote Fault. When set to 1, this bit indicates that the receive link of the link partner is down. This bit is set based on the auto-negotiated (1000BASE-X auto-negotiation) information from the link partner. • 0: The PCS did not detect a remote fault • 1: The PCS detected a remote fault Note that this bit is only valid when using 1000BASE-X auto-negotiation (PCS_MODE=0x0) because remote fault information is part of the exchanged base page. When using SGMII autonegotiation (PCS_MODE=0x2) this bit must be ignored since remote fault information is not exchanged.

Table 258. SGMII_BASIC_STATUS register - SGMII PCS register (address B001h)*...continued*

Bit	Symbol	Access	Value	Description
				Type: Latch High.
3	AN_ABL	R	1h	Auto-negotiation Ability. Always returns 1 because the PCS is able to perform auto-negotiation.
2	LINK_STS	R	0h	Link Status. When set to 1, it indicates that the Rx link is up. If the link goes down, it is latched until the host performs the read operation to this register. • 0: Link Down • 1: Link Up Type: Latch Low.
1	*reserved*	R	0h	Ignore on read.
0	EXT_REG_CAP	R	1h	Extended Register Capability. • 0: Extended Register capability does not exist • 1: Extended Register capability exists Always returns 1.

7.4.1.203 SGMII_SR_MII_DEV_ID1 register

Table 259. SGMII_SR_MII_DEV_ID1 register - SGMII PCS register (address B002h)

Bit	Symbol	Access	Value	Description
15:0	VS_MII_DEV_OUI_3_18	R	0h	Organizationally Unique Identifier[3:18]. This field contains Bits[18:3] of 24-bit OUI of device manufacturer.

7.4.1.204 SGMII_SR_MII_DEV_ID2 register

Table 260. SGMII_SR_MII_DEV_ID2 register - SGMII PCS register (address B003h)

Bit	Symbol	Access	Value	Description
15:10	VS_MMD_DEV_OUI_19_24	R	0h	Organizationally Unique Identifier[19:24]. This field contains Bits[24:19] of 24-bit OUI of device manufacturer.
9:4	VS_MMD_DEV_MMN_5_0	R	0h	Model Number. This field contains the 6-bit Model number of the device.
3:0	VS_MMD_DEV_RN_3_0	R	0h	Revision Number. This field contains the 4-bit Revision number of the device.

7.4.1.205 SGMII_AUTONEG_ADVERTISE register

Table 261. SGMII_AUTONEG_ADVERTISE register - SGMII PCS register (address B004h)

Bit	Symbol	Access	Value	Description
15	NP	R	0h	Next Page / SGMII Link Status. Always returns 0 when using 1000BASE-X auto-negotiation (PCS_MODE=0x0) because the Next Page feature is not supported.

Table 261. SGMII_AUTONEG_ADVERTISE register - SGMII PCS register (address B004h)*...continued*

Bit	Symbol	Access	Value	Description
				When using SGMII autonegotiation (PCS_MODE=0x2) Next Page information is not exchanged. Instead, in SGMII PHY mode (TX_CONFIG=1), this field is read-only and indicates the PHY's Link Status that is communicated (advertised) to the SGMII link partner, in line with the definition of the tx_config_Reg in the SGMII specification. The value that is advertised depends on the setting of PHY_MODE_CTRL and bit 4 (SGMII_LINK_STS) of SGMII_PCS_CONFIG2.
14	*reserved*	R	0h	Always write 0, ignore on read.
13:12	RF	RW	0h	Remote Fault / SGMII Duplex Mode. This field indicates the fault signaling of the local device to be communicated (advertised) to the link partner. • 00: No Error • 01: Offline • 10: Link Failure • 11: Auto-negotiation Error Note that this field is only valid when using 1000BASE-X auto-negotiation (PCS_MODE=0x0). When using SGMII autonegotiation (PCS_MODE=0x2) remote fault information is not exchanged. Instead, in SGMII PHY mode (TX_CONFIG=1), bit 12 is read-only and indicates the duplex mode of operation that is communicated (advertised) to the SGMII link partner, in line with the definition of the tx_config_Reg in the SGMII specification. The value that is advertised depends on the setting of PHY_MODE_CTRL and bit 5 (FD) of SGMII_AUTONEG_ADVERTISE. • 0: Half Duplex • 1: Full Duplex
11:9	*reserved*	R	0h	Always write 0, ignore on read.
8:7	PAUSE	RW	0h	Pause Ability. This field indicates the Pause ability of the local device to be communicated (advertised) to the link partner. Software can program suitable values based on the capability of the MAC. • 00: No Pause • 01: Asymmetric Pause towards the link partner • 10: Symmetric Pause • 11: Symmetric Pause and Asymmetric Pause towards the local device Note that this field is only valid when using 1000BASE-X auto-negotiation (PCS_MODE=0x0). When using SGMII autonegotiation (PCS_MODE=0x2) Pause Ability information is not exchanged.
6	HD	RW	0h	Half Duplex. When this bit is set, it indicates that the device can operate in the half-duplex mode. Note: Only valid when using 1000BASE-X auto-negotiation (PCS_MODE=0x0). When using SGMII autonegotiation (PCS_MODE=0x2) duplex information is not exchanged and this field must be ignored.

Table 261. SGMII_AUTONEG_ADVERTISE register - SGMII PCS register (address B004h)*...continued*

Bit	Symbol	Access	Value	Description
				Half-duplex operation is not supported at chip level.
5	FD	RW	1h	Full Duplex. When this bit is set, it indicates that the device can operate in the full-duplex mode. Note: Only valid when using 1000BASE-X auto-negotiation (PCS_MODE=0x0). When using SGMII autonegotiation (PCS_MODE=0x2) duplex information is not exchanged and this field must be ignored.
4:0	*reserved*	R	0h	Always write 0, ignore on read.

7.4.1.206 SGMII_AUTONEG_LP_ABILITY register

Table 262. SGMII_AUTONEG_LP_ABILITY register - SGMII PCS register (address B005h)

Bit	Symbol	Access	Value	Description
15	LP_NP	R	0h	Link Partner Next Page / Link Partner Link Status. This bit indicates that the link partner can handle Next Page. To exchange information through Next Page, both devices (local and remote) should have the capability to handle Next Page. The PCS does not support Next Page (see SGMII_AUTONEG_ADVERTISE.NP) therefore, the Next Page exchange does not happen. Note: Only valid when using 1000BASE-X auto-negotiation (PCS_MODE=0x0). When using SGMII autonegotiation (PCS_MODE=0x2) Next Page information is not exchanged and this field must be ignored. In SGMII auto-negotiation this field is used to indicate the Link Status of the SGMII link partner, in line with the definition of the tx_config_Reg in the SGMII specification.
14	LP_ACK	R	0h	Link Partner Acknowledge. ACK bit from the Link Partner. This bit indicates that the link partner has successfully received the page sent by the local device.
13:12	LP_RF	R	0h	Link Partner Remote Fault / Link Partner Duplex Mode. This field indicates the fault signaling of the link partner. • 00: No Error • 01: Offline • 10: Link Failure • 11: Auto-negotiation Error Note: Only valid when using 1000BASE-X auto-negotiation (PCS_MODE=0x0). When using SGMII autonegotiation (PCS_MODE=0x2) remote fault information is not exchanged and this field must be ignored. In SGMII auto-negotiation bit 12 of this field is used to indicate the duplex mode of operation of the SGMII link partner, in line with the definition of the tx_config_Reg in the SGMII specification.
11:9	*reserved*	R	0h	Ignore on read.
8:7	LP_PAUSE	R	0h	Link Partner Pause Ability. This field indicates the Pause ability of the link partner. • 00: No Pause

Table 262. SGMII_AUTONEG_LP_ABILITY register - SGMII PCS register (address B005h)*...continued*

Bit	Symbol	Access	Value	Description
				• 01: Asymmetric Pause towards the link partner • 10: Symmetric Pause • 11: Both Symmetric Pause and Asymmetric Pause towards the local device Note that this field is only valid when using 1000BASE-X auto-negotiation (PCS_MODE=0x0). When using SGMII autonegotiation (PCS_MODE=0x2) Pause Ability information is not exchanged.
6	LP_FD	R	0h	Link Partner Half Duplex. When this bit is set, it indicates that the link partner is capable of operating in the halfduplex mode. Note: Only valid when using 1000BASE-X auto-negotiation (PCS_MODE=0x0). When using SGMII autonegotiation (PCS_MODE=0x2) duplex information is not exchanged and this field must be ignored.
5	LP_HD	R	0h	Link Partner Full Duplex. When this bit is set, it indicates that the link partner is capable of operating in the full-duplex mode. Note: Only valid when using 1000BASE-X auto-negotiation (PCS_MODE=0x0). When using SGMII autonegotiation (PCS_MODE=0x2) duplex information is not exchanged and this field must be ignored.
4:0	*reserved*	R	0h	Always write 0, ignore on read.

7.4.1.207 SGMII_AUTONEG_EXPANSION register

Table 263. SGMII_AUTONEG_EXPANSION register - SGMII PCS register (address B006h)

Bit	Symbol	Access	Value	Description
15:3	*reserved*	R	0h	Ignore on read.
2	LD_NP_ABL	R	0h	Local Device Next Page Able. • 0: The local device does not have the next page ability • 1: The local device has the next page ability The PCS always returns this bit as 0 because it does not support Next Page.
1	PG_RCVD	R	0h	Page Received. This bit indicates that the local device received a page from the link partner. • 0: The local device did not receive a new page • 1: The local device received a new page Type: Latch High.
0	*reserved*	R	0h	Ignore on read.

7.4.1.208 SGMII_EXTENDED_STATUS register

Table 264. SGMII_EXTENDED_STATUS register - SGMII PCS register (address B00Fh)

Bit	Symbol	Access	Value	Description
15	CAP_1G_X_FD	R	1h	1000BASE-X Full-Duplex Capable.

Table 264. SGMII_EXTENDED_STATUS register - SGMII PCS register (address B00Fh)*...continued*

Bit	Symbol	Access	Value	Description
				• 0: Not 1000BASE-X full-duplex capable • 1: 1000BASE-X full-duplex capable The PCS always returns this bit as 1 because it does support this feature.
14	CAP_1G_X_HD	R	1h	1000BASE-X Half-Duplex Capable. • 0: Not 1000BASE-X half-duplex capable • 1: 1000BASE-X half-duplex capable The PCS always returns this bit as 1 because in principle it does have the capability to support a half-duplex MAC. However, it does not indicate actual half-duplex operation, this is not supported at chip level.
13	CAP_1G_T_FD	R	0h	1000BASE-T Full-Duplex Capable. • 0: Not 1000BASE-T full-duplex capable • 1: 1000BASE-T full-duplex capable The PCS always returns this bit as 0 because it does not support this feature.
12	CAP_1G_T_HD	R	0h	1000BASE-T Half-Duplex Capable. • 0: Not 1000BASE-T half-duplex capable • 1: 1000BASE-T half-duplex capable The PCS always returns this bit as 0 because it does not support this feature.
11:0	*reserved*	R	0h	Ignore on read.

7.4.1.209 SGMII_ADVANCED_CONTROL register

Table 265. SGMII_ADVANCED_CONTROL register - Advanced control (address B010h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	*reserved*	R	0	always write 0, ignore on read.
14	CONFIG_ENABLE	RW		SGMII PHY configuration register write protection
			0*	SGMII PHY configuration registers cannot be changed
			1	SGMII PHY configuration registers can be changed
13:2	*reserved*	R	000h	always write 0, ignore on read.
1	GOTO_STANDBY	RW		go to standby mode; transition to standby mode takes 100 µs and no SMI transaction should be issued during this time
			0*	no action
			1	go to standby
0	START_OPERATION	RW		start operation by exiting standby
			0*	no action
			1	exit standby

7.4.1.210 SGMII_ADVANCED_STATUS register

Table 266. SGMII_ADVANCED_STATUS register - Advanced status (address B011h)

Bit	Symbol	Access	Value	Description
15:3	*reserved*	R	0h	Ignore on read.
2	LINK_STATUS	R	0h	This bit represents the actual link_status value of the SGMII PHY.
1:0	*reserved*	R	0h	Ignore on read.

7.4.1.211 SGMII_ADVANCED_CONFIG register

Table 267. SGMII_ADVANCED_CONFIG register - Advanced configuration (address B013h)

Bit	Symbol	Access	Value	Description
15:1	*reserved*	R	0h	Always write 0, ignore on read.
0	AUTO	RW		Advanced configuration
			0*	PHY pauses in STANDBY at startup, until the start_operate bit is set.
			1	PHY autonomously proceeds to Normal mode for both startup and wake-up.

7.4.1.212 SGMII_IRQ_SOURCE register

Table 268. SGMII_IRQ_SOURCE register - SGMII interrupt source (address B014h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	TOPDOWN_RESET	RW		Top-down SGMII reset due to global reset event. All configuration settings return to defaults.This bit is W1 C (Cleared on W1).
			0*	no top-down reset since last clear
			1	top-down reset since last clear
14:5	*reserved*	R	0h	Always write 0, ignore on read.
4	FIFO_OVF	RW		SGMII PCS RX FIFO overflow. This bit is W1C (cleared on W1).
			0*	no RX FIFO overflow since last clear
			1	RX FIFO overflow since last clear
3	FIFO_UNF	RW		SGMII PCS RX FIFO underflow. This bit is W1C (Cleared on W1).
			0*	no RX FIFO underflow since last clear
			1	RX FIFO underflow since last clear
2	AUTONEG_EVENT	RW		First read B001 h.5 to check Auto-Negotiation has completed. If so, the contents of the AN MMD Advertisement, AN MMD Link partner Ability, and AN MMD Expansion registers are valid. This bit is W1C (Cleared on W1).
			0*	no Auto-Negotiation process (re)start or completion event

Table 268. SGMII_IRQ_SOURCE register - SGMII interrupt source (address B014h) *...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
			1	Auto-Negotiation process has been (re)started or completed
1	RX_LINK_STATUS_EVENT	RW		The actual SGMII link status is available in register B011h.2. This bit is W1C (Cleared on W1).
			0*	This link did not change since last clear
			1	This link status changed since last clear
0	*reserved*	R	0h	Always write 0, ignore on read.

7.4.1.213 SGMII_IRQ_ENABLE register

Table 269. SGMII_IRQ_ENABLE register - SGMII interrupt enables (address B015h)

Bit	Symbol	Access	Value	Description
15	TOPDOWN_RESET_ENABLE	RW	0h	If set, the respective IRQ is enabled This setting is preserved during deep sleep.
14:5	*reserved*	RW	0h	Always write 0, ignore on read.
4	FIFO_OVF_ENABLE	RW	0h	If set, the respective IRQ is enabled This setting is preserved during deep sleep.
3	FIFO_UNF_ENABLE	RW	0h	If set, the respective IRQ is enabled This setting is preserved during deep sleep.
2	AUTONEG_EVENT_ENABLE	RW	0h	If set, the respective IRQ is enabled This setting is preserved during deep sleep.
1	RX_LINK_STATUS_EVENT_ENABLE	RW	0h	If set, the respective IRQ is enabled This setting is preserved during deep sleep.
0	*reserved*	R	0h	Always write 0, ignore on read.

7.4.1.214 SGMII_IRQ_MSTATUS register

Table 270. SGMII_IRQ_MSTATUS register - SGMII interrupt mask status. This is AND of IRQ_SOURCE and IRQ_ENABLE (address B016h)

Bit	Symbol	Access	Value	Description
15	TOPDOWN_RESET_MSTS	R	0h	This is AND of IRQ_SOURCE and IRQ_ENABLE related to TOPDOWN_RESET _IRQ.
14:5	*reserved*	R	0h	Ignore on read.
4	FIFO_OVF_MSTS	R	0h	This is AND of IRQ_SOURCE and IRQ_ENABLE related to FIFO_OVF IRQ.
3	FIFO_UNF_MSTS	R	0h	This is AND of IRQ_SOURCE and IRQ_ENABLE related to FIFO_UNF IRQ.
2	AUTONEG_EVENT_MSTS	R	0h	This is AND of IRQ_SOURCE and IRQ_ENABLE related to AUTONEG_EVENTIRQ.
1	RX_LINK_STATUS_EVENT_MSTS	R	0h	This is AND of IRQ_SOURCE and IRQ_ENABLE related to RX_LINK_STATUS_EVENT IRQ.
0	*reserved*	R	0h	Ignore on read.

7.4.1.215 SGMII_LED_TRIGGER0 register

Table 271. SGMII_LED_TRIGGER0 register - SGMII LED trigger 0 (address B040h)
Registers SGMII_LED_TRIGGER1 (B041h) to 3 (B043h) have identical entries

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	0h	If set, the trigger is enabled
14:4	*reserved*	R	0h	Always write 0, ignore on read.
3:0	FUNCTION	RW	0h	Selectable LED functions: 0 = Reserved 1 = Link_status 2 = Role: MAC(0) or PHY(1) 3 = PHY active (AFE enabled) 4 = Frame reception (RX_DV = true) 5 = Symbol error 6 = Frame transmission (TX_EN=true) 7 = Frame activity (RX_DV=true | TX_EN=true)

7.4.1.216 SGMII_PCS_CONTROL register

Table 272. SGMII_PCS_CONTROL register - SGMII PCS register (address B070h)

Bit	Symbol	Access	Value	Description
15	VR_RST	RW	0h	Vendor-Specific Soft Reset. When the host sets this bit, this triggers the vendor-specific software reset process in which all internal blocks are reset, except the APB interface block and PCS registers. When this bit is set, it does reset the PMA & PMD registers. This bit is self-cleared after 32 clock cycles of the APB bus clock. Type: Self Clearing.
14	R2TLBE	RW	0h	PCS Rx to Tx Loopback Enable. This bit controls the PCS loopback path from the GMII Rx to the GMII Tx at the GMII interface. • 0: Loopback path is disabled • 1: Loopback path is enabled
13	*reserved*	RW	0h	always write 0; ignore on read.
12	CL37_BP	R	0h	Enable Clause 37 AN in Backplane Configuration. The PCS always returns this bit as 0 because it does not support this feature.
11:10	*reserved*	R	0h	ignore on read.
9	MAC_AUTO_SW	RW	0h	Automatic Speed Mode Change after SGMII CL37 AN Completion. This bit controls the automatic change of the PCS speed and duplex mode settings after completion of SGMII Clause 37 auto-negotiation. • 0: The PCS will not automatically change the speed/duplex mode and operate at the speed/duplex mode according to the values programmed to SR MII MMD Control Register (SGMII_BASIC_CONTROL). After the completion of CL37 AN, the application has to read the negotiated Speed/ Duplex Mode from the VR MII MMD AN Interrupt and Status Register (SGMII_AUTONEG_STATUS) and then

Table 272. SGMII_PCS_CONTROL register - SGMII PCS register (address B070h)*...continued*

Bit	Symbol	Access	Value	Description
				program the SR MII MMD Control Register (SGMII_BASIC_CONTROL) appropriately. • 1: The PCS automatically switches to the negotiated SGMII speed/duplex mode settings, after the completion of Clause 37 auto-negotiation. This mode is valid only when PCS is configured as MAC-side SGMII (TX_CONFIG=0 and PCS_MODE set to the SGMII) and should be set only when auto-negotiation is enabled (AN_ENABLE=1). Note: Only PCS speed/duplex mode settings are impacted and the application must still adjust other chip level speed/duplex mode settings appropriately.
8	INIT	RW	0h	Datapath Initialization Control. This bit can be set to flush/initialize the various FIFOs implemented in the PCS. This is a self-clearing bit. After writing a 1 to this bit, the application should poll this bit continuously and proceed to any other operation only after reading this bit as 0. Note: When this bit is programmed to 1, the RXFIFO_OVF/RXFIFO_UNF bits of VR MII MMD Digital Status Register (SGMII_PCS_STATUS) can get set incorrectly. Hence, these register bits must be read so that they get cleared. Type: Self Clearing.
7	MSK_RD_ERR	R	0h	Mask Running Disparity Error. The PCS always returns this bit as 0 because it does not support this feature.
6	PRE_EMP	RW	0h	Pre-emption Packet Enable. This bit must be set to 1 to allow the PCS to properly receive/transmit pre-emption packets in SGMII 10M/100M Modes.
4:5	*reserved*	R	0h	always write 0, ignore on read.
4	DTXLANED_0	RW	0h	Disable Tx Lane of the PMD. This bit should always be set to 0 as the PCS does not support this feature.
3	*reserved*	RW	0h	always write 0; ignore on read.
2	EN_2_5G_MODE	RW	0h	Enable 2.5G SGMII Mode. This bit should be set to 1 to enable 2.5G SGMII mode of operation. • 0: 2.5G SGMII mode is disabled and 1000M/100M/10M operation is supported • 1: 2.5G SGMII mode is enabled and only 2500M operation is supported Note: This bit must be set to 0 to allow SGMII to operate in 10/100/1000M.
1	BYP_PWRUP	R	0h	Reserved
0	PHY_MODE_CTRL	RW	1h	PHY mode AN advertisement control. This bit controls the Clause 37 auto-negotiation advertisement when operating in SGMII PHY mode. • 0: During SGMII autonegotiation the PCS advertises the values programmed to SGMII_LINK_STS of VR MII MMD AN Control Register (SGMII_PCS_CONFIG2), SS13 and

Table 272. SGMII_PCS_CONTROL register - SGMII PCS register (address B070h)*...continued*

Bit	Symbol	Access	Value	Description
				SS6 of SR MII MMD Control Register (SGMII_BASIC_ CONTROL) and FD of SR MII MMD AN Advertisement Register (SGMII_AUTONEG_ADVERTISE). • 1: During SGMII autonegotiation the PCS advertises the values of internal hardware input ports, controlled by chip level settings, in the SR MII MMD AN Advertisement Register (SGMII_AUTONEG_ADVERTISE). Note: This bit should be set only when the PCS is configured as PHY-side SGMII i.e. TX_CONFIG=1.

7.4.1.217 SGMII_PCS_STATUS register

Table 273. SGMII_PCS_STATUS register - SGMII PCS register (address B071h)

Bit	Symbol	Access	Value	Description
15:7	*reserved*	R	0h	ignore on read
6	RXFIFO_OVF	R	0h	Rx FIFO Overflow. This bit indicates overflow of the clock rate compensation FIFO. • 0: Normal operation • 1: FIFO overflow Type: Latch High.
5	RXFIFO_UNDF	R	0h	Rx FIFO Underflow. This bit indicates underflow of the clock rate compensation FIFO. • 0: Normal operation • 1: FIFO underflow Type: Latch High.
4:0	*reserved*	R	0h	ignore on read.

7.4.1.218 SGMII_PCS_CONFIG1 register

Table 274. SGMII_PCS_CONFIG1 register - SGMII PCS register (address B073h)

Bit	Symbol	Access	Value	Description
15:5	*reserved*	R	0h	Always write 0, ignore on read.
4	TX_POL_INV_0	RW	1h	Tx Polarity Invert. When set the data polarity on the Tx differential lines is reversed/inverted. Can be used to swap TXP and TXN. • 0: Do not invert data polarity on Tx differential lines • 1: Invert data polarity on Tx differential lines
3:1	*reserved*	R	0h	Always write 0, ignore on read.
0	RX_POL_INV_0	RW	0h	Rx Polarity Invert. When set the data received from Rx serial line is inverted. Can be used to swap RXP and RXN. • 0: Do not invert data polarity of data received from Rx differential lines • 1: Invert data polarity of data received from Rx differential lines

7.4.1.219 SGMII_PCS_CONFIG2 register

Table 275. SGMII_PCS_CONFIG2 register - SGMII PCS register (address B074h)

Bit	Symbol	Access	Value	Description
15:9	*reserved*	R	0h	Always write 0, ignore on read.
8	MII_CTRL	RW	0h	SGMII MII Control. This bit controls the width of the internal MII interface when operating at SGMII speed modes of 10 Mbps or 100 Mbps. • 0: 4-bit MII • 1: 8-bit MII This bit must always be set to 0 for proper operation of the internal MII interface.
7:5	*reserved*	R	0h	Always write 0, ignore on read.
4	SGMII_LINK_STS	RW	1h	SGMII Link Status. This bit is used in Bit 15 of the tx_config_Reg during SGMII Clause 37 auto-negotiation when operating in SGMII PHY-side. • 0: Link Down • 1: Link Up This mode is relevant only when PCS is configured as PHY-side SGMII (TX_CONFIG=1 and PCS_MODE set to the SGMII) and when auto-negotiation is enabled (AN_ENABLE=1).
3	TX_CONFIG	RW	1h	SGMII Transmit Configuration Register select. This bit controls the tx_config_Reg values to be used during the Clause 37 auto-negotiation in SGMII mode. • 0: Configures the PCS as MAC-side SGMII and uses MAC-to-PHY tx_config_Reg values for CL37 AN • 1: Configures the PCS as PHY-side SGMII and uses PHY-to-MAC tx_config_Reg values for CL37 AN This mode is relevant only when PCS is configured as SGMII (PCS_MODE set to the SGMII) and when auto-negotiation is enabled (AN_ENABLE=1).
2:1	PCS_MODE	RW	0h	PCS Mode. This field controls the PCS auto-negotiation (and operating) mode. • 00: 1000BASE-X mode (Clause 37 autonegotiation with tx_config_Reg according to IEEE802.3 Clause 37 and 1000 Base-X) • 01: Reserved • 10: SGMII mode (Clause 37 auto-negotiation with tx_config_Reg according to the SGMII specification) • 11: Reserved
0	MII_AN_INTR_EN	RW	1h	Clause 37 AN Complete Interrupt Enable. This bit controls the generation of an interrupt when Clause 37 auto-negotiation is completed. • 0: Disables the generation of Clause 37 auto-negotiation complete interrupt output • 1: Enables the generation of Clause 37 auto-negotiation complete interrupt output

7.4.1.220 SGMII_AUTONEG_STATUS register

Table 276. SGMII_AUTONEG_STATUS register - SGMII PCS register (address B075h)

Bit	Symbol	Access	Value	Description
15:7	*reserved*	R	0h	ignore on read.
6	LP_CK_STP	R	0h	Link Partner EEE Clock Stop Capability. The PCS always returns this bit as 0 because it does not support this feature.
5	LP_EEE_CAP	R	0h	Link Partner EEE Capability. The PCS always returns this bit as 0 because it does not support this feature.
4:1	CL37_ANSGM_STS	R	0h	Clause 37 AN SGMII Status. This field indicates the status received from remote link after the SGMII autonegotiation is complete. • CL37_ANSGM_STS[0] - 0: Half Duplex • CL37_ANSGM_STS[0] - 1: Full Duplex • CL37_ANSGM_STS[2:1] - 00: 10 Mbps speed link • CL37_ANSGM_STS[2:1] - 01: 100 Mbps speed link • CL37_ANSGM_STS[2:1] - 10: 1000 Mbps speed link • CL37_ANSGM_STS[2:1] - 11: Reserved • CL37_ANSGM_STS[3] - 0: Link is Down • CL37_ANSGM_STS[3] - 1: Link is Up This field is valid only when PCS is configured as SGMII (PCS_MODE set to the SGMII) and the autonegotiation is complete.
0	CL37_ANCMPLT_INTR	RW	0h	Clause 37 AN Complete Interrupt. The PCS sets this bit when Clause 37 autonegotiation is complete. The host must clear this bit by writing 0 to it. Type: Self Set / Write Clear.

7.5 Shared

7.5.1 Register description

Table 277. Register overview: Shared

Address	Name	Access	Reset	Description
2h	PHY_IDENTIFIER0	R	1Bh	PHY Identifier 0 register
3h	PHY_IDENTIFIER1	R	B013h	PHY Identifier 1 register
5h	DEVICES_IN_PACKAGE1	R	Bh	Devices in package 1 register
6h	DEVICES_IN_PACKAGE2	R	4000h	Devices in package 2 register
Eh	PACKAGE_IDENTIFIER0	R	1Bh	Package identifier 0 register
Fh	PACKAGE_IDENTIFIER1	R	B010h	Package identifier 1 register
8021h	COMPOSITE_STATUS	RW	3000h	Composite SGMII and Ethernet PHY status. Only applicable for TJF1103B
8040h	PORT_CONTROL	RW	0h	Port control register
8046h	PORT_ABILITIES	R	TJF1103A: 868h	Port abilities register
			TJF1103B: 808h	
8048h	PORT_FUNC_ENABLE	RW	2004h	Port functionality enable register
8070h	PORT_LEVEL_IRQ_SOURCE	RW	0h	Port-level IRQ source register
8072h	PORT_LEVEL_IRQ_ENABLE	RW	0h	Port-level IRQ enable register
8074h	PORT_LEVEL_IRQ_MSTATUS	R	0h	Port-level IRQ masked status register
8078h	PORT_FUNC_IRQ_STATUS	R	0h	Port-level IRQ status of sub-functions
807Ah	PORT_FUNC_IRQ_ENABLE	RW	B00Ch	Port-level IRQ enables of sub-functions
807Ch	PORT_FUNC_IRQ_MSTATUS	R	0h	Port-level IRQ masked status of sub-functions
8080h	EPHY_CAT_IRQ_SOURCE	R	0h	Ethernet PHY category IRQ source register
8081h	EPHY_CAT_IRQ_ENABLE	RW	555h	Ethernet PHY category enable register
8082h	EPHY_CAT_IRQ_MSTATUS	R	0h	Ethernet PHY category status register
80A0h	EPHY_FUNCTIONAL_IRQ_SOURCE	RW	0h	Ethernet PHY functional IRQ source register
80A1h	EPHY_FUNCTIONAL_IRQ_ENABLE	RW	0h	Ethernet PHY functional IRQ enable register
80A2h	EPHY_FUNCTIONAL_IRQ_MSTATUS	R	0h	Ethernet PHY functional IRQ masked status register
80C0h	EPHY_CONFIG_REGXS_IRQ_SOURCE	RW	0h	Ethernet PHY configuration register access IRQs source
80C1h	EPHY_CONFIG_REGXS_IRQ_ENABLE	RW	0h	Ethernet PHY configuration register access IRQs enable

Table 277. Register overview: Shared...*continued*

Address	Name	Access	Reset	Description
80C2h	EPHY_CONFIG_REGXS_IRQ_MSTATUS	R	0h	Ethernet PHY configuration register access IRQs masked status
80D0h	EPHY_DIAGNOSTIC_IRQ_SOURCE	RW	0h	Ethernet PHY diagnostic IRQ source register
80D1h	EPHY_DIAGNOSTIC_IRQ_ENABLE	RW	0h	Ethernet PHY diagnostic IRQ enable register
80D2h	EPHY_DIAGNOSTIC_IRQ_MSTATUS	R	0h	Ethernet PHY diagnostic masked IRQ masked status
8100h	PHY_CONTROL	RW	0h	PHY control register
8102h	PHY_STATUS	R	0h	PHY Status register
8104h	PHY_LATCHED_STATUS	RW	0h	PHY latched status register
8106h	PHY_ADDITIONAL_ABILITIES	R	6h	Additional PHY Abilties
8108h	PHY_CONFIG	RW	0h	PHY configuration register. This register can only be changed if CONFIG_ENABLE or SUPER_CONFIG_ENABLE are set to 1.
810Ch	PHY_STATE	R	0h	PHY state register
810Eh	PHY_PARAMETERS	RW	0h	PHY parameters registter. This register can only be changed if CONFIG_ENABLE or SUPER_CONFIG_ENABLE are set to 1.
8180h	WAKE_SLEEP_CONTROL	RW	0h	Wake sleep control register
8181h	WAKE_SLEEP_STATUS	RW	0h	Wake sleep status register
8182h	WAKE_SLEEP_CONFIG	RW	8032h	Wake sleep configuration register. This register can only be changed if CONFIG_ENABLE or SUPER_CONFIG_ENABLE are set to 1.
8184h	WAKE_SLEEP_PARAMETERS	RW	6333h	Wake sleep parameters register. This register can only be changed if CONFIG_ENABLE or SUPER_CONFIG_ENABLE are set to 1.
8190h	EPHY_LED_TRIGGER0	RW	8000h	Ethernet PHY LED trigger output 0 register
8191h	EPHY_LED_TRIGGER1	RW	TJF1103A:8000h TJF1103B: 8004h	Ethernet PHY LED trigger output 1 register, see EPHY_LED_TRIGGER0
8192h	EPHY_LED_TRIGGER2	RW	TJF1103A:8000h TJF1103B: 8006h	Ethernet PHY LED trigger output 2 register, see EPHY_LED_TRIGGER0
8193h	EPHY_LED_TRIGGER3	RW	TJF1103A:8000h TJF1103B: 0000h	Ethernet PHY LED trigger output 3 register, see EPHY_LED_TRIGGER0
8319h	TXC_STATUS	RW	0h	TXC status register
831Ah	RXC_STATUS	RW	0h	RXC status register
831Bh	SGMII_LATENT_STATUS	RW	0h	SGMII latent fault status register

Table 277. Register overview: Shared...*continued*

Address	Name	Access	Reset	Description
831Ch	EPHY_LATENT_STATUS	RW	0h	Ethernet PHY latent fault status register
831Dh	SGMII_CLK_STATUS	RW	0h	SGMII clock status register
831Eh	EPHY_CLK_STATUS	RW	0h	Ethernet PHY clock status
8320h	SIGNAL_QUALITY	RW	70h	Signal quality
8324h	MSE	RW	0h	Mean-square error register
8325h	MAX_MSE	R	0h	Max mean-square error register
8330h	CABLE_TEST	RW	0h	Cable test register
8340h	LINK_TRAINING_TIMER	R	0h	Link training timer register
8341h	LOC_RCVR_STATUS_ TIMER	R	0h	Local receiver status timer register
8342h	REM_RCVR_STATUS_ TIMER	R	0h	Remote receiver status timer register
8343h	FOLLOWER_SILENT_ TIMER	R	0h	Follower silent timer register
8350h	SYMBOL_ERROR_ COUNTER	R	0h	Symbol error counter register
8352h	ERROR_COUNTER_MISC	RW	8000h	Error counter miscellaneous register
8353h	LINK_LOSSES_AND_ FAILURES	R	0h	Link losses and failures counter register
83F0h	PHY_COMPLIANCE_TEST	RW	0h	PHY compliance test control register

7.5.1.1 PHY_IDENTIFIER0 register

Table 278. PHY_IDENTIFIER0 register - PHY Identifier 0 register (address 2h)

Bit	Symbol	Access	Value	Description
15:0	OUI_BITS_3_TO_18	R	1Bh	OUI bits [3:18] OUI = 00:60:37

7.5.1.2 PHY_IDENTIFIER1 register

Table 279. PHY_IDENTIFIER1 register - PHY Identifier 1 register (address 3h)

Bit	Symbol	Access	Value	Description
15:10	OUI_BITS_19_TO_24	R	2Ch	OUI bits [19:24] OUI = 00:60:37
9:4	MODEL	R	1h	6-bit PHY model number
3:0	REVISION	R	3h	4-bit PHY revision number

7.5.1.3 DEVICES_IN_PACKAGE1 register

Table 280. DEVICES_IN_PACKAGE1 register - Devices in package 1 register (address 5h)

Bit	Symbol	Access	Value	Description
15:8	*reserved*	R	0h	Ignore on read.

Table 280. DEVICES_IN_PACKAGE1 register - Devices in package 1 register (address 5h)*...continued*

Bit	Symbol	Access	Value	Description
7	AN_PRESENT	R	0h	If set, Auto-Negotiation present in package
6	TC_PRESENT	R	0h	If set, TC present in package
5	DTE_XS_PRESENT	R	0h	If set, DTE XS present in package
4	PHY_XS_PRESENT	R	0h	If set, PHY XS present in package
3	PCS_PRESENT	R	1h	If set, PCS present in package
2	WIS_PRESENT	R	0h	If set, WIS present in package
1	PMD_PMA_ PRESENT	R	1h	If set, PMA/PMD present in package
0	CL22_PRESENT	R	1h	If set, Clause 22 registers present in package

7.5.1.4 DEVICES_IN_PACKAGE2 register

Table 281. DEVICES_IN_PACKAGE2 register - Devices in package 2 register (address 6h)

Bit	Symbol	Access	Value	Description
15	MMD31_PRESENT	R	0h	If set, Vendor specific device 2 present in package
14	MMD30_PRESENT	R	1h	If set, Vendor specific device 1 present in package
13	CL22_EXT_ PRESENT	R	0h	If set, Clause 22 extension present in package
12:0	*reserved*	R	0h	Ignore on read.

7.5.1.5 PACKAGE_IDENTIFIER0 register

Table 282. PACKAGE_IDENTIFIER0 register - Package identifier 0 register (address Eh)

Bit	Symbol	Access	Value	Description
15:0	OUI_BITS_3_TO_18	R	1Bh	OUI bits [3:18] OUI = 00:60:37

7.5.1.6 PACKAGE_IDENTIFIER1 register

Table 283. PACKAGE_IDENTIFIER1 register - Package identifier 1 register (address Fh)

Bit	Symbol	Access	Value	Description
15:10	OUI_BITS_19_TO_24	R	2Ch	OUI bits [19:24] OUI = 00:60:37
9:4	MODEL	R	1h	6-bit Package model number
3:0	REVISION	R	0h	4-bit Package revision number

7.5.1.7 COMPOSITE_STATUS register

Table 284. COMPOSITE_STATUS register - Composite SGMII and Ethernet PHY status. Only applicable for TJF1103B (address 8021h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	AN_LINK_STATUS	R	0h	If the device operates in SGMII-MAC mode, this bit indicates the received LINK_STATUS according to TX_CONFIG_REG[15].
14:12	LINK_STATUS_SELECT	RW		Selects the source for TX_CONFIG_REG[15] used in the SGMII auto negotiation process. This interface must operate in SGMII-PHY mode. This setting is preserved during deep sleep.
			000	Reserved
			001	SGMII RX Link Status
			010	ePHY Link Availability
			011*	ePHY Link Available & SGMII RX Link Status
			1xx	Reserved
11:0	*reserved*	RW	0h	Always write all 0s, ignore on read.

7.5.1.8 PORT_CONTROL register

Table 285. PORT_CONTROL register - Port control (address 8040h)

Bit	Symbol	Access	Value	Description
15	RESET	RW	0h	If set, reset all functionality of this PORT. This bit is self-clearing.[1]
14	CONFIG_ENABLE	RW	0h	If set, configuration registers of this PORT (see PORT_FUNC_ENABLES) can be changed. Otherwise, the configuration registers are write-protected.
13:0	*reserved*	RW	0h	Always write all 0s, ignore on read.

[1] For TJF1103A: in RMII-clkmode, this will cause REFCLK_WARN and TXC_STATUS to be set.

7.5.1.9 PORT_ABILITIES register

Table 286. PORT_ABILITIES register - Port abilities (address 8046h)

Bit	Symbol	Access	Value	Description
15:12	*reserved*	R	0h	Ignore on read.
11	BIST_ABILITY	R	1h	If set, this port supports BIST
10:4	*reserved*	R	0h	Ignore on read.
3	PTP_ABILITY	R	1h	If set, this port supports PTP
2:1	*reserved*	R	0h	Ignore on read.
0	PORT_ABILITY_XTD	R	0h	Extended port abilities

7.5.1.10 PORT_FUNC_ENABLE register

Table 287. PORT_FUNC_ENABLE register - Port functionality enable register (address 8048h)

Bit	Symbol	Access	Value	Description
15:14	*reserved*	R	0h	Always write all 0s, ignore on read.
13	MII_ENABLE	RW	1h	If deasserted, the xMII interface (MII, RMII, RGMII, SGMII) is detached from the datapath. Device outputs become high-Z and inputs are disabled. This setting is configuration protected.
12	*reserved*	R	0h	Always write 0, ignore on read.
11	BIST_ENABLE	RW	0h	If set, BIST functionality is enabled for this PORT This setting is configuration protected.
10:4	*reserved*	R	0h	Always write all 0s, ignore on read.
3	PTP_ENABLE	RW	0h	If set, PTP functionality is enabled for this PORT. This setting is configuration protected.
2	EPHY_ENABLE	RW	1h	If set, Ethernet PHY of this PORT is enabled. This setting is configuration protected.
1	*reserved*	R	0h	Always write 0, ignore on read.
0	TEST_ENABLE	RW	0h	By default, entering test modes is restricted and guarded by respective TEST_ENABLE bits. This bit enables test mode selection of all sub-functions (ePHY, BIST and xMII) of a port. If this bit is not set, selecting a test mode has no effect, unless the TEST_ENABLE is set on global level or a sub-function specific TEST_ENABLE is set. If this bit is set, a test mode of all sub-functions can be entered. Note, the TEST_ENABLEs through the hierarchy (global, port, port sub-functions) are ORed. This setting is preserved during deep sleep. This setting is configuration protected.

7.5.1.11 PORT_LEVEL_IRQ_SOURCE register

Table 288. PORT_LEVEL_IRQ_SOURCE register - Port-level IRQ sources (address 8070h)

Bit	Symbol	Access	Value	Description
15	*reserved*	R	0h	Always write 0, ignore on read.
14	EPHY_CLK_WARN	RW	0h	If set, the Ethernet PHY clock warning is present, see EPHY_CLK_STATUS Write one to clear. This bit is latched-high.
13	SGMII_CLK_WARN	RW	0h	If set, the SGMII clock warning is present, see SGMII_CLK_STATUS Write one to clear. This bit is latched-high.
12	EPHY_LF	RW	0h	If set, the Ethernet latent fault is present, see EPHY_LATENT_STATUS Write one to clear.

Table 288. PORT_LEVEL_IRQ_SOURCE register - Port-level IRQ sources (address 8070h)*...continued*

Bit	Symbol	Access	Value	Description
				This bit is latched-high.
11	SGMII_LF	RW	0h	If set, the SGMII latent fault is present, see SGMII_LATENT_STATUS Write one to clear. This bit is latched-high.
10	TXC_CLK_WARN	RW	0h	If set, TXC clock warning is present, see TXC_STATUS register Write one to clear. This bit is latched-high.
9	RXC_CLK_WARN	RW	0h	If set, RXC clock warning is present, see RXC_STATUS register. Write one to clear. This bit is latched-high.
8:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.5.1.12 PORT_LEVEL_IRQ_ENABLE register

Table 289. PORT_LEVEL_IRQ_ENABLE register - Port-level IRQ enables (address 8072h)

Bit	Symbol	Access	Value	Description
15	*reserved*	R	0h	Always write 0, ignore on read.
14	EPHY_CLK_WARN	RW	0h	Enable for ePHY CLOCK_WARN interrupt; this setting is preserved during deep sleep
13	SGMII_CLK_WARN	RW	0h	Enable for SGMII Clock Warn Interrupt; this setting is preserved during deep sleep
12	EPHY_LF	RW	0h	Enable for ephy Link Latent Fault; this setting is preserved during deep sleep
11	SGMII_LF	RW	0h	Enable for SGMII Link Latent Fault; this setting is preserved during deep sleep
10	TXC_CLK_WARN	RW	0h	Enable for TXC Clock warn Interrupt; this setting is preserved during deep sleep
9	RXC_CLK_WARN	RW	0h	Enable for RXC Clock warn interrupt; this setting is preserved during deep sleep
8:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.5.1.13 PORT_LEVEL_IRQ_MSTATUS register

Table 290. PORT_LEVEL_IRQ_MSTATUS register - Port-level IRQ masked status (address 8074h)

Bit	Symbol	Access	Value	Description
15	*reserved*	R	0h	Ignore on read.
14	EPHY_CLK_WARN	R	0h	Masked-status of Ethernet PHY CLOCK_WARN interrupt
13	SGMII_CLK_WARN	R	0h	Masked Status of SGMII Clock Warn Interrupt
12	EPHY_LF	R	0h	Masked status of ePHY link Latent fault
11	SGMII_LF	R	0h	Masked Status of SGMII Link Latent fault

Table 290. PORT_LEVEL_IRQ_MSTATUS register - Port-level IRQ masked status (address 8074h)*...continued*

Bit	Symbol	Access	Value	Description
10	TXC_CLK_WARN	R	0h	Masked status of TXC Clock warn Fault
9	RXC_CLK_WARN	R	0h	Masked status of RXC Clock warn fault
8:0	*reserved*	R	0h	Ignore on read.

7.5.1.14 PORT_FUNC_IRQ_STATUS register

Table 291. PORT_FUNC_IRQ_STATUS register - Port-level IRQ status of sub-functions (address 8078h)

Bit	Symbol	Access	Value	Description
15	PORT_LEVEL_IRQ	R	0h	Status bit indicating an interrupt at PORT-level from functionality that doesn't belong to one specific sub-function.
14	*reserved*	R	0h	Ignore on read.
13	SERDES_MII_IRQ	R	0h	Status bit indicating an interrupt from the SERDES-MII (SGMII) function of this port when it is configured to use this MII type.
12	INFRA_IRQ	R	0h	Status bit indicating an interrupt from INFRAstructure functionality for this port.
11:4	*reserved*	R	0h	Ignore on read.
3	PTP_IRQ	R	0h	Status bit indicating an interrupt from the PTP function of this port.
2	EPHY_IRQ	R	0h	Status bit indicating an interrupt from the ePHY of this port.
1:0	*reserved*	R	0h	Ignore on read.

7.5.1.15 PORT_FUNC_IRQ_ENABLE register

Table 292. PORT_FUNC_IRQ_ENABLE register - Port-level IRQ enables of sub-functions (address 807Ah)

Bit	Symbol	Access	Value	Description
15	PORT_LEVEL_IRQ	RW	1h	Enable for port level interrupt This setting is preserved during deep sleep.
14	*reserved*	R	0h	Always write 0, ignore on read.
13	SERDES_MII_IRQ	RW	1h	Enable for SERDES-MII interrupt This setting is preserved during deep sleep.
12	INFRA_IRQ	RW	1h	Enable for INFRA interrupt This setting is preserved during deep sleep.
11:4	*reserved*	R	0h	Always write all 0s, ignore on read.
3	PTP_IRQ	RW	1h	Enable for PTP interrupt This setting is preserved during deep sleep.
2	EPHY_IRQ	RW	1h	Enable for Ethernet PHY interrupt This setting is preserved during deep sleep.
1:0	*reserved*	R	0h	Always write 00, ignore on read.

7.5.1.16 PORT_FUNC_IRQ_MSTATUS register

Table 293. PORT_FUNC_IRQ_MSTATUS register - Port-level IRQ masked status of sub-functions (address 807Ch)

Bit	Symbol	Access	Value	Description
15	PORT_LEVEL_IRQ	R	0h	Masked status of PORT_LEVEL interrupt
14	*reserved*	R	0h	Ignore on read.
13	SERDES_MII_IRQ	R	0h	Masked status of SERDES-MII interrupt
12	INFRA_IRQ	R	0h	Masked status of INFRA interrupt
11:4	*reserved*	R	0h	Ignore on read.
3	PTP_IRQ	R	0h	Masked status of PTP interrupt
2	EPHY_IRQ	R	0h	Masked status of ePHY interrupt
1:0	*reserved*	R	0h	Ignore on read.

7.5.1.17 EPHY_CAT_IRQ_SOURCE register

Table 294. EPHY_CAT_IRQ_SOURCE register - Ethernet PHY category IRQ sources (address 8080h)

Bit	Symbol	Access	Value	Description
15:11	*reserved*	R	0h	Ignore on read.
10	EPHY_ DIAGNOSTIC_IRQ	R	0h	If set, pending interrupts present in 'Diagnosis and Test interrupts' source register
9	*reserved*	R	0h	Ignore on read.
8	EPHY_CONFIG_ REGXS_IRQ	R	0h	If set, pending interrupts present in 'Config and Register Access' interrupts source register
7:5	*reserved*	R	0h	Always write 000, ignore on read.
4	EPHY_ FUNCTIONAL_IRQ	R	0h	If set, pending interrupts present in 'Functional baseline' source register
3:0	*reserved*	R	0h	Ignore on read.

7.5.1.18 EPHY_CAT_IRQ_ENABLE register

Table 295. EPHY_CAT_IRQ_ENABLE register - Ethernet PHY category enables (address 8081h)

Bit	Symbol	Access	Value	Description
15:11	*reserved*	R	0h	Always write all 0s, ignore on read.
10	EPHY_ DIAGNOSTIC_IRQ	RW	1h	Enable EPHY_DIAGNOSTIC_IRQ category
9	*reserved*	R	0h	Always write 0, ignore on read.
8	EPHY_CONFIG_ REGXS_IRQ	RW	1h	Enable EPHY_CONFIG_REGXS_IRQ category
7:5	*reserved*	R	0h	Always write 000, ignore on read.
4	EPHY_ FUNCTIONAL_IRQ	RW	1h	Enable EPHY_FUNCTIONAL_IRQ category
3:0	*reserved*	R	0h	Always write 0000, ignore on read.

7.5.1.19 EPHY_CAT_IRQ_MSTATUS register

Table 296. EPHY_CAT_IRQ_MSTATUS register - Ethernet PHY category status register (address 8082h)

Bit	Symbol	Access	Value	Description
15:11	*reserved*	R	0h	Ignore on read.
10	EPHY_ DIAGNOSTIC_IRQ	R	0h	Masked status of EPHY_DIAGNOSTIC_IRQ category
9	*reserved*	R	0h	Ignore on read.
8	EPHY_CONFIG_ REGXS_IRQ	R	0h	Masked status of EPHY_CONFIG_REGXS_IRQ category
7:5	*reserved*	R	0h	Ignore on read.
4	EPHY_ FUNCTIONAL_IRQ	R	0h	Masked status of EPHY_FUNCTIONAL_IRQ category
3:0	*reserved*	R	0h	Ignore on read.

7.5.1.20 EPHY_FUNCTIONAL_IRQ_SOURCE register

Table 297. EPHY_FUNCTIONAL_IRQ_SOURCE register - Ethernet PHY functional IRQ sources (address 80A0h)

Bit	Symbol	Access	Value	Description
15	POLARITY_ CONFLICT	RW	0h	If set, unresolved polarity conflict Write one to clear. This bit is latched-high.
14	TRAINING_ FAILURE	RW	0h	If set, failure occured during training. This including but is not necessarilly restricted to expiration of the max_wait_timer. Write one to clear. This bit is latched-high.
13	TRANSMIT_ FAILURE	RW	0h	If set, attempt to transmit data without a link availale Write one to clear. This bit is latched-high.
12:5	*reserved*	R	0h	Always write all 0s, ignore on read.
4	*reserved*	RW	0h	Always write 0, ignore on read.
3	WAKE_SLEEP_ EVENT	RW	0h	If set, the PHY's Wake-Sleep status has changed Write one to clear. This bit is latched-high.
2	LINK_AVAILABLE_ EVENT	RW	0h	If set, LINK_AVAILABILITY has changed Write one to clear. This bit is latched-high.
1	LINK_STATUS_ EVENT	RW	0h	If set, LINK_STATUS has changed Write one to clear. This bit is latched-high.
0	*reserved*	R	0h	Always write 0, ignore on read.

7.5.1.21 EPHY_FUNCTIONAL_IRQ_ENABLE register

Table 298. EPHY_FUNCTIONAL_IRQ_ENABLE register - Ethernet PHY functional IRQ enables (address 80A1h)

Bit	Symbol	Access	Value	Description
15	POLARITY_ CONFLICT	RW	0h	If set, POLARITY_CONFLICT IRQ is enabled This setting is preserved during deep sleep.
14	TRAINING_ FAILURE	RW	0h	If set, TRAINING_FAILURE IRQ is enabled This setting is preserved during deep sleep.
13	TRANSMIT_ FAILURE	RW	0h	If set, TRANSMIT_FAILURE IRQ is enabled This setting is preserved during deep sleep.
12:5	*reserved*	R	0h	Always write all 0s, ignore on read.
4	*reserved*	RW	0h	Always write 0, ignore on read.
3	WAKE_SLEEP_ EVENT	RW	0h	If set, WAKE_SLEEP_EVENT IRQ is enabled This setting is preserved during deep sleep.
2	LINK_AVAILABLE_ EVENT	RW	0h	If set, LINK_AVAILABLE_EVENT IRQ is enabled This setting is preserved during deep sleep.
1	LINK_STATUS_ EVENT	RW	0h	If set, LINK_STATUS_EVENT IRQ is enabled This setting is preserved during deep sleep.
0	*reserved*	R	0h	Always write 0, ignore on read.

7.5.1.22 EPHY_FUNCTIONAL_IRQ_MSTATUS register

Table 299. EPHY_FUNCTIONAL_IRQ_MSTATUS register - Ethernet PHY functional IRQ masked status (address 80A2h)

Bit	Symbol	Access	Value	Description
15	POLARITY_ CONFLICT	R	0h	Masked status of POLARITY_CONFLICT
14	TRAINING_ FAILURE	R	0h	Masked status of TRAINING_FAILURE
13	TRANSMIT_ FAILURE	R	0h	Masked status of TRANSMIT_FAILURE
12:5	*reserved*	R	0h	Ignore on read.
4	*reserved*	R	0h	Always write 0, ignore on read.
3	WAKE_SLEEP_ EVENT	R	0h	Masked status of WAKE_SLEEP_EVENT
2	LINK_AVAILABLE_ EVENT	R	0h	Masked status of LINK_AVAILABLE_EVENT
1	LINK_STATUS_ EVENT	R	0h	Masked status of LINK_STATUS_EVENT
0	*reserved*	R	0h	Ignore on read.

7.5.1.23 EPHY_CONFIG_REGXS_IRQ_SOURCE register

Table 300. EPHY_CONFIG_REGXS_IRQ_SOURCE register - Ethernet PHY configuration register access IRQs sources (address 80C0h)

Bit	Symbol	Access	Value	Description
15	*reserved*	RW	0h	Always write 0, ignore on read.
14:13	*reserved*	R	0h	Always write 0, ignore on read.
12	RECONFIG_ DENIED	RW	0h	If set, Denied config attempt to PHY register Write one to clear. This bit is latched-high.
11	INIT_ERROR	RW	0h	If set, PHY initialization at (re)boot or restart has not completed successfully Write one to clear. This bit is latched-high.
10:2	*reserved*	R	0h	Always write all 0s, ignore on read.
1	SMI_ERROR	RW	0h	If set, this bit flags invalid SMI transactions to this PHY's register space, like writing to read-only registers and reading or writing non-existent registers. Write one to clear. This bit is latched-high.
0	*reserved*	R	0h	Always write 0, ignore on read.

7.5.1.24 EPHY_CONFIG_REGXS_IRQ_ENABLE register

Table 301. EPHY_CONFIG_REGXS_IRQ_ENABLE register - Ethernet PHY configuration register access IRQs enables (address 80C1h)

Bit	Symbol	Access	Value	Description
15	*reserved*	RW	0h	Always write 0, ignore on read.
14:13	*reserved*	R	0h	Always write 00, ignore on read.
12	RECONFIG_ DENIED	RW	0h	If set, RECONFIG_DENIED_EN IRQ is enabled This setting is preserved during deep sleep.
11	INIT_ERROR	RW	0h	If set, INIT_ERROR_EN IRQ is enabled This setting is preserved during deep sleep.
10:2	*reserved*	R	0h	Always write all 0s, ignore on read.
1	SMI_ERROR	RW	0h	If set, SMI_ERROR IRQ is enabled This setting is preserved during deep sleep.
0	*reserved*	R	0h	Always write 0, ignore on read.

7.5.1.25 EPHY_CONFIG_REGXS_IRQ_MSTATUS register

Table 302. EPHY_CONFIG_REGXS_IRQ_MSTATUS register - Ethernet PHY configuration register access IRQs masked status (address 80C2h)

Bit	Symbol	Access	Value	Description
15:13	*reserved*	R	0h	Ignore on read.
12	RECONFIG_ DENIED	R	0h	Masked status of RECONFIG_DENIED IRQ

Table 302. EPHY_CONFIG_REGXS_IRQ_MSTATUS register - Ethernet PHY configuration register access IRQs masked status (address 80C2h)*...continued*

Bit	Symbol	Access	Value	Description
11	INIT_ERROR	R	0h	Masked status of INIT_ERROR IRQ
10:2	*reserved*	R	0h	Ignore on read.
1	SMI_ERROR	R	0h	Masked status of SMI_ERROR IRQ
0	*reserved*	R	0h	Ignore on read.

7.5.1.26 EPHY_DIAGNOSTIC_IRQ_SOURCE register

Table 303. EPHY_DIAGNOSTIC_IRQ_SOURCE register - Ethernet PHY diagnostic IRQ sources (address 80D0h)

Bit	Symbol	Access	Value	Description
15:2	*reserved*	R	0h	Always write all 0s, ignore on read.
1	SQI_WARN	RW	0h	If set, SQI dipped below the selected warning level. Write one to clear. This bit is latched-high.
0	*reserved*	R	0h	Always write 0, ignore on read.

7.5.1.27 EPHY_DIAGNOSTIC_IRQ_ENABLE register

Table 304. EPHY_DIAGNOSTIC_IRQ_ENABLE register - Ethernet PHY diagnostic IRQ enables (address 80D1h)

Bit	Symbol	Access	Value	Description
15:2	*reserved*	R	0h	Always write all 0s, ignore on read.
1	SQI_WARN	RW	0h	If set, SQI_WARN IRQ is enabled This setting is preserved during deep sleep.
0	*reserved*	R	0h	Always write 0, ignore on read.

7.5.1.28 EPHY_DIAGNOSTIC_IRQ_MSTATUS register

Table 305. EPHY_DIAGNOSTIC_IRQ_MSTATUS register - Ethernet PHY diagnostic masked IRQ masked status (address 80D2h)

Bit	Symbol	Access	Value	Description
15:2	*reserved*	R	0h	Ignore on read.
1	SQI_WARN	R	0h	Masked status of SQI_WARN IRQ
0	*reserved*	R	0h	Ignore on read.

7.5.1.29 PHY_CONTROL register

Table 306. PHY_CONTROL register - PHY control register (address 8100h)

Bit	Symbol	Access	Value	Description
15	RESET	RW	0h	If set, the PHY is reset This bit is self-clearing.
14	CONFIG_ENABLE	RW	0h	If set, configuration registers of this PHY can be changed. Otherwise access is restricted.

Table 306. PHY_CONTROL register - PHY control register (address 8100h)*...continued*

Bit	Symbol	Access	Value	Description
				This setting is preserved during deep sleep.
13:2	*reserved*	R	0h	Always write all 0s, ignore on read.
1	GOTO_STANDBY	RW	0h	If set, the PHY is directed to go to STANDBY. This bit is self clearing. On read it returns 1, if the PHY is still in transition. This bit is self-clearing.
0	START_ OPERATION	RW	0h	If set, exit STANDBY state and start PHY operation. This bit is self clearing. On read it returns 1, if the PHY is still in transition. This bit is self-clearing.

7.5.1.30 PHY_STATUS register

Table 307. PHY_STATUS register - PHY Status register (address 8102h)

Bit	Symbol	Access	Value	Description
15:8	*reserved*	R	0h	ignore on read.
7	DETECTED_ POLARITY	R	0h	If set, polarity inversed with respect to pin definitions; polarity correction required
6	LINK_AVAILABLE	R	0h	If set, link is available for use by higher OSI layers
5	SENDN_OR_DATA	R	0h	If set, PHY in SEND_IDLE_OR_DATA state
4	REM_RCVR_ STATUS	R	0h	If set, the remote receiver status is set
3	SCRAMBLER_ STATUS	R	0h	If set, the scrambler is synchronized
2	LINK_STATUS	R	0h	If set, the link status from Link Monitor FSM is set
1	LOC_RCVR_ STATUS	R	0h	If set, the PHY is synchronized to the received signal and symbols values can be robustly detected
0	*reserved*	R	0h	If set,additional status bits in register 8103h ignore on read.

7.5.1.31 PHY_LATCHED_STATUS register

Table 308. PHY_LATCHED_STATUS register - PHY latched status register (address 8104h)

Bit	Symbol	Access	Value	Description
15:3	*reserved*	R	0h	Always write all 0s, ignore on read.
2	REMOTE_FAILURE	RW	0h	If set, a link failure caused by remote event. Write one to clear. This bit is latched-high.
1	EXPIRED_MAX_ WAIT	RW	0h	If set, MAX_WAIT_TIMER has expired since last clear. Write one to clear. This bit is latched-high.
0	*reserved*	R	0h	If set, Additional latched status in register 8105h Always write 0, ignore on read.

7.5.1.32 PHY_ADDITIONAL_ABILITIES register

Table 309. PHY_ADDITIONAL_ABILITIES register - Additional PHY Abilties (address 8106h)

Bit	Symbol	Access	Value	Description
15:3	*reserved*	R	0h	Ignore on read.
2	TC10_ABILITY	R	1h	If set, PHY is able to support TC10 Wake-Sleep
1	BASIC_SLEEP_ ABILITY	R	1h	If set, PHY is able to support SLEEP state
0	*reserved*	R	0h	If set, Additional abilities in register 8107h Ignore on read.

7.5.1.33 PHY_CONFIG register

Table 310. PHY_CONFIG register - PHY configuration register (address 8108h)[1]

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:6	*reserved*	R	0h	Always write all 0s, ignore on read.
5	STATUS_FILTER_ DISABLE	RW	0h	Burst errors robustness is enhanced by filtering signals that drive status bits and the state machine. This avoids burst error-triggered retraining when the PHY is still locked and will likely auto-recover quickly. This bit allows to turn off that filtering. Disabling is strongly discouraged This setting is configuration protected.
4	JUMBO_ENABLE	RW	0h	If set, Enable support for jumbo packets This setting is preserved during deep sleep. This setting is configuration protected.
3	POLARITY_SWAP	RW		Polarity swap The bits [POLARITY_SWAP, POLARITY_CORRECT_ DISABLE] encode the following behavior: 00 = Polarity correction, default pin polarity 01 = No polarity correction, default pin polarity 10 = Polarity correction plus forced polarity swap 11 = Forced polarity swap, no polarity correction This setting is preserved during deep sleep. This setting is configuration protected.
			0*	No additional polarity swap
			1	Enforce an additional polarity swap in order to virtually swap the DP/DN pins
2	POLARITY_ CORRECT_ DISABLE	RW	0h	If set, automatic polarity correction is disabled and no link established in normal mode if input polarity is swapped. This setting is preserved during deep sleep. This setting is configuration protected.
1	TEST_ENABLE	RW	0h	This bit guards against accidental test mode selection of the Ethernet PHY. If this bit is not set, selecting a test mode has no effect, unless TEST_ENABLE was set on port or super level.

Table 310. PHY_CONFIG register - PHY configuration register (address 8108h)[1]*...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
				Test modes do also include loopbacks, cable test, and other standardized or proprietary diagnostic features which are available to the customer but interfer with normal operation. This setting is configuration protected.
0	AUTO_OPERATION	RW	0h	If set, PHY proceeds autonomously to Normal node for both start-up and wake-up. The default confiruration is latched from pin strapping. This setting is preserved during deep sleep. This setting is configuration protected.

[1] This register can only be changed if CONFIG_ENABLE or SUPER_CONFIG_ENABLE are set to 1.

7.5.1.34 PHY_STATE register

Table 311. PHY_STATE register - PHY state register (address 810Ch)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	BUSY	R	0h	TEST_OR_DIAGNOSIS = 0: if set, PHY busy transitioning to next state TEST_OR_DIAGNOSIS = 1: this bit can be ignored (always returns 1)
14	TEST_OR_ DIAGNOSIS	R	0h	If set, the PHY is not functionally operational but in a test or diagnosis state
13:12	*reserved*	R	0h	Ignore on read.
11:8	TRANSMIT_STATE	R		Transmit state. The PHY reports DISABLED when in PMA test modes.
			0000*	DISABLED
			0001	SEND_Z
			1100	SEND_IDLE
			1101	SEND_DATA
			1110	SEND_WUR
			1111	SEND_LPS
			others	Reserved
7:4	*reserved*	R	0h	Ignore on read.
3:0	BASIC_STATE	R		Basic state. Bits [3:2] of this field classify the states into active and inactive states: 00=INACTIVE states 01=Reserved for LPI/EEE 10=ACTIVE transitional states 11=ACTIVE trained states
			0000*	DISABLED
			0001	STANDBY

Table 311. PHY_STATE register - PHY state register (address 810Ch)*...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
			0010	FAILSAFE/Reserved
			0011	SLEEP
			0110	Reserved
			1000	TRAINING
			1001	FOLLOWER_SILENT
			1011	SLEEP_SILENT
			1100	SEND_IDLE (state)
			1101	SEND_IDLE_OR_DATA
			1111	SEND_IDLE_OR_DATA_SLEEP_CHECK
			others	Reserved

7.5.1.35 PHY_PARAMETERS register

Table 312. PHY_PARAMETERS register - PHY parameters registter (address 810Eh)[1]

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:3	*reserved*	R	0h	Always write all 0s, ignore on read.
2:0	LINK_AVAILABLE_HYST_TIME	RW		Time hysteresis on link availability assertion This setting is preserved during deep sleep. This setting is configuration protected.
			000*	0 ms
			001	250 us
			010	500 us
			011	1 ms
			100	2 ms
			101	4 ms
			110	8 ms
			111	16 ms

[1] This register can only be changed if CONFIG_ENABLE or SUPER_CONFIG_ENABLE are set to 1.

7.5.1.36 WAKE_SLEEP_CONTROL register

Table 313. WAKE_SLEEP_CONTROL register - Wake sleep control register (address 8180h)

Bit	Symbol	Access	Value	Description
15	WAKEUP_PHY_REQUEST	RW	0h	If set, wake-up request to this PHY This bit is self-clearing.
14:3	*reserved*	R	0h	Always write all 0s, ignore on read.
2	SLEEP_REJECT	RW	0h	If set, reject sleep request

Table 313. WAKE_SLEEP_CONTROL register - Wake sleep control register (address 8180h)*...continued*

Bit	Symbol	Access	Value	Description
				This bit is self-clearing.
1	SLEEP_ACCEPT	RW	0h	If set, accept sleep request received on MDI This bit is self-clearing.
0	SLEEP_REQUEST	RW	0h	If set, start the handshake to bring this PHY and it link partner into sleep state This bit is self-clearing.

7.5.1.37 WAKE_SLEEP_STATUS register

Table 314. WAKE_SLEEP_STATUS register - Wake sleep status register (address 8181h)

Bit	Symbol	Access	Value	Description
15	*reserved*	RW	0h	Always write 0, ignore on read.
14	WU_IO_RECEIVED	RW	0h	If set, Wake-up request on WAKE_IN_OUT pin received. Write one to clear. This bit is latched-high.
13	*reserved*	RW	0h	Always write 0, ignore on read.
12	WU_PHY_ RECEIVED	RW	0h	If set, Wake-up request received by WU_PHY bit Write one to clear. This bit is latched-high.
11	WUP_RECEIVED	RW	0h	If set, Wake-Up Pulse received Write one to clear. This bit is latched-high.
10	WUR_RECEIVED	RW	0h	If set, Wake-Up Relay received Write one to clear. This bit is latched-high.
9	*reserved*	RW	0h	Always write 0, ignore on read.
8:4	*reserved*	R	0h	Always write 00000, ignore on read.
3	AUTO_SLEEP_ EVENT	RW	0h	If set, Auto sleep has been triggered. This bis is cleared automatically, when the PHY wakes up. Write one to clear. This bit is latched-high.
2	SLEEP_FAILED	RW	0h	If set, Failed to enter Sleep mode. This bis is cleared automatically, when the PHY wakes up. Write one to clear. This bit is latched-high.
1	LPS_RECEIVED	RW	0h	If set, Sleep request received. This bis is cleared automatically, when the PHY wakes up. Write one to clear. This bit is latched-high.
0	SLEEP_STATUS	R	0h	If set, PHY has entered Sleep state

7.5.1.38 WAKE_SLEEP_CONFIG register

Table 315. WAKE_SLEEP_CONFIG register - Wake sleep configuration register (address 8182h)[1]

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15:14	FUNCTION_SELECT	RW		Wakeup sleep function selection register This setting is preserved during deep sleep. This setting is configuration protected.
			00	No Wake-Sleep functionality
			01	Basic Wake-Sleep functionality
			10*	TC10 Wake-Sleep functionality
			11	Reserved
13:12	*reserved*	RW	0h	Always write 00, ignore on read.
11	WU_IO_ENABLE	RW	0h	If set, wake-up the PHY on WAKE_IN_OUT pin assertion This setting is preserved during deep sleep. This setting is configuration protected.
10	WU_SMI_ENABLE	RW	0h	If this bit is set to one, this PHY wakes up when the system wake-up WU_SMI bit is asserted in register ALWAYS_ACCESSIBLE. This setting is preserved during deep sleep. This setting is configuration protected.
9	FWD_WU_PHY_TO_WU_IO	RW	0h	If set, the PHY forwards a wake request by WAKE_REQUEST_PHY control bit to WAKE_IN_OUT This setting is preserved during deep sleep. This setting is configuration protected.
8	FWD_WUPWUR_TO_WU_IO	RW	0h	If set, a WUP/WUR requests received on MDI by this PHY is forwarded to the device WAKE_IN_OUT pin This setting is preserved during deep sleep. This setting is configuration protected.
7:6	*reserved*	R	0h	Always write 00, ignore on read.
5	SLEEP_SILENT_CHECK	RW	1h	If set, sleep responder waits for the initiator to become silent before entering SLEEP_SILENT. This setting is preserved during deep sleep. This setting is configuration protected.
4	WUR_IN_SEND_LPS	RW	1h	If this bit is set to zero, a wake-up request during SEND_LPS will never be serviced directly but be stored and serviced after the sleep request procedure completes, successful or not. If this bit is set to one, a wake-up request occuring during SEND_LPS before either PHY has become SILENT, will cause a WUR to be transmitted. Note that this WUR will imply discontinuation of the LPS sequence. This WUR provides fastest forwarding of the wake-up event and stops the sleep request if possible. If the sleep process wasn't stopped by the WUR, the pending wake-up will be serviced after the sleep request process completes. This setting is preserved during deep sleep. This setting is configuration protected.

Table 315. WAKE_SLEEP_CONFIG register - Wake sleep configuration register (address 8182h)[1]*...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
3	AUTO_REJECT	RW	0h	If set, a sleep request is automatically rejected on SLEEP_ACK_TIMER expiration. Otherwise, sleep requests are auto-accepted by the responder on SLEEP_ACK_TIMER expiration (TC10) This setting is preserved during deep sleep. This setting is configuration protected.
2	AUTO_SLEEP_ON_IDLE	RW	0h	If set, long idle autonomous sleep request enabled This setting is preserved during deep sleep. This setting is configuration protected.
1	AUTO_SLEEP_ON_SILENCE	RW	1h	If set, a follower automatically returns to SLEEP after wake-up if no signal is received from the leader This setting is preserved during deep sleep. This setting is configuration protected.
0	NO_AUTO_ON_WAKE	RW	0h	If set, the PHY pauses in "active STANDBY" after wake-up until the START_OPERATION bit is set. Otherwise, the PHY autonomously proceeds to normal mode after wake-up. This setting is preserved during deep sleep. This setting is configuration protected.

[1] This register can only be changed if CONFIG_ENABLE or SUPER_CONFIG_ENABLE are set to 1.

7.5.1.39 WAKE_SLEEP_PARAMETERS register

Table 316. WAKE_SLEEP_PARAMETERS register - Wake sleep parameters register (address 8184h)[1]

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	*reserved*	R	0h	Always write 0, ignore on read.
14:12	SLEEP_ACK_TIMER	RW		Timer for auto accept (or reject) sleep request This setting is preserved during deep sleep. This setting is configuration protected.
			0h	0 us
			1h	250 us
			2h	500 us
			3h	1 ms
			4h	2 ms
			5h	4 ms
			6h*	8 ms
			7h	12 ms
11	*reserved*	R	0h	Always write 0, ignore on read.
10:8	AUTO_SLEEP_IDLE_TIMER	RW		Auto sleep idle timer This setting is preserved during deep sleep. This setting is configuration protected.

Table 316. WAKE_SLEEP_PARAMETERS register - Wake sleep parameters register (address 8184h)[1]*...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
			0h	125 ms
			1h	250 ms
			2h	500 ms
			3h*	1 s
			4h	2 s
			5h	4 s
			6h	8 s
			7h	16 s
7	*reserved*	R	0h	Always write 0, ignore on read.
6:4	AUTO_SLEEP_ SILENCE_TIMER	RW		Auto sleep silence timer This setting is preserved during deep sleep. This setting is configuration protected.
			0h	125 ms
			1h	250 ms
			2h	500 ms
			3h*	1 s
			4h	2 s
			5h	4 s
			6h	8 s
			7h	16 s
3	*reserved*	R	0h	Always write 0, ignore on read.
2:0	MIN_SILENT_ TIMER	RW		Minimum duration of SLEEP_SILENT state. This setting is preserved during deep sleep. This setting is configuration protected.
			0h	125 us
			1h	250 us
			2h	500 us
			3h*	1 ms
			4h	2 ms
			5h	4 ms
			6h	8 ms
			7h	16 ms

[1] This register can only be changed if CONFIG_ENABLE or SUPER_CONFIG_ENABLE are set to 1.

7.5.1.40 EPHY_LED_TRIGGER0 register

Table 317. EPHY_LED_TRIGGER0 register - Ethernet PHY LED trigger output 0 register (address 8190h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	1h	If set, trigger is enabled
14:4	*reserved*	R	0h	Always write all 0s, ignore on read.
3:0	FUNCTION	RW		LED trigger function selection
			0h*	Link_availability
			1h	Link_status
			2h	Role: Leader(1) or Follower(0)
			3h	PHY Active (AFE running)
			4h	Frame reception (RX_DV=1)
			5h	Symbol errors
			6h	Frame/test transmission (TX_EN=1)
			7h	Frame activity (RX or TX)
			others	reserved

7.5.1.41 EPHY_LED_TRIGGER1 register

Table 318. EPHY_LED_TRIGGER1 register - Ethernet PHY LED trigger output 1 register, see EPHY_LED_TRIGGER0 (address 8191h)

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	1h	If set, trigger is enabled
14:4	*reserved*	R	0h	Always write all 0s, ignore on read.
3:0	FUNCTION	RW	TJF1103A: 0h	LED trigger function selection, see EPHY_LED_TRIGGER0
			TJF1103B: 4h	

7.5.1.42 EPHY_LED_TRIGGER2 register

Table 319. EPHY_LED_TRIGGER2 register - Ethernet PHY LED trigger output 2 register, see EPHY_LED_TRIGGER0 (address 8192h)

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	1h	If set, trigger is enabled
14:4	*reserved*	R	0h	Always write all 0s, ignore on read.
3:0	FUNCTION	RW	TJF1103A: 0h	LED trigger function selection, see EPHY_LED_TRIGGER0
			TJF1103B: 6h	

7.5.1.43 EPHY_LED_TRIGGER3 register

Table 320. EPHY_LED_TRIGGER3 register - Ethernet PHY LED trigger output 3 register, see EPHY_LED_TRIGGER0 (address 8193h)

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	TJF1103A: 1h	If set, trigger is enabled
			TJF1103B: 0h	
14:4	*reserved*	R	0h	Always write all 0s, ignore on read.
3:0	FUNCTION	RW	0h	LED trigger function selection, see EPHY_LED_TRIGGER0

7.5.1.44 TXC_STATUS register

Table 321. TXC_STATUS register - TXC status register (address 8319h)

Bit	Symbol	Access	Value	Description
15	HIGH_FQ_EVENT	RW	0h	If set, Ratio between the TXC and FRO frequencies was too high. Write one to clear. This bit is latched-high.
14	LOW_FQ_EVENT	RW	0h	If set, Ratio between the TXC and FRO frequencies was too low. Write one to clear. This bit is latched-high.
13	HIGH_FQ_NOW	R	0h	If set, Ratio of TXC and FRO frequencies is too high
12	LOW_FQ_NOW	R	0h	If set, Ratio of TXC and FRO frequencies is too low
11	CLK_PRESENT	R	0h	If set, TXC PRESENT
10:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.5.1.45 RXC_STATUS register

Table 322. RXC_STATUS register - RXC status register (address 831Ah)

Bit	Symbol	Access	Value	Description
15	HIGH_FQ_EVENT	RW	0h	If set, Ratio between the RXC and FRO frequencies was too high. Write one to clear. This bit is latched-high.
14	LOW_FQ_EVENT	RW	0h	If set, Ratio between the RXC and FRO frequencies was too low. Write one to clear. This bit is latched-high.
13	HIGH_FQ_NOW	R	0h	If set, Ratio of RXC and FRO frequencies is too high
12	LOW_FQ_NOW	R	0h	If set, Ratio of RXC and FRO frequencies is too low
11	CLK_PRESENT	R	0h	If set, RXC PRESENT
10:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.5.1.46 SGMII_LATENT_STATUS register

Table 323. SGMII_LATENT_STATUS register - SGMII latent fault status register (address 831Bh)

Bit	Symbol	Access	Value	Description
15	TXPLL_STATUS	RW	0h	SGMII TX PLL latent fault event detected at startup. Write one to clear. This bit is latched-high.
14	RXPLL_STATUS	RW	0h	SGMII RX PLL latent fault event detected at startup. Write one to clear. This bit is latched-high.
13:11	*reserved*	R	0h	Always write 000, ignore on read.
10	LINK_STATUS	RW	0h	SGMII LINK latent fault detected at startup. Write one to clear. This bit is latched-high.
9:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.5.1.47 EPHY_LATENT_STATUS register

Table 324. EPHY_LATENT_STATUS register - Ethernet PHY latent fault status register (address 831Ch)

Bit	Symbol	Access	Value	Description
15	PLL_STATUS	RW	0h	EPHY PLL Latent Fault. Write one to clear. This bit is latched-high.
14	*reserved*	RW	0h	Always write 0, ignore on read.
13	LOC_RCVR_ STATUS	RW	0h	EPHY LOC RCVR latent fault detected at startup. Write one to clear. This bit is latched-high.
12	REM_RCVR_ STATUS	RW	0h	EPHY REM RCVR latent fault detected at startup. Write one to clear. This bit is latched-high.
11	SCR_STATUS	RW	0h	EPHY SCR latent fault detected at startup. Write one to clear. This bit is latched-high.
10	LINK_STATUS	RW	0h	EPHY LINK latent fault detected at startup. Write one to clear. This bit is latched-high.
9:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.5.1.48 SGMII_CLK_STATUS register

Table 325. SGMII_CLK_STATUS register - SGMII clock status register (address 831Dh)

Bit	Symbol	Access	Value	Description
15	HIGH_FQ_EVENT	RW	0h	If set, Ratio of TCLK and REFCLK frequencies has been too high. Write one to clear. This bit is latched-high.

Table 325. SGMII_CLK_STATUS register - SGMII clock status register (address 831Dh)*...continued*

Bit	Symbol	Access	Value	Description
14	LOW_FQ_EVENT	RW	0h	If set, Ratio of TCLK and REFCLK frequencies has been too low. Write one to clear. This bit is latched-high.
13	HIGH_FQ_NOW	R	0h	If set, Ratio of TCLK and REFCLK frequencies is too high
12	LOW_FQ_NOW	R	0h	If set, Ratio of TCLK and REFCLK frequencies is too low
11	CLK_PRESENT	R	0h	If set, SGMII CLK PRESENT
10:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.5.1.49 EPHY_CLK_STATUS register

Table 326. EPHY_CLK_STATUS register - Ethernet PHY clock status (address 831Eh)

Bit	Symbol	Access	Value	Description
15	HIGH_FQ_EVENT	RW	0h	If set, Ratio of TCLK and REFCLK frequencies has been too high. Write one to clear. This bit is latched-high.
14	LOW_FQ_EVENT	RW	0h	If set, Ratio of TCLK and REFCLK frequencies has been too low. Write one to clear. This bit is latched-high.
13	HIGH_FQ_NOW	R	0h	If set, Ratio of TCLK and REFCLK frequencies is too high
12	LOW_FQ_NOW	R	0h	If set, Ratio of TCLK and REFCLK frequencies is too low
11	CLK_PRESENT	R	0h	If set, ePHY CLK PRESENT
10:0	*reserved*	R	0h	Always write all 0s, ignore on read.

7.5.1.50 SIGNAL_QUALITY register

Table 327. SIGNAL_QUALITY register - Signal quality (address 8320h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	*reserved*	RW	0h	Always write 0, ignore on read.
14	VALID	R	0h	If set, the SQI value is valid
13:11	*reserved*	R	0h	Always write 000, ignore on read.
10:8	SQI_WARN_LIMIT	RW		SQI warning threshold. Exceeding the warn limit (SQI value is below the programmed value) will fire an SQI_WARN_IRQ This setting is preserved during deep sleep.
			000*	no warn limit
			001	class A SQI limit
			010	class B SQI limit
			011	class C SQI limit

Table 327. SIGNAL_QUALITY register - Signal quality (address 8320h)*...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
			100	class D SQI limit
			101	class E SQI limit
			110	class F SQI limit
			111	class G SQI limit
7	*reserved*	R	0h	Always write 0, ignore on read.
6:4	SQI_WORST	R	7h	Lowest SQI level sinse last cleared. Reading sets the value to the current SQI level. This bit is latched-low.
3	*reserved*	R	0h	Always write 0, ignore on read.
2:0	SQI	R	0h	Current SQI level

7.5.1.51 MSE register

Table 328. MSE register - Mean-square error register (address 8324h)

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	0h	If set, the MSE is calculated. Otherwise, MSE reports zeros. This setting is preserved during deep sleep.
14:12	*reserved*	R	0h	Always write 000, ignore on read.
11:4	MSE	R	0h	Mean-square value of slicer error
3:0	*reserved*	R	0h	Always write 0000, ignore on read.

7.5.1.52 MAX_MSE register

Table 329. MAX_MSE register - Max mean-square error register (address 8325h)

Bit	Symbol	Access	Value	Description
15:12	*reserved*	R	0h	Ignore on read.
11:4	MAX_MSE	R	0h	The MAX_MSE tracks the peak MSE value. This field is cleared on read. MSE values while the PHY is in SEND_IDLE_OR_DATA. During all other PHY states this register value will be preserved. This flag is cleared on read. This bit is latched-high.
3:0	*reserved*	R	0h	Ignore on read.

7.5.1.53 CABLE_TEST register

Table 330. CABLE_TEST register - Cable test register (address 8330h)

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
15	ENABLE	RW	0h	If set, Cable test functionality enabled

Table 330. CABLE_TEST register - Cable test register (address 8330h) *...continued*

*Legend: *reset value*

Bit	Symbol	Access	Value	Description
14	START	RW		Start This bit is self-clearing.
			0*	Writing a zero stops a running test. Reading a zero indiciates a completed, stopped or not-started condition.
			1	On write, a cable test is initiated. On read it is indicated that the test is still running.
13	VALID	R	0h	If set, test results are available and valid
12:3	*reserved*	R	0h	Always write all 0s, ignore on read.
2:0	FAULT_TYPE	R		Fault type
			000*	No cabling fault detected
			001	Shorted pair
			010	Open pair
			111	Unable to detect
			others	Reserved

7.5.1.54 LINK_TRAINING_TIMER register

Table 331. LINK_TRAINING_TIMER register - Link training timer register (address 8340h)

Bit	Symbol	Access	Value	Description
15:12	*reserved*	R	0h	Ignore on read.
11:4	TIME_MS	R	0h	This value returns the time in ms and saturates at 251ms. If invalid, 255 is returned. The meassurement is started when the PHY initially enters FOLLOWER_SILENT and stopped when LINK_AVAILABILITY=1.
3:1	TIME_SUBMS	R	0h	Fractional part in multiples of 125us
0	*reserved*	R	0h	Ignore on read.

7.5.1.55 LOC_RCVR_STATUS_TIMER register

Table 332. LOC_RCVR_STATUS_TIMER register - Local receiver status timer register (address 8341h)

Bit	Symbol	Access	Value	Description
15:12	*reserved*	R	0h	Ignore on read.
11:4	TIME_MS	R	0h	This value returns the time in ms and saturates at 251ms. If invalid, 255 is returned. The meassurement is started when the PHY initially enters FOLLOWER_SILENT and stopped when LOC_RCVR_STATUS=1.
3:1	TIME_SUBMS	R	0h	Fractional part in multiples of 125us
0	*reserved*	R	0h	Ignore on read.

7.5.1.56 REM_RCVR_STATUS_TIMER register

Table 333. REM_RCVR_STATUS_TIMER register - Remote receiver status timer register (address 8342h)

Bit	Symbol	Access	Value	Description
15:12	*reserved*	R	0h	Ignore on read.
11:4	TIME_MS	R	0h	This value returns the time in ms and saturates at 251ms. If invalid, 255 is returned. The meassurement is started when the PHY initially enters FOLLOWER_SILENT and stopped when REM_RCVR_STATUS=1.
3:1	TIME_SUBMS	R	0h	Fractional part in multiples of 125us
0	*reserved*	R	0h	Ignore on read.

7.5.1.57 FOLLOWER_SILENT_TIMER register

Table 334. FOLLOWER_SILENT_TIMER register - Follower silent timer register (address 8343h)

Bit	Symbol	Access	Value	Description
15:12	*reserved*	R	0h	Ignore on read.
11:4	TIME_MS	R	0h	This value returns the time in ms and saturates at 251ms. The meassurement is started when the PHY initially enters FOLLOWER_SILENT and ends when the PHY transitions to TRAINING.
3:1	TIME_SUBMS	R	0h	Fractional part in multiples of 125us
0	*reserved*	R	0h	Ignore on read.

7.5.1.58 SYMBOL_ERROR_COUNTER register

Table 335. SYMBOL_ERROR_COUNTER register - Symbol error counter register (address 8350h)

Bit	Symbol	Access	Value	Description
15:0	SYMBOL_ERRORS	R	0h	This register counts symbol errors when LINK_AVAILABLE=1 and ERROR_COUNTER_MISC[COUNTERS_ENABLE]=1. When reaching its maximum value, this register does not saturate, but automatically rolls-over to zero. The value does not get reset by link retraining, but does not increment while LINK_AVAILABLE=0. The counter is reset when the counter is disabled (COUNTER_ENABLE=0), during a power-cycle, when inhibit is de-asserted, on PHY_CONTROL[RESET] or MMD1.PMA_CONTROL1[RESET]

7.5.1.59 ERROR_COUNTER_MISC register

Table 336. ERROR_COUNTER_MISC register - Error counter miscellaneous register (address 8352h)

Bit	Symbol	Access	Value	Description
15	COUNTER_ENABLE	RW	1h	If set, the SYM_ERRORS, LINK_AVAILABLE_DROPS, LINK_STATUS_DROPS, LINK_FAILURES and LINK_LOSSES counters are enabled. This setting is preserved during deep sleep.

Table 336. ERROR_COUNTER_MISC register - Error counter miscellaneous register (address 8352h)*...continued*

Bit	Symbol	Access	Value	Description
14	*reserved*	R	0h	Always write 0, ignore on read.
13:8	LINK_STATUS_DROPS	R	0h	This register counts how many times the non-latched LINK_STATUS bit has dropped unintentionally. The value saturates at max value. The counter is reset when the counter is disabled (COUNTER_ENABLE=0), during a power-cycle, when inhibit is de-asserted, on PHY_CONTROL[RESET] or MMD1.PMA_CONTROL1[RESET]
7:6	*reserved*	R	0h	Always write 00, ignore on read.
5:0	LINK_AVAILABLE_DROPS	R	0h	This register counts the number of times that LINK_AVAILBILITY has dropped unintentionally. The value saturates at max value. The counter is reset when the counter is disabled (COUNTER_ENABLE=0), during a power-cycle, when inhibit is de-asserted, on PHY_CONTROL[RESET] or MMD1.PMA_CONTROL1[RESET]

7.5.1.60 LINK_LOSSES_AND_FAILURES register

Table 337. LINK_LOSSES_AND_FAILURES register - Link losses and failures counter register (address 8353h)

Bit	Symbol	Access	Value	Description
15:10	LINK_LOSSES	R	0h	A link loss is counted when the LOC_RCVR_STATUS becomes 0 and the PHY will go through a full training.
9:0	LINK_FAILURES	R	0h	If COUNTER_ENABLED is set, this counter counts the number of link failures that do not cause a link drop. This includes SSD and ESD errors, as well as transmitting SEND_I when the REM_RCVR_STATUS=0 and LOC_RCVR_STATUS=1. Note that symbol errors in an idle sequence are covered by the symbol error counter and not counted as link failure. The value saturates at max value. The counter is reset when the counter is disabled (COUNTER_ENABLE=0), during a power-cycle, when inhibit is de-asserted, on PHY_CONTROL[RESET] or MMD1.PMA_CONTROL1[RESET]

7.5.1.61 PHY_COMPLIANCE_TEST register

Table 338. PHY_COMPLIANCE_TEST register - PHY compliance test control register (address 83F0h)

Bit	Symbol	Access	Value	Description
15:1	*reserved*	R	0h	Always write all 0s, ignore on read.
0	TX_TCLK_EN	RW	0h	If enabled, the PHY provides the transmit clock for jitter test on an external pin. This setting is configuration protected.

8 Thermal characteristics

Table 339. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board[1].

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		38	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	[2]	14	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package		8	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 µm)

[2] Case temperature refers to the center of the heatsink at the bottom of the package.

9 Limiting values

Table 340. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are defined with respect to ground unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	Voltage on pin x	on pins MDC, INT_N, RST_N, INH, WAKE_IN_OUT, GPIOx, RX_ER, RX_CTL, RXDx, RXC, TX_ER, TXC, TX_CTL, TXDx, MDIO	–0.5	+4	V
		on pins XI, XO	–0.5	+1.6	V
		on pins TRX_P, TRX_M	–0.5	+4	V
		on pins SIN, SIP, SOP, SON	–0.5	+1.6	V
		on pin VDDIO	–0.5	+4	V
		on pin VDD_CORE	–0.5	+1.6	V
		on pin VREGA_OUT	–0.5	+4	V
		on pin VDDA_AO	–0.5	+4	V
		on pin VREGD_IN, VREGA_IN	–0.5	+4	V
		on pins VDDA_TRX	–0.5	+4	V
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM)			
		on any pin	–2	+2	kV
		on pins TRX_P, TRX_M to GND [1]	–4	+4	kV
		Charge Device Model (CDM)			
		on all pins	–500	+500	V
T_{vj}	virtual junction temperature	[2]	–40	+125	°C
T_{stg}	storage temperature	[3]	–55	+125	°C
T_{amb}	ambient temperature	[4]	–40	+105	°C

[1] Pins stressed to GND, emulating the application circuits.
[2] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is the thermal resistance from virtual junction to ambient of the device (see Table 339) and P is the customer-application-controlled power dissipation. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
[3] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.
[4] Specification for virtual junction temperature T_{vj} is leading, i.e., maximum ambient temperature of 105 °C can only be sustained if self-heating through power dissipation is ≤ 25 °C.

10 Static characteristics

Table 341. Static characteristics

T_{vj} = –40 °C to + 125 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC. [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power supply						
V_{DD}	supply voltage	on pin VDDIO, 1.8 V signaling	1.65	1.8	1.95	V
		on pin VDDIO, 2.5 V signaling	2.25	2.5	2.75	V
		on pin VDDIO, 3.3 V signaling	3	3.3	3.6	V
		on pin VDD_CORE if VREGD is bypassed and VREGD_IN is connected to VDD_CORE.	1.045	1.1	1.155	V
		on pin VDDA_AO, 3.3 V operation [2]	3.135	3.3	3.465	V
		on pin VDDA_AO, 2.5 V operation	2.375	2.5	2.625	V
		on pin VREGD_IN, if integrated VREGD LDO is enabled, 3.3 V operation	3.135	3.3	3.465	V
		on pin VREGD_IN, if integrated VREGD LDO is enabled, 2.5 V operation	2.375	2.5	2.625	V
		on pin VREGA_IN, if integrated VREGA LDO is enabled	3.135	3.3	3.465	V
		on pins VDDA_TRX if VREGA is bypassed and VREGA_IN is connected to VDDA_TRX.	2.375	2.5	2.625	V
		on pins VDDA_SI, VDDA_SO	1.045	1.1	1.155	V
Current consumption (single supply mode) [3][4]						
$I_{DD(RMS)}$	RMS supply current	on pin VDD_CORE [5]	—	0	0	mA
		on pin VREGA_IN mode DEVICE_OPERATIONAL [6]	—	22	27	mA
		on pin VREGA_IN mode DEVICE_STANDBY [6]	—	1	1	mA
		on pin VREGD_IN; TJF1103A				
		mode DEVICE_OPERATIONAL 100BASE-T1 LEADER mode 100BASE-T1 link-up	—	17	37	mA
		mode DEVICE_OPERATIONAL 100BASE-T1 FOLLOWER mode 100BASE-T1 link-up	—	17	37	mA
		mode DEVICE_STANDBY	—	2	15	mA

Table 341. Static characteristics...*continued*

T_{vj} = –40 °C to + 125 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC. [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		mode DEVICE_SLEEP [7]	—	2	15	mA
		on pin VREGD_IN; TJF1103B				
		mode DEVICE_OPERATIONAL 100BASE-T1 LEADER mode 100BASE-T1 link-up and SGMII link-up	—	52	62	mA
		mode DEVICE_OPERATIONAL 100BASE-T1 FOLLOWER mode 100BASE-T1 link-up and SGMII link-up	—	52	62	mA
		mode DEVICE_OPERATIONAL 100BASE-T1 LEADER or FOL LOWER mode 100BASE-T1 link-up and SGMII link-down	—	30	42	mA
		mode DEVICE_STANDBY SGMII link-up	—	26	32	mA
		mode DEVICE_SLEEP [7] SGMII link-down	—	11	18	mA
		mode DEVICE_STANDBY 100BASE-T1 link-down and SGMII link-down	—	13	22	mA
Current consumption (individual supply mode)[3][4]						
$I_{DD(RMS)}$	RMS supply current	on pin VREGD_IN [8]	—	—	0	mA
		on pin VDDA_TRX; TJF1103A				
		mode DEVICE_OPERATIONAL	—	15	17	mA
		mode DEVICE_STANDBY	—	0.01	0.3	mA
		mode DEVICE_SLEEP	—	0.01	0.3	mA
		on pin VDD_CORE; TJF1103A				
		mode DEVICE_OPERATIONAL 100BASE-T1 LEADER mode 100BASE-T1 link-up	—	16	37	mA
		mode DEVICE_OPERATIONAL 100BASE-T1 FOLLOWER mode 100BASE-T1 link-up	—	16	37	mA
		mode DEVICE_STANDBY	—	2	15	mA
		mode DEVICE_SLEEP	—	2	15	mA
		on pin VDDA_TRX; TJF1103B				
		mode DEVICE_OPERATIONAL	—	17	19	mA
		mode DEVICE_STANDBY	—	0.25	0.35	mA

Table 341. Static characteristics...*continued*

T_{vj} = –40 °C to + 125 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC. [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		mode DEVICE_SLEEP	—	0.25	0.35	mA
		on pin VDD_CORE; TJF1103B				
		mode DEVICE_OPERATIONAL 100BASE-T1 LEADER mode 100BASE-T1 link-up	—	22	30	mA
		mode DEVICE_OPERATIONAL 100BASE-T1 FOLLOWER mode 100BASE-T1 link-up	—	22	30	mA
		mode DEVICE_STANDBY	-	10	20	mA
		mode DEVICE_SLEEP	—	10	20	mA
		on pin VDDA_SI; SGMII link-up; (TJF1103B only)	—	—	25	mA
		on pin VDDA_SO; SGMII link-up (TJF1103B only)	—	—	15	mA
Current consumption (IO) on pins VDDIO; 3.3 V VDDIO[3][4][9]						
$I_{DD(RMS)}$	RMS supply current	MII mode; frame size 1500 bytes; default IO settings; payload pattern 0xA5 [10]	—	—	14	mA
		RMII mode; frame size 1500 bytes; default IO settings; payload pattern 0xCC [10]	—	—	4	mA
		RGMII mode; frame size 1500 bytes; default IO settings; payload pattern 0xA5 [10]	—	—	9	mA
		MII mode; frame size 128 bytes; PRBS pattern; default IO settings; 25°C ambient [10]	—	14	—	mA
		RMII mode; frame size 128 bytes; PRBS pattern; default IO settings; 25°C ambient [10]	—	2	—	mA
		RGMII mode; frame size 128 bytes; PRBS pattern; default IO settings; 25°C ambient [10]	—	7	—	mA
Current consumption (other pins)[3]						
$I_{DD(RMS)}$	RMS supply current	on pin VDDA_AO	—	—	1	mA
I_{sleep}	sleep current	on pin VDDA_AO; device mode DEVICE_DEEP_SLEEP [11]				
		TJF1103A	—	—	35	µA
		TJF1103B	—	20	55	µA
Integrated LDO (VREGD)						
V_O	output voltage	on pin VDD_CORE	1.078	1.1	1.137	V

Table 341. Static characteristics...*continued*

T_{vj} = –40 °C to + 125 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC. [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_O	output current	on pin VDD_CORE	—	50	65	mA
$V_{th(act)}$	regulator activation threshold	on pin VREGD_IN [3] Below the activation threshold, the device expects a supply connected directly to VDD_CORE	2.26	—	—	V
I_{PD}	power-down current	LDO disabled [3]	1	—	30	uA
Integrated LDO (VREGA)						
V_O	output voltage	on pin VREGA_OUT	2.437	2.5	2.59	V
I_O	output current	on pin VREGA_OUT	—	—	25	mA
$V_{th(act)}$	regulator activation threshold	on pin VREGA_IN [3] Below the activation threshold, the device expects a supply connected directly to VDDA_TRX	3.0	—	—	V
Digital I/O pins[12]						
V_{IH}	HIGH-level input voltage	3.3, 2.5, 1.8 V signaling [13]	0.7 × V_{DDIO}	—	—	V
V_{IL}	LOW-level input voltage	3.3, 2.5, 1.8 V signaling	—	—	0.3 × V_{DDIO}	V
V_{OH}	HIGH-level output voltage	3.3 V signaling; I_{OH} = –2 mA	V_{DDIO}– 0.4	—	—	V
		2.5 V signaling; I_{OH} = –2 mA	V_{DDIO} -–0.4	—	—	V
		1.8 V signalings; I_{OH} = –2 mA	V_{DDIO} -–0.4	—	—	V
V_{OL}	LOW-level output voltage	3.3 V signaling; I_{OL} = 2 mA	—	—	0.4	V
		2.5 V signaling; I_{OL} = 2 mA	—	—	0.4	V
		1.8 V signaling; I_{OL} = 2 mA	—	—	0.4	V
C_i	input capacitance	[3]	—	—	5.0	pF
V_{hys}	input hysteresis voltage	[3]	0.1 × V_{DDIO}	—	—	V
I_{OSH}	HIGH-level short-circuit output current	[3]	—	—	144	mA
I_{OSL}	LOW-level short-circuit output current	[3]	—	—	144	mA
I_{IL}	HIGH-level input current	V_{IL}= $V_{DD(IO)}$ internal pull-up or pull-down disabled	—	—	10	uA
I_{IH}	LOW-level input current	V_{IL}=0 V internal pull-up or pull-down disabled	–10	—	—	uA
R_{pd}	pull-down resistance		40	50	62	kΩ
R_{pu}	pull-up resistance		40	50	62	kΩ

Table 341. Static characteristics...*continued*

T_{vj} = –40 °C to + 125 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC. [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R	output impedance	Default register settings. VDDIO = 3.3 V [3]				
		TJF1103A	—	65	—	Ω
		TJF1103B	—	50	—	Ω
		Default register settings. VDDIO = 2.5 V [3]				
		TJF1103A	—	55	—	Ω
		TJF1103B	—	50	—	Ω
		Default register settings. VDDIO = 1.8 V [3]				
		TJF1103A	—	45	—	Ω
		TJF1103B	—	50	—	Ω
SGMII[3]						
$\lvert V_{o(dif)} \rvert$	differential output voltage (absolute value)	R_L = 100 Ω	150	—	400	mV
$R_{term(se)}$	single-ended termination resistance		—	50	—	Ω
$V_{ring(o)}$	ringing voltage		—	—	0.1 × Vo(dif)	V
$Z_{o(se)}$	single-ended output impedance		40	—	140	Ω
$\Delta Z_{o(se)}$	single-ended output impedance mismatch		—	—	10	%
$\lvert \Delta_{Vo(dif)} \rvert$	differential output voltage difference	change in differential output voltage between complementary output states R_L = 100 Ω	—	—	25	mV
ΔV_{cm}	common-mode voltage difference	change in output offset voltage between complementary output states R_L = 100 Ω	—	—	25	mV
$V_{th(i)dif}$	differential input threshold voltage		–50	—	50	mV
$Z_{i(dif)RX}$	receiver differential input impedance		80	100	120	Ω
100BASE-T1[3]						
$\lvert V_{o(dif)} \rvert$	differential output voltage (absolute value)	load 100 Ω meassured at MDI	—	—	2.2	V
R_{term}	termination resistance		—	100	—	Ω
Oscillator[3]						
C_i	input capacitance	on pin XI	—	2	—	pF
C_L	load capacitance	[14]	—	8	—	pF
$V_{i(p-p)}$	input voltage	on pin XI for externally connected AC-coupled clock.	0.8	—	1.21	V_{pp}

Table 341. Static characteristics...*continued*

T_{vj} = –40 °C to + 125 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC. [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		C_{AC}=100 pF				
Voltage monitors						
V_{uvd}	undervoltage detection voltage	on pin VDD_CORE	0.99	—	—	V
		on pins VDDA_TRX	2.25	—	—	V
V_{uvr}	undervoltage recovery voltage	on pins VDDA_TRX	—	—	2.38	V
V_{ovd}	overvoltage detection voltage	on pin VDD_CORE	—	—	1.21	V
		on pins VDDA_TRX	—	—	2.75	V
		on pin VREGA_IN	—	—	3.63	V
		on pin VREGD_IN	—	—	3.63	V
V_{ovr}	overvoltage recovery voltage	on pins VDDA_TRX	2.63	—	—	V
		on pin VREGA_IN	3.47	—	—	V
		on pin VREGD_IN	3.47	—	—	V

[1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.
[2] Note that INH and WAKE_IN_OUT logic levels are according to VDDA_AO
[3] Not measured in production, guaranteed by design.
[4] Typical values for 25 °C and typical operating voltages
[5] When supplied internally, pin VDD_CORE is connected to a bypass capacitor.
[6] VDDA_TRX is supplied through VREGA_OUT
[7] Device in Sleep mode, but VREGD_IN is still supplied.
[8] When supplied externally, pin VREGD_IN is externally connected to VDD_CORE, VDDA_SI and VDDA_SO.
[9] If VDDIO is supplied with a lower voltage, the current is guaranteed to be less than the specified value.
[10] Characterized on a 18.5 cm FR4 trace and 10 kΩ pull-down on RXD2.
[11] At an ambient temperature of 85 °C; supply on pins other than VDDA_AO is expected to be removed in DEVICE_DEEP_SLEEP.
[12] Some pins are input-only or output-only. In this case only the relevant information applies
[13] Pins RST_N, WAKE_IN_OUT and INH are referenced to V_{DDA_AO}; see pinning list for details.
[14] Value of external load capacitors depend on the selected crystal. Consult the TJF1103 Appnote for details.

11 Dynamic characteristics

Table 342. Dynamic characteristics

T_{vj} = –40 °C to + 125 °C; all voltages are defined with respect to ground unless otherwise specified. Not measured in production, guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital I/Os (JTAG, GPIOs)[1]						
t_r	rise time	15 cm PCB transmission line: 50 Ω; 5 pF far-end load. 20% to 80%				
		1.8 V, default IO settings	1.3	—	3.9	ns
		2.5 V, default IO settings	1.5	—	4.26	ns
		3.3 V, default IO settings	2.2	—	4.7	ns
t_f	fall time	15 cm PCB transmission line: 50 Ω; 5 pF far-end load.				

Table 342. Dynamic characteristics...*continued*

T_{vj} = –40 °C to + 125 °C; all voltages are defined with respect to ground unless otherwise specified. Not measured in production, guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		20% to 80%				
		1.8 V, default IO settings	1.3	—	3.9	ns
		2.5 V, default IO settings	1.5	—	4.26	ns
		3.3 V, default IO settings	2.2	—	4.7	ns
Digital I/Os (MDIO, MII, RMII, RGMII)[1]						
t_r	rise time	15 cm PCB transmission line: 50 Ω; 5 pF far-end load. 20% to 80%				
		1.8 V, default IO settings	0.39	—	2	ns
		2.5 V, default IO settings	0.92	—	3.3	ns
		3.3 V, default IO settings	1.2	—	3.6	ns
t_f	fall time	15 cm PCB transmission line: 50 Ω; 5 pF far-end load. 20% to 80%				
		1.8 V, default IO settings	0.39	—	2	ns
		2.5 V, default IO settings	0.92	—	3.3	ns
		3.3 V, default IO settings	1.2	—	3.6	ns
MII transmit timing						
T_{clk}	clock period	on pin TX_CLK	—	40	—	ns
δ	duty cycle	on pin TX_CLK	35	—	65	%
t_{WH}	pulse width HIGH	on pin TX_CLK	—	20	—	ns
t_{WL}	pulse width LOW	on pin TX_CLK	—	20	—	ns
t_{su}	set-up time	from pins TXD[3:0], TX_ER, TX_EN to TX_CLK				
		MII mode	10	—	—	ns
		revMII mode	10	—	—	ns
t_h	hold time	from TX_CLK to TXD[3:0], TX_ER, TX_EN				
		MII mode	0	—	—	ns
		revMII mode	10	—	—	ns
MII receive timing						
T_{clk}	clock period	on pin RX_CLK	—	40	—	ns
δ	duty cycle	on pin RX_CLK	35	—	65	%
t_{WH}	pulse width HIGH	on pin RX_CLK	—	20	—	ns
t_{WL}	pulse width LOW	on pin RX_CLK	—	20	—	ns
t_d	delay time	from RX_CLK to RXD[3:0], RX_ER, RX_DV				

Table 342. Dynamic characteristics...*continued*

T_{vj} = –40 °C to + 125 °C; all voltages are defined with respect to ground unless otherwise specified. Not measured in production, guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		25 pF load default IO settings 15 pF load MII_DATA_IO_CONFIG[ALTERNATE_CONFIG] = 1				
		MII	10	—	25	ns
		revMII	0	—	25	ns
RMII transmit/receive timing						
T_{clk}	clock period	on pin REF_CLK	—	20	—	ns
δ	duty cycle	on pin REF_CLK	35	—	65	%
t_{WH}	pulse width HIGH	on pin REF_CLK	—	10	—	ns
t_{WL}	pulse width LOW	on pin REF_CLK	—	10	—	ns
t_{su}	set-up time	from pins TXD[1:0], TX_EN, TX_ER to REF_CLK	4	—	—	ns
t_h	hold time	from REF_CLK to TXD[1:0], TX_EN, TX_ER	2	—	—	ns
t_d	delay time	from REF_CLK to RXD[1:0], CRSDV, RX_ER 25 pF load default IO settings 15 pF load MII_DATA_IO_CONFIG[ALTERNATE_CONFIG] = 1	2	—	10	ns
RGMII transmit/receive timing						
T_{clk}	clock period	on pin TXC	—	40	—	ns
δ	duty cycle	on pin TXC	40	50	60	%
$t_{sk(o)TX}$	transmitter output skew time	RGMII mode, from pin RXC to RXD[3:0], RX_CTL [2] 25 pF load default IO settings 15 pF load MII_DATA_IO_CONFIG[ALTERNATE_CONFIG] = 1	–500	—	500	ps
$t_{sk(i)RX}$	receiver input skew time	RGMII mode, from pin TXC to TXD[3:0], TX_CTL	1	—	2.6	ns
$t_{su(o)TX}$	transmitter output setup time	RGMII-ID mode, from pins RXD[3:0], RX_CTL to RXC [3] 25 pF load default IO settings 15 pF load MII_DATA_IO_CONFIG[ALTERNATE_CONFIG] = 1	1.2	—	—	ns
$t_{h(o)TX}$	transmitter output hold time	RGMII-ID mode, from pin RXC to RXD[3:0], RX_CTL 25 pF load default IO settings 15 pF load MII_DATA_IO_CONFIG[ALTERNATE_CONFIG] = 1	1.2	—	—	ns
$t_{su(o)RX}$	receiver output setup time	RGMII-ID mode, from pins TXD[3:0], TX_CTL to TXC	1	—	—	ns

Table 342. Dynamic characteristics...*continued*

T_{vj} = –40 °C to + 125 °C; all voltages are defined with respect to ground unless otherwise specified. Not measured in production, guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(o)RX}$	receiver output hold time	RGMII-ID mode, from pin TXC to TXD[3:0], TX_CTL	1	—	—	ns
SGMII						
t_r	rise time	20% to 80%	40	—	200	ps
t_f	fall time	20% to 80%	40	—	200	ps
t_{jit}	jitter time	TIE (Time Interval Error): RMS value	—	—	10	ps
MDIO timing						
T_{clk}	clock period	on pin MDC	50	—	1000	ns
δ	duty cycle	on pin MDC	—	50	—	%
t_{su}	set-up time	from pin MDIO to MDC	10	—	—	ns
t_h	hold time	from pin MDC to MDIO	10	—	—	ns
t_d	delay time	from pin MDC to MDIO	0	—	15	ns
JTAG						
f_{clk}	clock frequency	on pin TCK	0.1	—	25	MHz
δ	duty cycle	on pin TCK	40	50	60	%
t_{su}	set-up time	TJF1103A	4	—	—	ns
		TJF1103B	8	—	—	ns
t_h	hold time		25	—	—	ns
t_{ov}	output valid time		—	—	20	ns
CLK_OUT[4]						
f_{clk}	clock frequency	on pins CLK_OUT	—	25	—	MHz
Δf	frequency deviation	on pins CLK_OUT [5]	–100	—	100	ppm
MDI						
$t_{d,tx}$	transmit latency	Jumbo frames disabled				
		MII from TX_EN to SSD on MDI	145	—	207	ns
		revMII from TX_EN to SSD on MDI	266	—	366	ns
		RMII from TX_EN to SSD on MDI	385	—	486	ns
		RGMII from TX_EN to SSD on MDI	425	—	526	ns
		SGMII /S/ to SSD on MDI	1000	—	1120	ns
$t_{d,rx}$	receive latency	SSD to RX_DV, MII	651	—	808	ns
		SSD to RX_DV, revMII	791	—	987	ns
		SSD to DV_CRS, RMII	831	—	1047	ns
		SSD to TX_EN on RGMII	651	—	807	ns
		SSD to /S/ on SGMII	980	—	1200	ns
Voltage monitor						

Table 342. Dynamic characteristics...*continued*

T_{vj} = –40 °C to + 125 °C; all voltages are defined with respect to ground unless otherwise specified. Not measured in production, guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{uvd(det)}$	undervoltage detection time	from crossing detection level to IRQ generation	—	—	5	ms
$t_{ovd(det)}$	overvoltage detection time	from crossing detection level to IRQ generation	—	—	5	ms
Power-up timing						
dV_{ru}/dt	rate of change of ramp-up voltage	supply ramp up rate; 20 % to 80 %				
		on pin VDD_AO	1	—	35	V/ms
		on pin VDD_CORE	1	—	35	V/ms
		on pin VDDIO	1	—	35	V/ms
		on pin VDDA_SI, VDDA_SO	1	—	35	V/ms
		on pin VREGA_IN	1	—	35	V/ms
		on pin VREGD_IN	1	—	35	V/ms
		on pin VDDA_TRX	1	—	35	V/ms
$t_{init(ps)}$	pin strapping initialization time	from deasserting RST_N pin to completion of pin strapping	—	—	3	ms
Oscillator						
f_{osc}	oscillator frequency		—	25	—	MHz
Δf	frequency deviation	over lifetime and temperature range [6]				
		MII, SGMII	–100	—	100	ppm
		RGMII, RMII [7]	–50	—	50	ppm
Oscillator Follower Mode (external clock)[8]						
δ	duty cycle	on pin XI	45	50	55	%
$t_{jit(i)rms}$	RMS input jitter time	on pin XI				
		TJF1103A	—	—	20	ps
		TJF1103B	—	—	30	ps
Reset						
$t_{det(rst)}$	reset detection time	on pin RST_N	5	—	—	µs

[1] For reference only. Run simulations with the IBIS model and your custom board for accurate results.
[2] Device configured to operate in RGMII mode.
[3] Device configured to operate in RGMII-ID mode, phase shift = 90 °, delay is in the transmitter
[4] CLK_OUT is disabled after device reset
[5] With 100 ppm crystal or clock source connected to XI pin.
[6] The frequency deviation depends on the selected crystal
[7] Device can tolerate a 100 ppm crystal in RGMII/RMII mode, but clock output ppm specifications are not met.
[8] Consult the TJF1103 Application Note for more information on clocking.

12 Timing diagrams

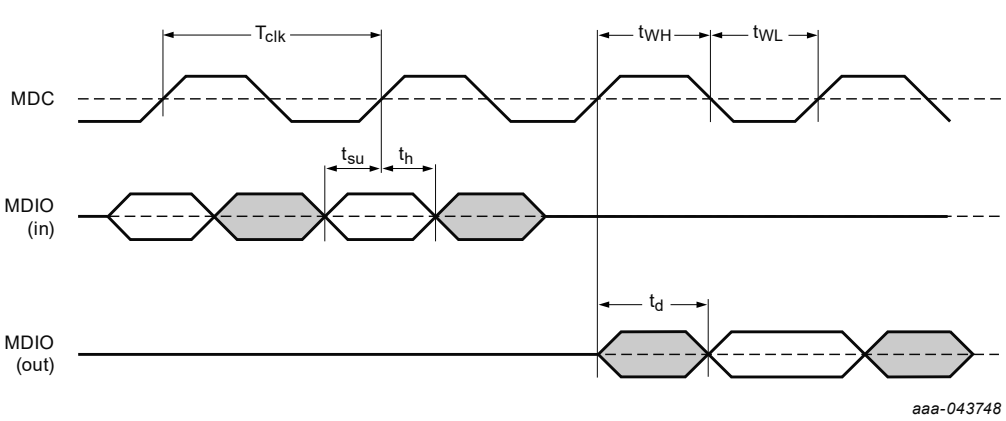


Figure 38. MDIO timing diagram

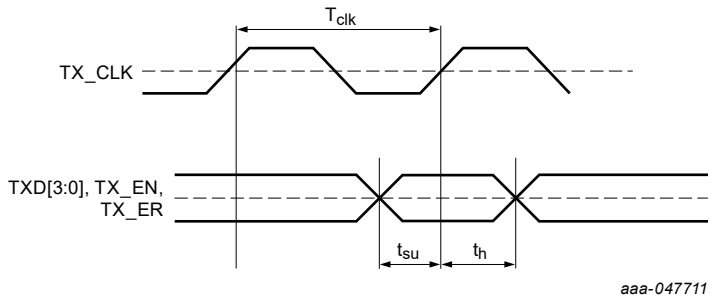


Figure 39. MII transmit timing diagram

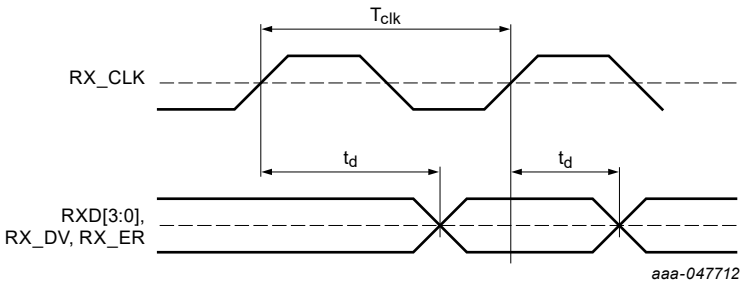


Figure 40. MII receive timing diagram

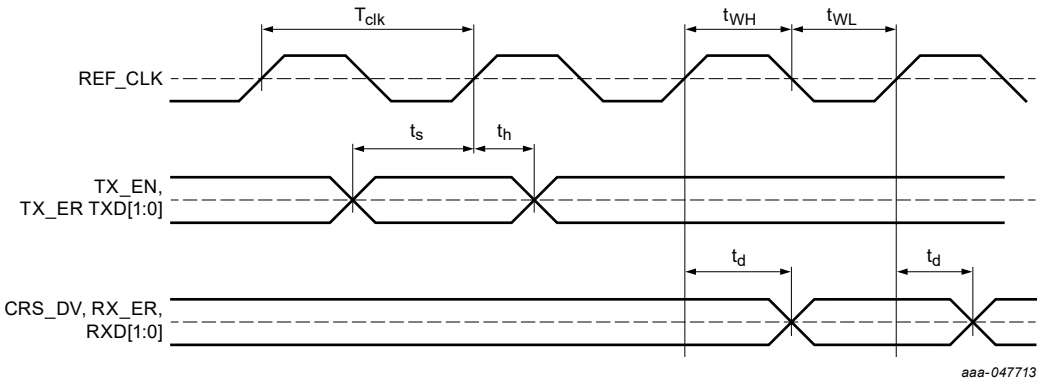


Figure 41. RMII transmit/receive timing diagram

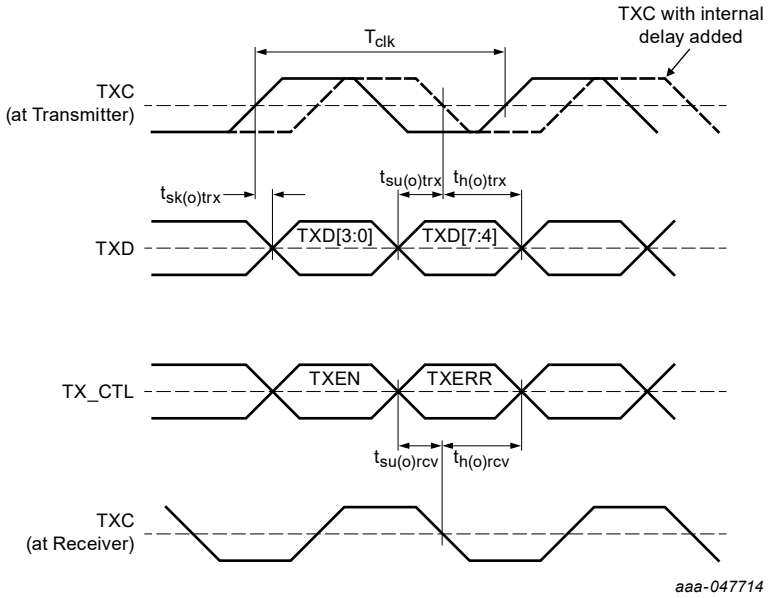


Figure 42. RGMII transmit timing diagram

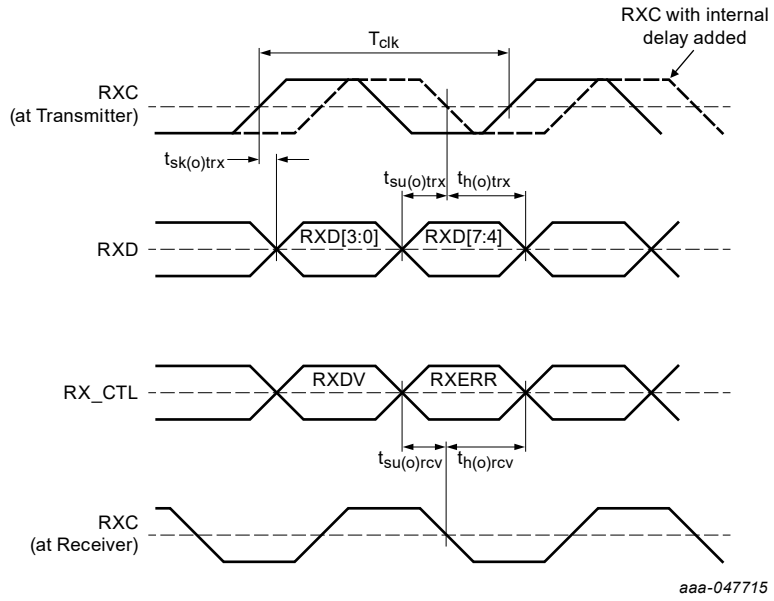


Figure 43. RGMII receive timing diagram

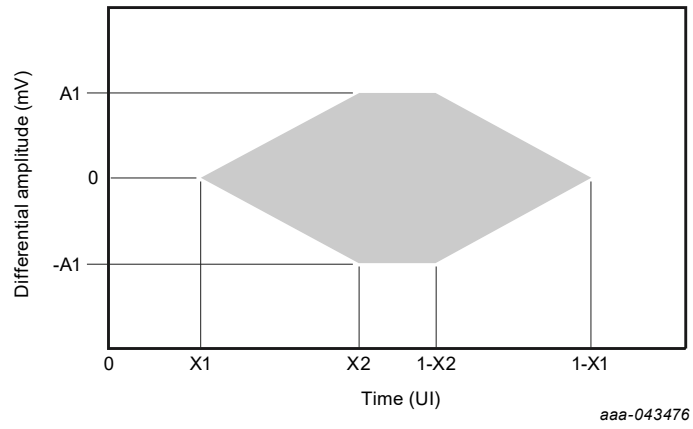


Figure 44. SGMII receiver input compliance mask

Table 343. SGMII receive AC timing specifications

Parameter	Value	Unit
A1	100	mV
X1	0.275	UI
X2	0.400	UI
Eye width	0.45	UI (p-p)
Receiver sensitivity (eye height)	200	mV (p-p)
Deterministic jitter tolerance	0.37	UI (p-p)
Ramdom jitter	12.5	mUI (rms)
Total jitter tolerance	0.55	UI (p-p)

13 Application information

The schematics in Figure 45 to Figure 48 show application examples. See the Application notes for further information.

13.1 Supply

The device can operate with a single 3.3 V supply for reduced PCB estate and low BOM. Alternatively, individual voltages can be supplied directly to reduce power dissipation. Examples showing typical supply topologies are described in Section 13.1.1 and Section 13.1.2.

13.1.1 Single supply

Example applications of the TJF1103A and TJF1103B with a single 3.3 V supply are shown in Figure 45 and Figure 46. Connect all voltage rails to the 3.3 V supply, as illustrated.

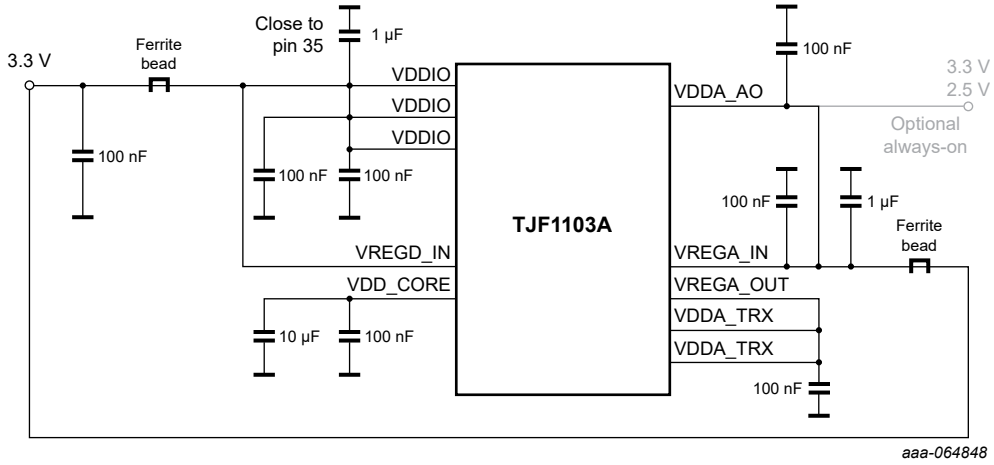


Figure 45. Example TJF1103A application with single 3.3 V supply

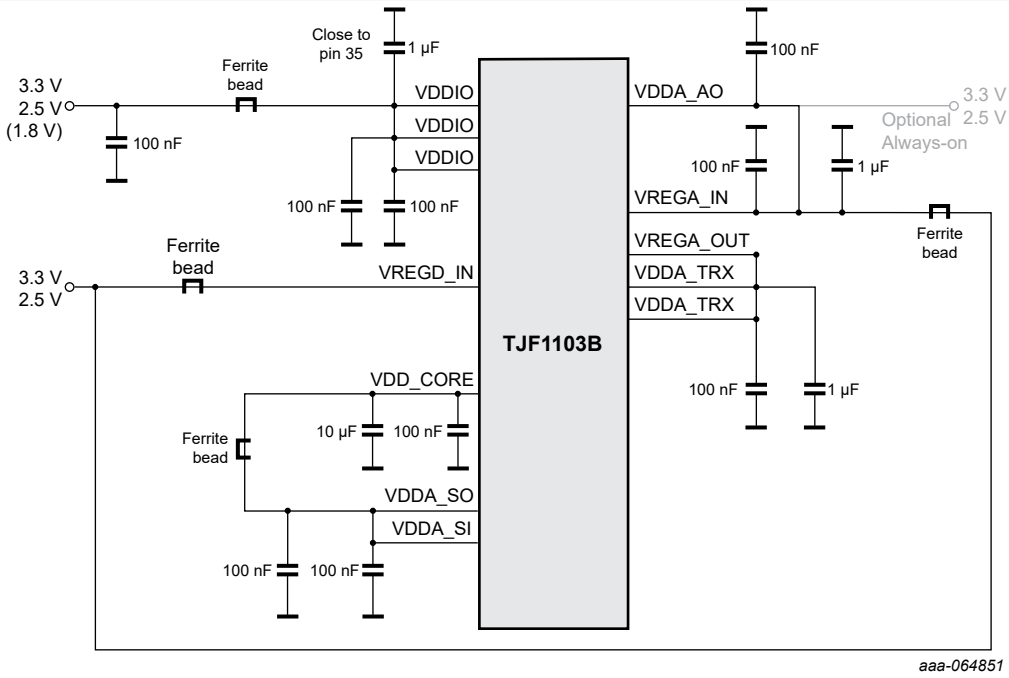


Figure 46. Example TJF1103B application with single 3.3 V supply

13.1.2 Individual supply

Example applications of the TJF1103A and TJF1103B with individual supplies are shown in Figure 47 and Figure 48.

Pins VREGD_IN and VDD_CORE are shorted together and connected to an external 1.1 V source. Pins VREGA_IN, VREGA_OUT and VDDA_TRX are shorted together and connected to an external 2.5 source. For the TJF1103B, pins VREGD_IN, VDD_CORE, VDDA_SO and VDDA_SI must be supplied from the same 1.1 V supply source.

It is possible to supply 1.1 V directly as shown and use the internal regulator to generate VDDA_TRX, as illustrated in Figure 47 and Figure 48. This approach is recommended when a 1.1 V supply is available but not a 2.5 V sypply.

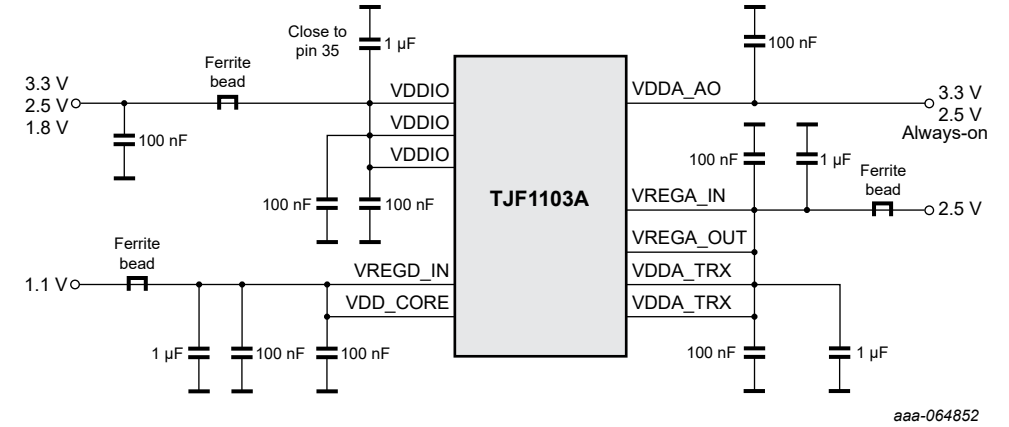


Figure 47. Example TJF1103A application with individual supplies

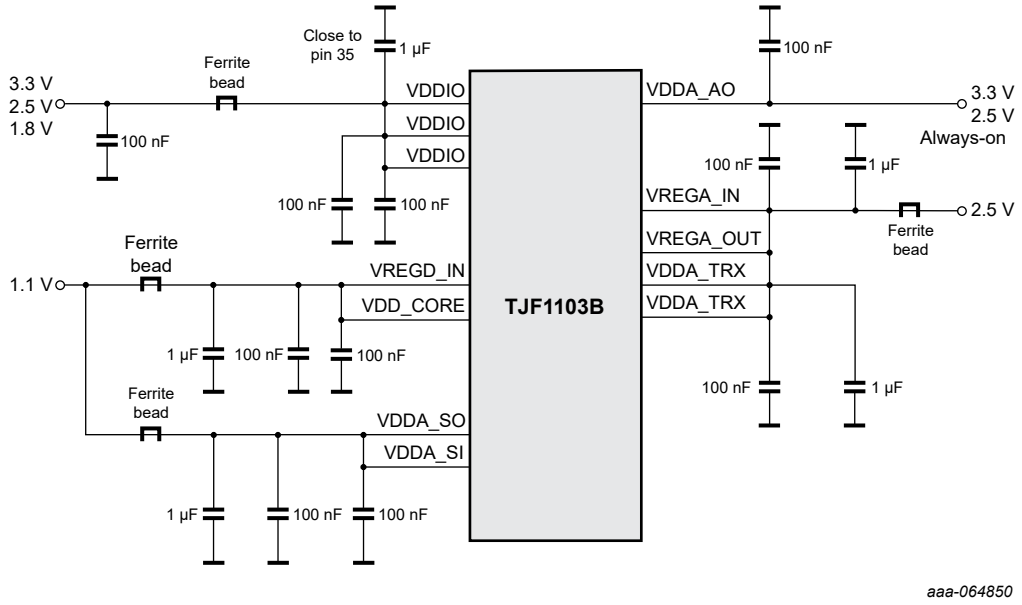


Figure 48. Example TJF1103B application with individual supplies

13.2 Wake-up/Sleep

When the wake-up/sleep feature is used, VDDA_AO must be supplied by a dedicated standby supply. The VDDA_AO supply can operate at 2.5 V or 3.3 V; however 3.3 V is most commonly used. Consult the TJF1103 application notes ref.[6] for further information. Pins INH, WAKE_IN_OUT and RST_N are in the VDDA_AO domain. So any interfacing to these pins must be compatible with the level on VDDA_AO.

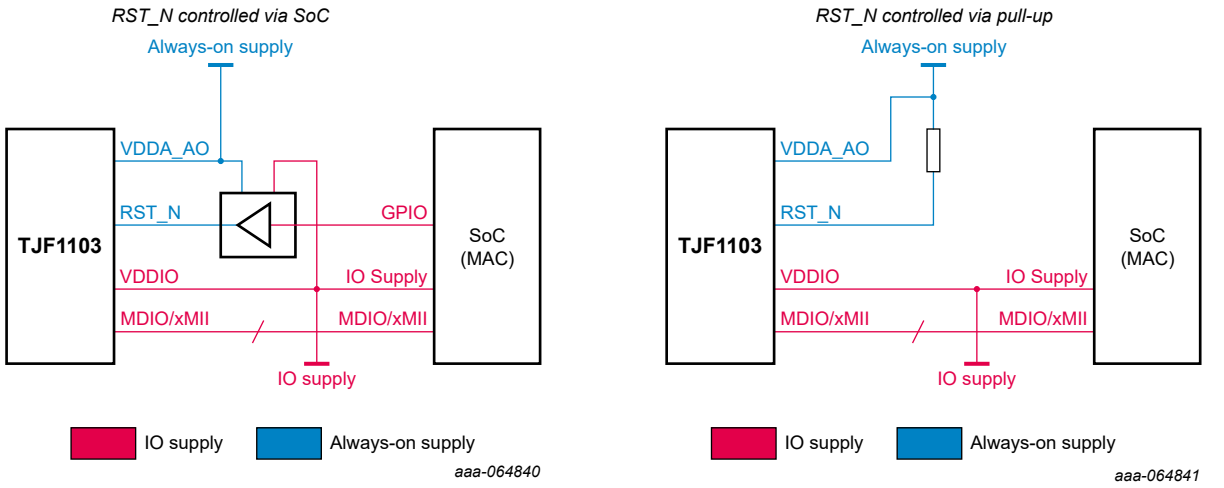
13.3 Reset

The RST_N pin is part of the VDDA_AO voltage domain. It makes sure the device does not run through a reset sequence automatically after a deep-sleep during which only VDDA_AO is present. When VDDA_AO and VDDIO are different supplies, RST_N must be is driven with voltage levels according to VDDA_AO.

For example, if VDDIO is 1.8 V, all microcontroller pins operate in 1.8 V mode. In this case, RST_N cannot be connected directly to a microcontroller pin, because RST_N has thresholds relative to VDDA_AO and not VDDIO. See the application notes ref.[6] for examples.

Figure 49 shows two possible ways the TJF1103 and a microcontroller can be connected. Additional components, such as pull-up resistors, may be required. It is mandatory to keep the RST_N at defined levels during all phases of system startup, operation, sleep and wake-up.

Note: *Never assert RST_N during wake/sleep cycles. A device reset clears all wakeup/sleep-related states. When the microcontroller controls RST_N, check that the GPIO behavior of the microcontroller during startup/reset is well defined. A glitch on the GPIO outputs can lead to a TJF1103 reset.*



(a) RST_N controlled via SoC

(b) RST_N controlled via pull-up

Figure 49. Driving the RST_N pin

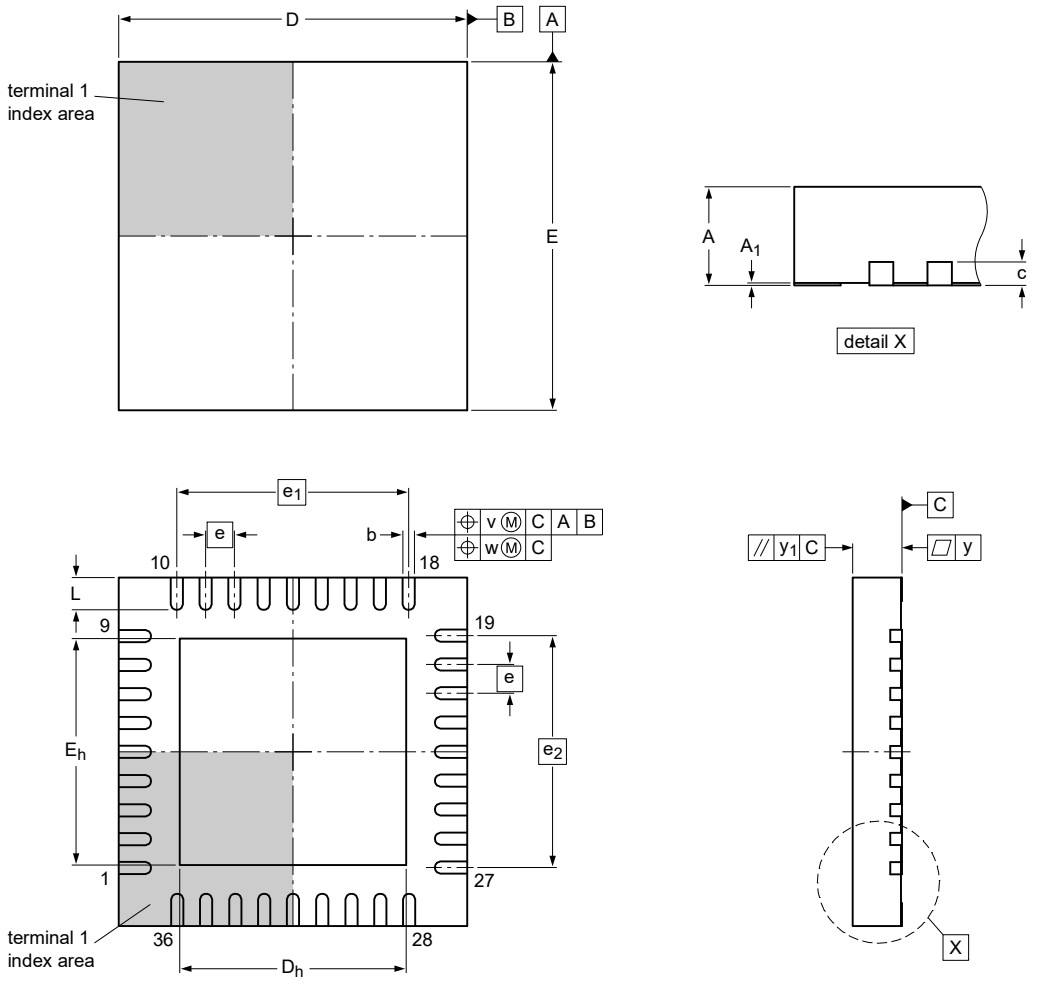
14 Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 Rev-H - *Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

15 Package outline

HVQFN36: plastic thermal enhanced very thin quad flat package; no leads; 36 terminals; body 6 x 6 x 0.85 mm **SOT1092-2**



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	1.00	0.05	0.30		6.1	4.05	6.1	4.05				0.65				
	nom	0.85	0.02	0.21	0.2	6.0	3.90	6.0	3.90	0.5	4	4	0.55	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		5.9	3.75	5.9	3.75				0.45				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1092-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1092-2		---	---			~~09-02-23~~ 09-02-24

Figure 50. Package outline TJF1103 HVQFN36

16 Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 51) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 344 and Table 345

Table 344. SnPb eutectic process (from J-STD-020D)

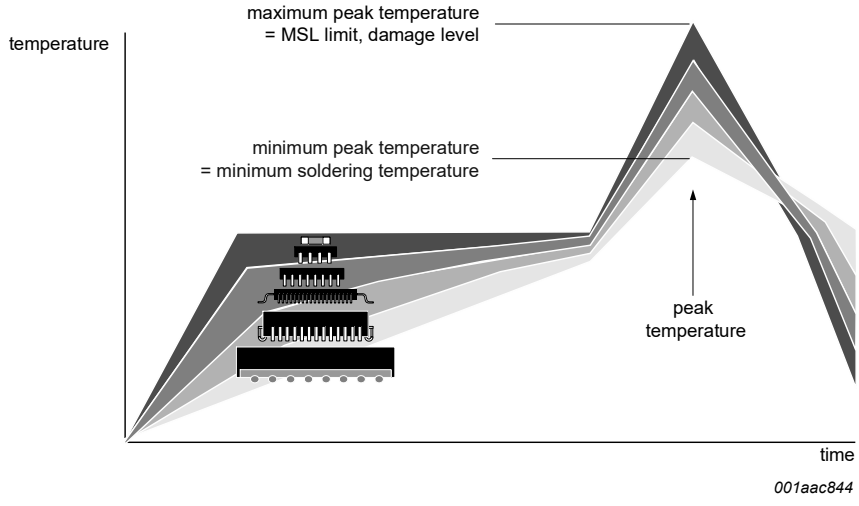
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 345. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 51.



MSL: Moisture Sensitivity Level

Figure 51. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17 Abbreviations

Table 346. List of abbreviations

Abbreviation	Description
AFE	analog frontend
BIST	built-in self-test
BSCAN	boundary scan
CDM	charged-device model
CMOS	complementary metal-oxide-semiconductor
ECU	electronic control unit
EMC	electromagnetic compatibility
EPHY	ethernet physical layer
ESD	electrostatic discharge, end of stream delimiter ref.[1]
FUSA	functional safety
GPIO	general-purpose Input-output
HBM	human body model
HVQFN	enhanced very thin quad flat package
IEEE	institute of electrical and electronics engineers
ISI	inter-symbol interference
IRQ	interrupt
IPG	Inter-packet gap
JTAG	joint test action group
LED	light emitting diode
LVCMOS	low-voltage CMOS
MAC	media access control
MDI	media-dependant interface
MDIO	management data input/output
MII	media independent interface
MMD	MDIO manageable devices
MSE	mean square error
OUI	organizationally unique Identifier
OV	over voltage
PCB	printed circuit board
PHY	physical layer
PPS	pulse-per-second
PTP	precision time protocol
RGMII	reduced gigabit media independent interface
RMII	reduced media independent interface

Table 346. List of abbreviations...*continued*

Abbreviation	Description
SerDes	serializer / deserializer
SFD	start of frame delimiter
SSD	start of stream delimiter
SGMII	serial gigabit media independent interface
SQI	singal quality indicator
UV	under voltage
xMII	x media independent interface

18 References

[1] IEEE Std 802.3-2018, 31 August 2018
[2] RMII Specification 1.2, RMII Consortium, 20 March 1998
[3] RGMII Specification 2.0, Broadcom, HP, Marvell, 1 April 2002
[4] ISO 21111-2:2020 Road vehicles — In-vehicle Ethernet — Part 2: Common physical entity requirements
[5] Serial-GMII Specification 1.8, Cisco Systems, 27 April 2005
[6] AN14876, TJF1103 application notes, NXP, https://www.nxp.com/

19 Revision history

Table 347. Revision history

Document ID	Release date	Description
TJF1103 v.1.0	22 May 2026	• Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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