TEA2392T

GreenChip synchronous rectifier controller

Rev. 1.0 — 12 March 2026 Product data sheet

1 General description

The TEA2392T is a member of a new generation of synchronous rectifier (SR) controller ICs for switched mode power supplies. It includes an adaptive gate drive for maximum efficiency at any load.

The TEA2392T is a dedicated controller IC for synchronous rectification on the secondary side of the asymmetrical half-bridge (AHB) and standard flyback converters. It incorporates the sensing stage and driver stage for driving the SR MOSFET, which is rectifying the output of the secondary transformer winding.

The TEA2392T is optimized for efficient operation with very low-ohmic MOSFETs and relative high output voltages.

The TEA2392T is fabricated in a silicon-on-insulator (SOI) process.

2 Features and benefits

2.1 Efficiency features

- Adaptive gate drive for maximum efficiency at any load
- Supply current in energy save operation of 80 µA
- Regulation level of −29 mV for driving low-ohmic MOSFETs

2.2 Application features

- Drain sense voltage to 200 V
- Wide supply voltage range from 4.5 V to 38 V
- Synchronous rectification for AHB and flyback
- Supports 5 V operation for a logic level SR MOSFET
- SO8 package

2.3 Control features

- SR control without minimum on-time
- Adaptive gate drive for fast turn-off at the end of conduction
- Undervoltage lockout (UVLO) protection with active gate pull-down

3 Applications

The TEA2392T is intended for asymmetrical half-bridge or flyback power supplies. It can drive an external synchronous rectifier MOSFET for the rectification of the voltage on the secondary winding of the transformer. This MOSFET replaces the diode. It can be used in all power supplies that require high efficiency:

- Adapters
- Chargers
- Asymmetrical half-bridge or flyback power supplies
- Flyback power supplies with very low and/or variable output voltage
- Power supplies for E-bikes or small EVs
- Power supplies for industrial applications

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA2392T/1	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5 Marking

Table 2. Marking

Type number	Marking code
TEA2392T/1	TEA2392

6 Block diagram

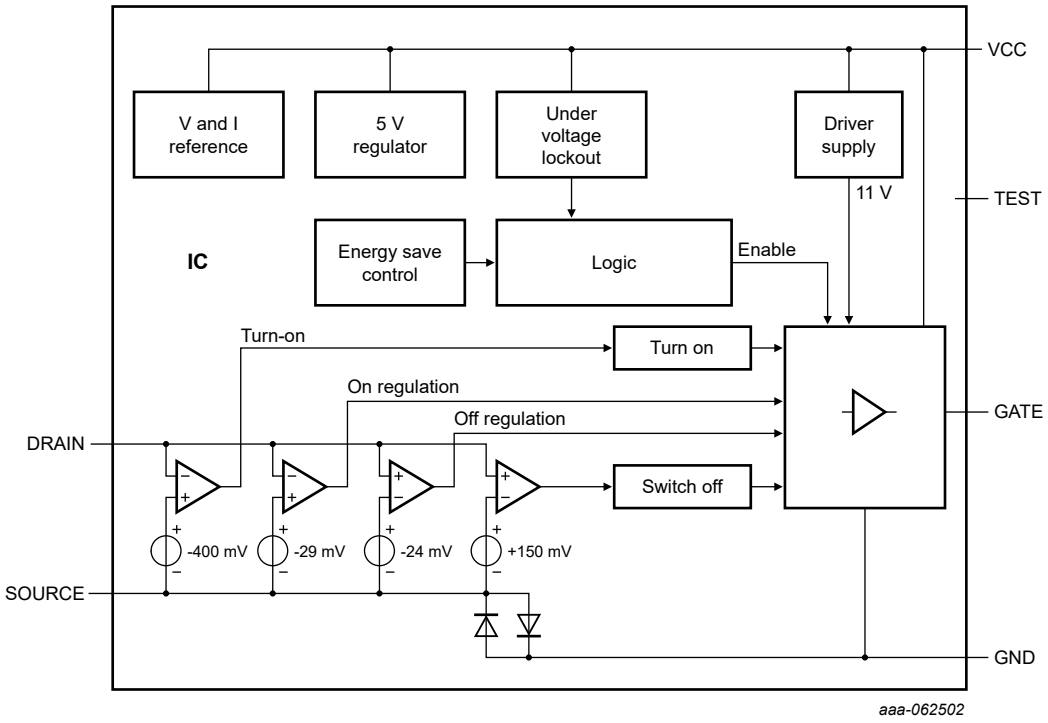


Figure 1. TEA2392T block diagram

7 Pinning information

7.1 Pinning

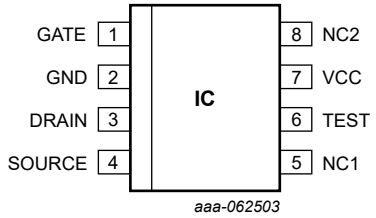


Figure 2. TEA2392T pin configuration (SOT96-1)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
GATE	1	gate drive output MOSFET
GND	2	ground
DRAIN	3	drain sense input for synchronous timing MOSFET
SOURCE	4	source sense input MOSFET
NC1	5	not connected
TEST	6	TEST pin. Must externally be connected to pin VCC
VCC	7	supply voltage
NC2	8	not connected

8 Functional description

8.1 Introduction

The TEA2392T is a controller IC for synchronous rectification. It is perfectly suited to be used in asymmetrical half-bridge (AHB) and standard flyback converters. It can drive an external synchronous rectifier MOSFET for the rectification of the voltage on the secondary winding of the transformer. Figure 3 shows a typical configuration.

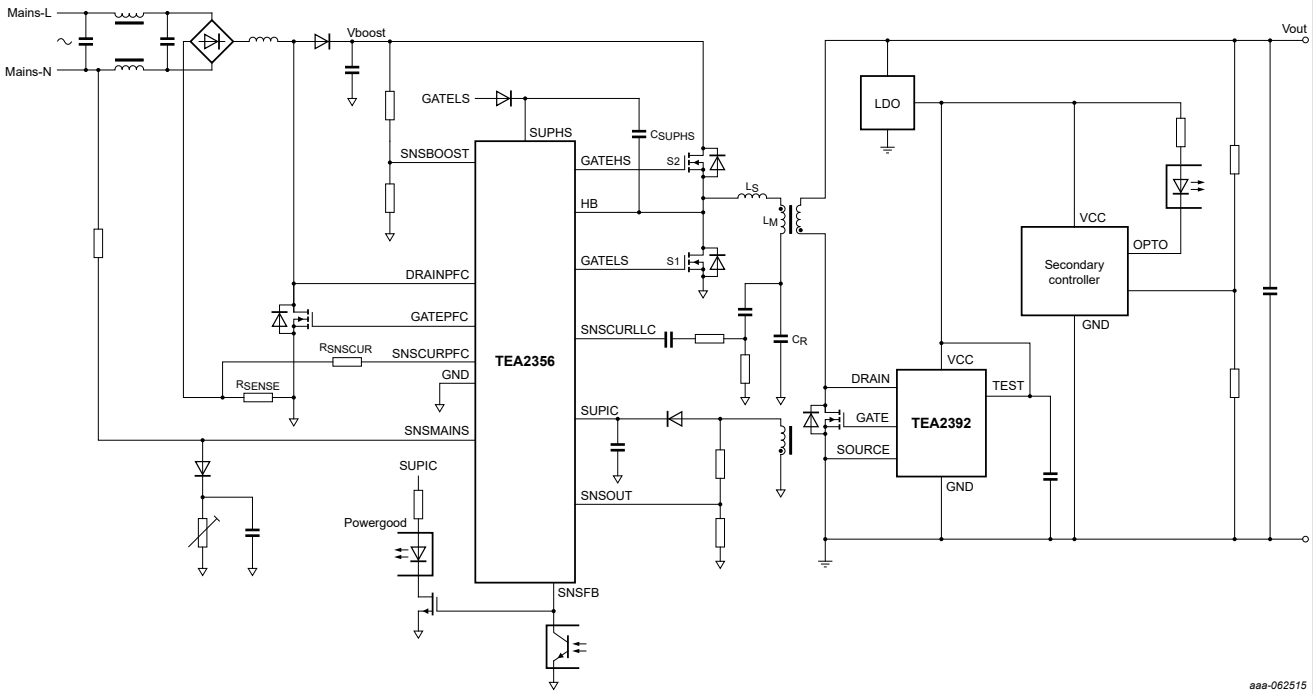


Figure 3. TEA2392T typical configuration

8.2 Start-up and undervoltage lockout (V_{CC} pin)

When the voltage on the V_{CC} pin exceeds V_{start}, the IC leaves the UVLO state and activates the SR circuit. When the voltage drops to below V_{stop}, the IC reenters the UVLO state. The SR MOSFET gate driver output is actively kept low. For proper operation, the V_{CC} pin must be decoupled with an extra capacitor (not only with C_{out}) between the V_{CC} pin and the GND pin. To reduce inductance effects because of high gate driver currents, the extra capacitor must be connected as close as possible to the IC.

8.3 Drain sense (DRAIN pin)

The drain sense pin is an input pin capable of handling input voltages up to 200 V.

At positive drain sense voltages, the gate driver is in off-mode with pulled-down gate driver pin (pins GATE). At negative drain sense voltages, the IC enables the SR through sensing the drain source differential voltage.

8.4 Synchronous rectification (DRAIN and SOURCE pins)

The IC senses the voltage difference between the drain sense (pin DRAIN) and the source sense (pin SENSE) connections. The drain source differential voltage of the SR MOSFET is used to drive the gate of the SR MOSFET.

When this absolute voltage difference is higher than $V_{act(drv)}$, the gate driver output turns on the external SR MOSFET. When the external SR MOSFET is switched on, the absolute voltage difference between the drain and the source sense connections drops to below $V_{act(drv)}$. The regulation phase follows the turn-on phase.

In the regulation phase, the IC regulates the difference between the drain and the source sense inputs to an absolute level ($V_{reg(drv)}$). When the absolute difference is higher than $V_{reg(drv)}$, the gate driver output increases the gate voltage of the external SR MOSFET until the $V_{reg(drv)}$ level is reached. The SR MOSFET does not switch off at low currents. The IC operates without minimum on-time.

When the absolute difference is lower than $V_{deact(drv)}$, the gate driver output decreases the gate voltage of the external SR MOSFET. The voltage waveform on the gate of the SR MOSFET follows the waveform of the current through the SR MOSFET. When the current through the external SR MOSFET reaches zero, the SR MOSFET is quickly switched off.

After the SR MOSFET switch-off, the drain voltage increases. For a drain voltage above V_{swoff}, a low ohmic gate pull-down of $R_{pd(G)}$ keeps the gate of the SR MOSFET switched off.

8.5 Gate driver (GATE pin)

During the rising part of the current, the gate driver circuit charges the gate of the external SR MOSFET. During the falling part of the current, the driver circuit discharges the gate. The gate driver has a source capability of typically I_{source} and a sink capability of typically I_{sink}. The source and sink capability allow a fast turn-on and a fast turn-off of the external SR MOSFET.

The maximum driver output voltage is limited to $V_{G(max)}$. This high output voltage drives all MOSFET brands to the minimum on-state resistance.

In applications where the IC is supplied with 5 V, the maximum output voltage of the driver is limited to 5 V. Logic level SR MOSFETs can be used.

During start-up conditions ($V_{CC} < V_{start}$) and UVLO, the driver output voltage is actively pulled low.

8.6 Source sense connection (SOURCE pin)

The IC is equipped with an additional source sense pin (SOURCE). This pin is used to measure the SR MOSFET drain-to-source voltage. The source-sense input must be connected as close as possible to the source pin of the external SR MOSFET. It minimizes errors that voltage differences on PCB tracks cause because of parasitic inductance and high dI/dt values.

9 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{CC}	supply voltage		−0.4	+38	V
$V_{sense(DRAIN)}$	sense voltage on pin DRAIN	DC	−0.8	+200	V
$V_{sense(SOURCE)}$	sense voltage on pin SOURCE	DC	−0.4	+0.4	V
V_{GATE}	voltage on pin GATE	DC [1]	−0.4	+12	V
General					
f_{max}	maximum frequency	if not limited by T_j	-	1	MHz
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		−40	+150	°C
Electrostatic discharge (ESD)					
V_{ESD}	electrostatic discharge voltage	human body model (HBM) [2]	-	2000	V
		charged device model (CDM) [3]	-	500	V

[1] Output pin; not to be voltage driven.
[2] Human body model: Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
[3] Charged device model: Equivalent to charging the IC and discharging each pin over a 1 Ω resistor.

10 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.75	38	V
T_j	junction temperature		−40	+125	°C

11 Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO8 package; PCB 1 layer; 35 µm Cu; 60 mm x 125 mm	135	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	SO8 package	50	K/W

12 Characteristics

Table 7. Characteristics

T_{amb} = 25 °C; V_{CC} = 12 V; C_{GDA}/C_{GDB} = 10 nF (capacitors between GDA and GND and between GDB and GND). All voltages are measured with respect to ground (pin 2). Currents are positive when flowing into the IC, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage management (pin VCC)						
V_{start}	start voltage		4.3	4.5	4.7	V
V_{stop}	stop voltage		4.0	4.2	4.4	V
$I_{CC(oper)}$	operating supply current	energy-save	60	80	100	µA
		normal operation (without gate charge)	0.6	0.8	1.1	mA
$t_{act(es)}$	energy-save mode activation time		85	110	135	ns
Synchronous rectification sense input (pins DRAIN and SOURCE)						
$V_{act(drv)}$	driver activation voltage	$V_{sense(SOURCE)}$ = 0 V	−450	−400	−350	mV
$V_{reg(drv)}$	driver regulation voltage	$V_{sense(SOURCE)}$ = 0 V	−36	−29	−23	mV
V_{swoff}	switch-off voltage	$V_{sense(SOURCE)}$ = 0 V	60	150	200	mV
$t_{d(act)(drv)}$	driver activation delay time	$V_{sense(SOURCE)}$ = 0 V; normal operation; time from step on V_{DRAIN} (2 V to −0.5 V) to rising of V_{GATE} at 10 % of end value	-	80	-	ns
$t_{d(deact)(drv)}$	driver deactivation delay time	$V_{sense(SOURCE)}$ = 0 V; normal operation; time from step on V_{DRAIN} (−0.5 V to 2 V) to falling of V_{GATE} at 90 % of begin value	-	40	-	ns
Gate driver (pin GATE)						
I_{source}	source current	peak current at V_{DRAIN} = −0.5 V; V_{GATE} = 0 V	-	−0.3	-	A
I_{sink}	sink current	regulation current at V_{DRAIN} = 0 V; V_{GATE} = 5 V	-	1	-	A
		peak current at V_{DRAIN} = 0.25 V; V_{GATE} = 5 V	-	2	-	A
$R_{pd(G)}$	gate pull-down resistance	V_{DRAIN} = 12 V; I_{GATE} = 100 mA	2.0	2.5	3.0	Ω
$V_{G(max)}$	maximum gate voltage	V_{GATE} at V_{CC} = 5 V	4.98	4.99	5.00	V
		V_{GATE} at V_{CC} = 12 V	10.4	10.7	11.0	V
		V_{GATE} at V_{CC} = 38 V	10.6	10.9	11.2	V

13 Application information

An asymmetrical half-bridge switched-mode power supply with the TEA2392T consists of a primary side half-bridge, a transformer, a resonant capacitor, and an output stage. To obtain low conduction loss rectification, an SR MOSFET is used in the output stage. The TEA2392T controls the SR MOSFET.

The gate drive voltage for the SR switch is derived from the voltage difference between the drain sense and source sense pin.

Special attention must be paid to the connection of the drain sense and source sense pin. The voltage difference between these pins is used to control gate drive voltage. Wrong measurement results in a less efficient gate drive because the gate voltage is either too low or too high. The connections to these pins must not interfere with the power wiring. The power wiring conducts currents with high dI/dt values. It can easily cause measurement errors resulting from induced voltages due to parasitic inductances.

The separate source-sense pin enables the direct sensing of the source voltage of the external MOSFET. Using the current carrying power ground tracks is not allowed.

For output voltages below 38 V, the V_{CC} pin can be connected to V_{out} directly.

For output voltages exceeding 38 V, the V_{CC} voltage can be generated via a linear or a discrete regulator (see Figure 5).

13.1 Asymmetrical half-bridge application

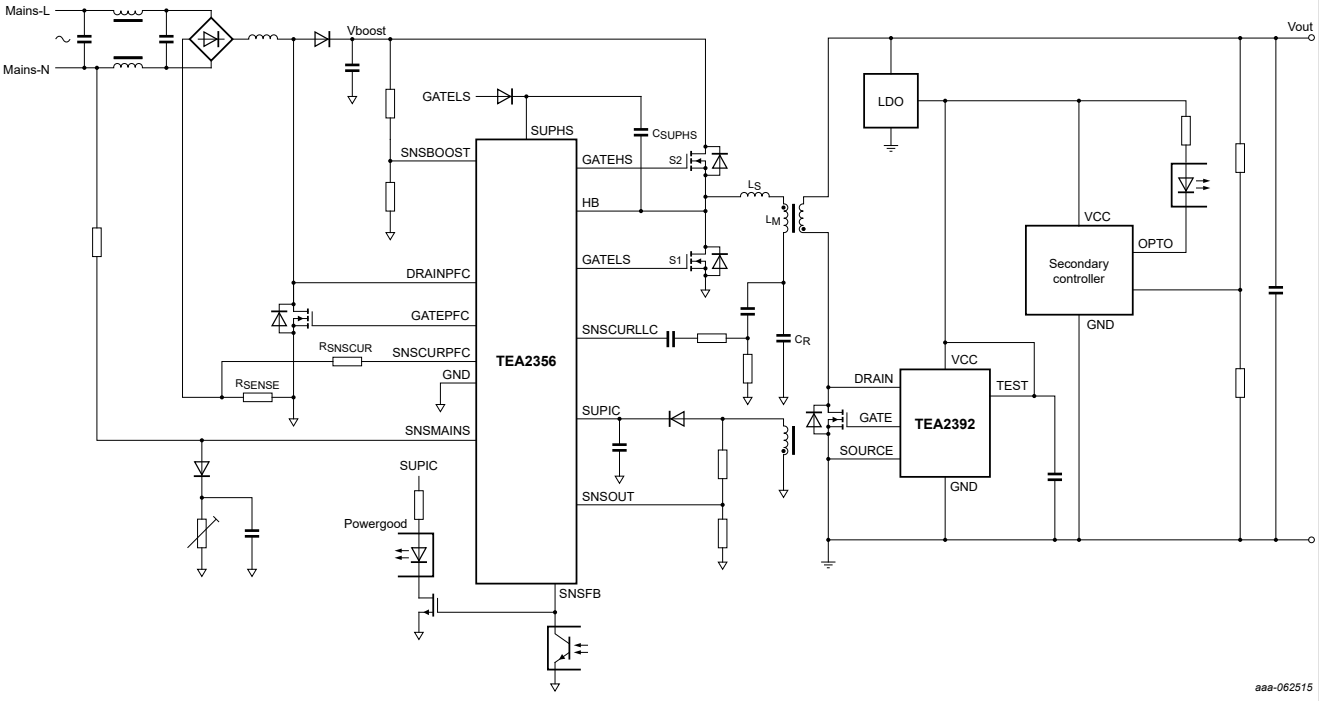
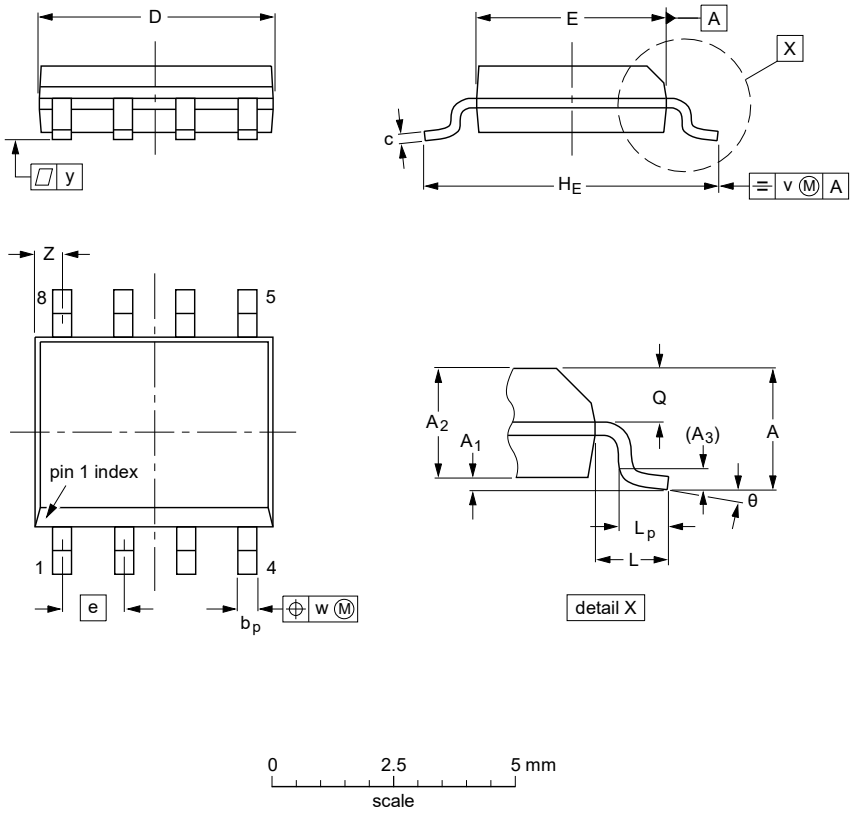


Figure 4. Typical AHB Application with TEA2392T

14 Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Figure 5. Package outline SOT96-1 (SO8)

15 Abbreviations

Table 8. Abbreviations

Acronym	Description
CDM	charged device model
ESD	electrostatic discharge
HBM	human body model
MOSFET	metal-oxide-semiconductor field-effect transistor
SOI	silicon-on insulator
SR	synchronous rectification
UVLO	undervoltage lockout

16 Revision history

Table 9. Revision history

Document ID	Release date	Description
TEA2392T v.1.0	12 March 2026	Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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