S32M2xx

S32M2xx Data Sheet

Supports S32M24x and S32M27x

Rev. 3 — 10/2023

Data Sheet: Advance Information

S32M241
S32M242
S32M243
S32M244
S32M274
S32M276

- This document provides electrical specifications for S32M2xx.
- For functional characteristics and the programming model, see S32M24x and S32M27x Reference Manuals.

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1 About the document

This document is divided into four main parts:

1. Sections in the first set contain information that applies to the S32M27x and S32M24x System in Package (SIP) devices. These includes from section 2 to section 7 and section 11 and 12.
2. Sections in the second set are applicable to “Application extension” Subsytem, hence applies to both S32M24x and S32M27x, this includes section 8 and its sub-sections.
3. Sections in the third set are applicable to S32M27x MCU, this includes section 9 and its sub-sections.
4. Sections in the fourth set are applicable to S32M24x MCU, this includes section 10 and its sub-sections.

2 Introduction

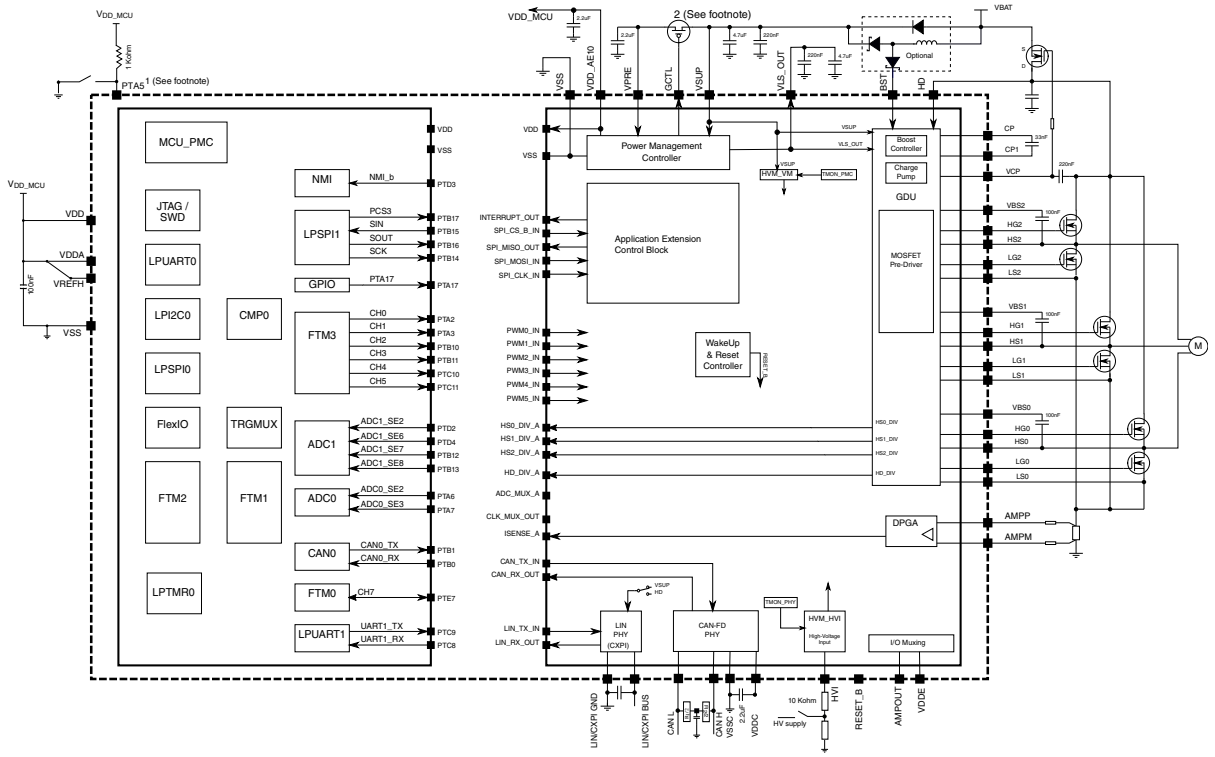
S32M2 is a family of integrated solutions based on ARM Cortex M microcontroller cores that closely resemble NXP’s S32K MCU products with the addition of high voltage analog features. The commonality between S32M2 and S32K, be that hardware or supporting software and firmware, results in a combined portfolio with scalability between general purpose MCUs and integrated solutions. Building on S32K System on Chip (SoC) microcontrollers, S32M2's System in Package (SiP) integrates automotive qualified and application-focused capabilities like voltage-regulators operating directly from a car battery, physical communications interfaces (LIN, CXPI, or CAN FD), and MOSFET Gate pre-drivers for motor control. With attention to cost at the system level, S32M2 integrates voltage regulators, pulse-width modulators, analog to digital converters, timers, non-volatile memory and more to reduce overall component count and reduce board space.

This document covers, S32M24x and S32M27x families, both targeting motor control for a single BLDC/PMSM motor or up to three Brushed DC motors. Communication is over LIN, CXPI, or CAN FD directly with the included physical interfaces. The main attributes of devices within the sub-family are:

- Built-in voltage regulation and protection to run directly from a reverse-battery protected 12V car battery supply.
- 5V voltage output to supply power to an external component like hall sensor.
- LIN, CXPI or CAN-FD physical interface for direct connection to the communications bus without an external phy.
- Arm Cortex M4 processors with Floating Point running up to 80MHz or Arm Cortex M7 processors with Floating Point running up to 120 MHz.
- Non-volatile program memory from 128KB to 1MB.
- Integrated gate driver for up to 6 external power MOSFETs for BLDC or PMSM motor drive applications.
- 64-pin LQFP-EP Package.

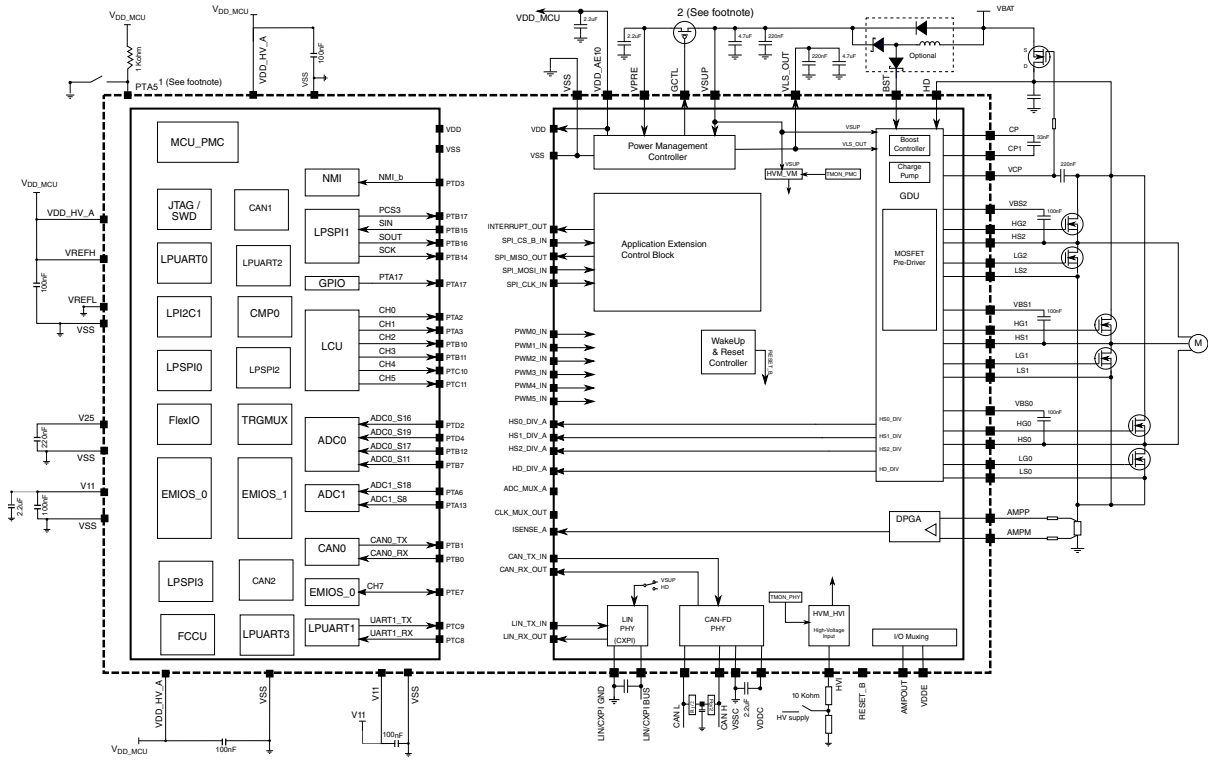
3 Block diagram

The following figures shows block diagram of the S32M24x and S32M27x family. On the left side is the MCU and on the right side is the AE. The SiP boundary is the bold dashed line. The diagram shows typical external components required for a 3-phase motor control application with single-shunt current sensing.



1. The pins PTA5 and RESET_B must be connected at board level.
2. The VPRE voltage can be regulated using an external p-channel power FET (gate controlled via the GCTL pin), to reduce the on chip power dissipation and assure that the maximum operating junction temperature is not exceeded. Depending on the operating conditions of the application (ambient temperature, MCU load), the external FET could be required.

Figure 1. S32M24x Block diagram



1. The pins PTA5 and RESET_B must be connected at board level
2. The VPRE voltage can be regulated using an external p-channel power FET (gate controlled via the GCTL pin), to reduce the on chip power dissipation and assure that the maximum operating junction temperature is not exceeded. Depending on the operating conditions of the application (ambient temperature, MCU load), the external FET could be required.

Figure 2. S32M27x Block diagram

4 Feature comparison

The following tables shows feature comparison between different devices from the S32M2 family. For each part number, there are two different options, with either a CAN-FD physical layer or a LIN physical layer, compatible with CXPI. For certain peripherals (for example, UART, I2C, SPI, or EMIOS) the amount of channels available in each package option is indicated in the table with “CAN” or “LIN”. See the Ordering Information section.

Table 1. S32M24x Feature comparison

	Feature description	S32M241	S32M242	S32M243	S32M244
System	Core and Frequency	Arm CM4F @80MHz	Arm CM4F @80MHz	Arm CM4F @80MHz	Arm CM4F @80MHz
	ISO 26262	ASIL - B	ASIL - B	ASIL - B	ASIL - B
	Operating Temperature	Grade 1	Grade 1	Grade 0	Grade 0
	HW Security Options	CSEc	CSEc	CSEc	CSEc
Memory	Program flash memory	128 kB	256 kB	256 kB	512 kB

Table continues on the next page...

Table 1. S32M24x Feature comparison (continued)

	Feature description	S32M241	S32M242	S32M243	S32M244
	SRAM	32 kB	32 kB	32 kB	64 kB
	Data flash memory	4 kB (FlexRAM) / 64 kB (Dflash)	4 kB (FlexRAM) / 64 kB (Dflash)	4 kB (FlexRAM) / 64 kB (Dflash)	4 kB (FlexRAM) / 64 kB (Dflash)
Timer	PWM and Logic Control[1 2]	4x 16-bit FlexTimer	4x 16-bit FlexTimer	4x 16-bit FlexTimer	4x 16-bit FlexTimer
	Other Timers	LPIT, LPTMR, RTC	LPIT, LPTMR, RTC	LPIT, LPTMR, RTC	LPIT, LPTMR, RTC
Analog	External ADC channels[3]	2x ADC 12bits	2x ADC 12bits	2x ADC 12bits	2x ADC 12bits
	ADC Trigger control / delay	2x PDB	2x PDB	2x PDB	2x PDB
	Comparator 8-bit DAC	1x	1x	1x	1x
Communication	UART/LIN[4]	1x	1x	1x	1x
	I2C, SPI[5]	1x LPSPI, 1x LPI2C	1x LPSPI, 1x LPI2C	2x LPSPI, 1x LPI2C	2x LPSPI, 1x LPI2C
	CAN (CAN-FD)[6]	1x CAN-FD	1x CAN-FD	1x CAN-FD	1x CAN-FD
	FlexIO (configurable as UART, SPI, I2C, I2S)	1x 7ch	1x 7ch	1x 7ch	1x 7ch
Integrated components	Integrated 12V regulator	Yes	Yes	Yes	Yes
	Supply for external loads	5V (30mA)	5V (30mA)	5V (30mA)	5V (30mA)
	Physical Interface option[4,6]	1x (LIN or CXPI or CAN FD)	1x (LIN or CXPI or CAN FD)	1x (LIN or CXPI or CAN FD)	1x (LIN or CXPI or CAN FD)
	MOSFET Gate Driver Unit (GDU)[1,3]	6 ch (3 ph)	6 ch (3 ph)	6 ch (3 ph)	6 ch (3 ph)
	Temperature sensor[3]	Yes	Yes	Yes	Yes
	High Voltage Input , Battery monitor[3]	1x HVI, 1x VM	1x HVI, 1x VM	1x HVI, 1x VM	1x HVI, 1x VM
	Current Sense[3]	1x DPGA	1x DPGA	1x DPGA	1x DPGA
Other	Debug & Trace	SWD, JTAG	SWD, JTAG	SWD, JTAG	SWD, JTAG
	SW Watchdog	1x	1x	1x	1x
	External Watchdog Monitor	1x	1x	1x	1x

Table continues on the next page...

Table 1. S32M24x Feature comparison (continued)

	Feature description	S32M241	S32M242	S32M243	S32M244
	Package Options (Exposed Pad)	64-pin LQFP-EP	64-pin LQFP-EP	64-pin LQFP-EP	64-pin LQFP-EP

1. Six channels of the FTM3 are internally connected for the PWM signals on GDU.
2. The number of timer channels available on external pins depends on the package option (CAN or LIN). For the actual IO mapping, see the IOMUX file attached to the S32M24x Reference Manual.
3. The number of ADC channels available on external pins depends on the package option (CAN or LIN). For the actual ADC mapping, see the IOMUX file attached to the S32M24x Reference Manual. Additionally, there are six ADC channels that are internally connected for: current sense from DPGA, DC link voltage monitoring, phase voltage measurement, and HVM connections (high voltage Input, VSUP sense, temperature sensor).
4. There are two UART/LIN modules in S32M24x. On LIN variants, LPUART1 is internally connected to LIN/CXPI PHY.
5. There are two SPI modules in S32M242 and S32M241, and three SPI modules in S32M244 and S32M243. LPSPI1 is dedicated to internal configuration and communication.
6. There is one CAN module in S32M24x. On CAN variant, CAN0 is internally connected to CAN FD PHY for CAN FD communication.

Table 2. S32M27x Feature comparison

	Feature description	S32M274	S32M276
System	Core & Frequency	Arm CM7F @ 120 MHz	Arm CM7F @ 120 MHz
	ISO 26262	ASIL-B	ASIL-B
	Operating Temperature	Grade 1	Grade 1
	HW Security	HSE-B	HSE-B
Memory	Program flash memory	512 kB	1 MB
	SRAM	112 kB SRAM including 96 kB TCM	128 kB SRAM including 96 kB TCM
	Data flash memory	64 kB (D Flash)	64 kB (D Flash)
Timers	PWM and Logic Control[1]	2x EMIOS CAN: 15ch+5ch LIN: 16ch+6ch 2x LCU	2x EMIOS CAN: 15ch+5ch LIN: 16ch+6ch 2x LCU
	Other Timers	2x PIT, 1x STM	2x PIT, 1x STM
Analog	External ADC channels[2]	2x ADC 15bit	2x ADC 15bit
	ADC trigger control/delay	1x BCTU	1x BCTU
	Comparator with 8-bit DAC	2x	2x
Communication	UART / LIN[3]	CAN: 2x LPUART, LIN: 3x LPUART	CAN: 2x LPUART, LIN: 3x LPUART
	I2C, SPI[4]	CAN: 1x LPSPI, 1x LPI2C LIN: 2x LPSPI, 1x LPI2C	CAN: 1x LPSPI, 1x LPI2C LIN: 2x LPSPI, 1x LPI2C
	CAN (CAN-FD)[5]	CAN: 2x CAN-FD	CAN: 2x CAN-FD

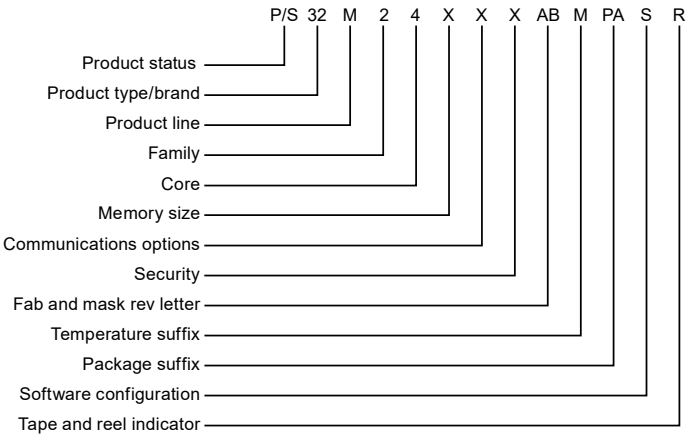
Table continues on the next page...

Table 2. S32M27x Feature comparison (continued)

	Feature description	S32M274	S32M276
		LIN: 3x CAN-FD	LIN: 3x CAN-FD
	FlexIO (configurable as UART, SPI, I2C, I2S)	1x 9ch	1x 9ch
Integrated components	Integrated 12- V regulator	Yes	Yes
	Supply for external loads	5V (30 mA)	5V (30 mA)
	Physical Interface option[3,5]	1x (LIN or CXPI or CAN FD)	1x (LIN or CXPI or CAN FD)
	MOSFET Gate Driver Unit (GDU)[1,2]	6ch (3- phase)	6ch (3- phase)
	Temperature Sensor[2]	Yes	Yes
	High Voltage Input, Battery Monitor[2]	1x HVI, 1x VM	1x HVI, 1x VM
	Current Sense[2]	1x DPGA	1x DPGA
Other	Debug & Trace	SWD, JTAG	SWD, JTAG
	SW Watchdog	1x	1x
	External Watchdog Monitor	1x	1x
Package	Exposed Pad	64-pin LQFP-EP	64-pin LQFP-EP

1. Six outputs of the LCU are internally connected for the PWM signals on GDU.
2. Additionally, there are six ADC channels that are internally connected for: current sense from DPGA, DC link voltage monitoring, phase voltage measurement, and HVM connections (high voltage Input, VSUP sense, temperature sensor).
3. There are four UART/LIN modules in S32M27x. On LIN variants, LPUART1 is internally connected to LIN/CXPI PHY.
4. There are four LPSPI modules in S32M27x, listing only modules with external pins available. LPSPI1 is dedicated to internal configuration and communication.
5. There are three CAN modules in S32M27x. On CAN variant, CAN0 is internally connected to CAN FD PHY for CAN FD communication.

5 Ordering information



Product status
P: Prototype
S: Qualified ordering P/N

Product type/brand
32: Automotive 32-bit MCU/MPU

Product line and family
M2 = 12 V motor control

Core platform
4 = Arm cortex M4
7 = Arm cortex M7, single core

Memory size

	0	1	2, 3*	4	6	8
M24x M27x	-	128 K	256 K	512 K	1 MB	8 MB

* 3 is used only for S32M243, a special grade zero capable version for 256 KB

Features
Communication phy option

L: LIN phy
C: CAN FD phy
X: CXPI phy

Security
C: CSEc security (S32M24x)
H: HSE security (S32M27x)
x: OEM specific security firmware

Fab and mask rev letter
See table 3 below

Temperature suffix
V: -40°C to 105°C
M: -40°C to 125°C
W: -40°C to 150°C (S32M243/244 only)

Package suffix

Pins	LQFP-EP
64	KH

Software configuration
S = Family SW package, including:
- SDK
- AUTOSAR MCAL(ISO26262, crypto driver included)
- Core self test SW
- Standard security firmware

Additional solution specific SW

Tape and reel indicator
T: Trays/tubes
R: Tape and reel

Figure 3. Ordering information

Table 3. Part number information

Product family	Fab/Mask revision ordering code	MCU mask revision	Analog die mask revision	Notes
S32M241/ S32M242	T0	0N33V	0P73G	Pre-production samples only
	AB	0N33V	0P69K	-
S32M243/ S32M244	T0	0P64A	0P73G	Pre-production samples only
	AB	0P64A	0P69K	-
S32M274/ S32M276	T0	0P98C	0P73G	Pre-production samples only
	AB	0P98C	0P69K	-

6 General

6.1 Absolute maximum ratings

NOTE

Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in the following table for specific conditions. For the functional operating conditions see the DC electrical characteristics section "Voltage and current operating requirements". All voltages are referred to VSS unless otherwise specified. All the limits defined in the datasheet specification must be honored together and any violation to any one or more will not guarantee desired operation. Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device. Unless otherwise specified, all maximum and minimum values in the datasheet are across process, voltage, and temperature.

CAUTION

When the MCU is in an unpowered state, current injected through the chip pins may bias internal chip structures (for example, ESD diodes) and incorrectly power up these internal structures through inadvertent paths. The presence of such residual voltage may influence different chip-internal blocks in an unpredictable manner and may ultimately result in unpredictable chip behavior (for example, POR flag not set). Once in the illegal state, powering up the chip further and then applying reset will clear the illegal state. Injection current specified for the chip under the aspect of absolute maximum ratings represent the capability of the internal circuitry to withstand such condition without causing physical damage. Functional operation of the chip under conditions specified as absolute maximum ratings is not implied.

Table 4. Absolute maximum ratings

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VSUP	Voltage regulator and LINPHY supply voltage	-0.3	—	42	V	—	—
VLIN	DC voltage on LIN	-32	—	42	V	—	—
VCANH, VCANL	DC voltage on CANH and CANL	-32	—	40	V	—	—
VHVI	DC voltage on HVI pin HVI0 [1]	-32	—	42	V	—	—
VHD	MOSFET pre-driver high-side drain voltage	-0.3	—	42	V	—	—
VVLS_OUT	MOSFET pre-driver supply, internally generated	-0.3	—	12	V	—	—
VVBSx	MOSFET pre-driver bootstrap capacitor connection	-0.3	—	VHSx + 12	V	—	—
VHGx	MOSFET pre-driver high-side gate [2]	-2	—	VHSx + 12	V	—	—

Table continues on the next page...

Table 4. Absolute maximum ratings (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VHSx	MOSFET pre-driver high-side source	-2	—	42	V	—	—
VHSx	MOSFET pre-driver high-side source, negative pulse of up to 100ns [3]	-7	—	—	V	—	—
VLGx	MOSFET pre-driver low-side gate [2]	-2	—	12	V	—	—
VLSx	MOSFET pre-driver low-side source	-2	—	10	V	—	—
VLSx	MOSFET pre-driver low-side source, negative pulse of up to 100ns [3]	-7	—	—	V	—	—
VCP	MOSFET pre-driver charge pump driver output	-0.3	—	12	V	—	—
VCP1	MOSFET pre-driver charge pump charge & discharge node	-0.3	—	55	V	—	—
VVCP	MOSFET pre-driver charge pump output voltage	-0.3	—	55	V	—	—
VBST	MOSFET pre-driver boost converter connection	-0.3	—	42	V	—	—
VDDC	CAN-FD PHY supply, internally generated	-0.3	—	6	V	—	—
VAMPP	DPGA amplifier non-inverting input voltage	-0.3	—	6	V	—	—
VAMPP	DPGA amplifier non-inverting input voltage, negative pulse of up to 1us [4]	-7	—	—	V	—	—
VAMPM	DPGA amplifier inverting input voltage	-0.3	—	6	V	—	—
VAMPM	DPGA amplifier inverting input	-7	—	—	V	—	—

Table continues on the next page...

Table 4. Absolute maximum ratings (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	voltage, negative pulse of up to 1us [4]						
VAMPOUT	DPGA amplifier output voltage	-0.3	—	6	V	—	—
VVPRE	VPRE internally generated pre-regulation stage	-0.3	—	7.5	V	—	—
VGCTL	Voltage regulator ballast connection	-0.3	—	42	V	—	—
VSUP - VGCTL	VSUP to GCTL differential voltage [5]	-0.3	—	5	V	—	—
VDD_AE10	3.3V/5V regulated voltage for MCU supply	-0.3	—	5.8	V	—	—
VDD, VDDA	MCU I/O and analog supply voltages (S32M24x devices) [6,7]	-0.3	—	5.8	V	—	—
VREFH	ADC high reference voltage (S32M24x devices) [7]	-0.3	—	5.8	V	—	—
VGPIO_DC	Continuous DC Voltage on any MCU I/O pin (S32M24x devices) [8]	-0.8	—	5.8	V	—	—
VGPIO_ TRANSIENT	Transient overshoot voltage allowed on MCU I/O pin beyond the VGPIO_DC limit (S32M24x devices) [9]	—	—	6.8	V	—	—
VDD_HV_A	MCU I/O and analog supply voltage (S32M27x devices) [10,11]	-0.3	—	6	V	—	—
V25	Flash memory supply (2.5 V), internally regulated (S32M27x devices)	-0.3	—	2.9	V	—	—
V11	Core logic voltage supply (1.1 V), internally	-0.3	—	1.26	V	—	—

Table continues on the next page...

Table 4. Absolute maximum ratings (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	regulated (S32M27x devices)						
VREFH	ADC high reference voltage (S32M27x devices) [10]	-0.3	—	6	V	—	—
VGPIO_trans	Transient overshoot voltage allowed on MCU I/O pin (S32M27x devices) [10,12]	—	—	6	V	—	—
IINJPAD_DC_ABS	Continuous DC input current (positive or negative) that can be injected into an MCU I/O pin [13]	-3	—	3	mA	—	—
IINJSUM_DC_ABS	Sum of absolute value of injected currents on all MCU I/O pins (continuous DC limit) [14]	—	—	30	mA	—	—
VDDE	DC voltage on VDDE pin	-0.3	—	6	V	—	—

1. Negative range is applicable only with external 10Kohm series resistor. Otherwise, the HVI input pin voltage range is limited to -0.3V < VHVI < 42V.
2. Negative DC voltages on the High-Side Gate (HGx) pins and Low-Side Gate (LGx) pins are only possible when the corresponding High-Side or Low-Side source pins are at a similar negative voltage. The DC differential voltage on the pre-driver pins must be higher or equal to -0.3V and may not exceed 12V: High-side drivers: 12V ≥ (HGx - HSx) ≥ -0.3V ; Low-side drivers: 12V ≥ (LGx - LSx) ≥ -0.3V.
3. Negative limit is applicable only for pulsed operation.
4. Negative range is applicable only with external series resistor populated, R ≥ 2.34KOhm.
5. If the GCTL pin is not used, it must be left unconnected.
6. For S32M24x devices, VDD_AE10, VDD and VDDA must be shorted to a common source on PCB.
7. The supply should be kept in operating conditions and once out of operating conditions, the device should be either reset or powered off. Operation with supply between 5.5 V and 5.8 V not in reset condition is allowed for 60 seconds cumulative over lifetime, the part will operate with reduced functionality. Operation with supply between 5.5 V and 5.8 V but held in reset condition by external circuit is allowed for 10 hours cumulative over lifetime.
8. While respecting the maximum current injection limit.
9. 60 seconds lifetime; device in reset (no outputs enabled/toggling)
10. 6.0 V maximum for 10 hours over lifetime; 7.0 V maximum for 60 seconds over lifetime.
11. For S32M27x devices, VDD_AE10 and VDD_HV_A must be shorted to a common source on PCB.
12. Absolute max rating must be honored under all conditions, including current injection.
13. When input pad voltage levels are close to the supply (VDD or VDD_HV_A) or VSS, practically no current injection is possible.
14. All MCU digital I/O pins are internally clamped to VSS and VDD or VDDA (S32M24x devices), or VSS and VDD_HV_A (S32M27x devices).

NOTE

All VSS or ground pins and the exposed pad must be connected in a common and single reference in the PCB.

6.2 Voltage and current operating requirements

This section describes the operating conditions of the device. All voltages are referred to VSS unless otherwise specified.

Typical conditions assumes the MCU supply (for S32M24x devices: VDD and VDDA, for S32M27x devices: VDD_VHV_A) and the ADC reference high voltage (VREFH) at 5 V, temperature = 25 °C and typical silicon process unless otherwise stated.

NOTE

Please refer to the temperature rating of the device with regards to the ambient temperature (TA) and the junction temperature (TJ).

NOTE

Device functionality is guaranteed down to the LVR assert level, however electrical performance of 12-bit ADC, CMP with 8-bit DAC, IO electrical characteristics, and communication modules electrical characteristics will be degraded when voltage drops below the minimum supply voltage.

Table 5. Voltage and current operating requirements

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VSUP	Voltage regulator and LINPHY supply voltage [1]	3.5	12	40	V	—	—
VDD_AE10	Main MCU, I/O and analog supply voltage, internally generated	3.13	3.3 or 5.0	5.5	V	—	—
VDD - VDDA	VDD-to-VDDA differential voltage (S32M24x devices) [2]	-0.1	—	0.1	V	—	—
VREFH	ADC high reference voltage (S32M242, S32M241 devices) [3]	2.7	3.3 or 5.0	VDDA + 0.1	V	—	—
VREFH	ADC high reference voltage (S32M244, S32M243 devices) [3]	3.13	3.3 or 5.0	VDDA + 0.1	V	—	—
VREFH	ADC high reference voltage (S32M27x devices) [3]	2.97	3.3 or 5.0	5.5	V	—	—
V25	Flash memory and clock supply (2.5 V), internally regulated (S32M27x devices)	—	2.5	—	V	—	—
V11	Core logic supply (1.1 V), internally regulated (S32M27x devices)	—	1.14	—	V	—	—
VGPIO	Input voltage range at any I/O or analog	-0.3	—	VDD + 0.3	V	—	—

Table continues on the next page...

Table 5. Voltage and current operating requirements (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	pin (S32M24x devices)						
VGPIO	Input voltage range at any I/O or analog pin (S32M27x devices)	-0.3	—	VDD_HV_A + 0.3	V	—	—
VODPU	Open-drain pull-up voltage (S32M24x devices) [4]	—	—	VDD	V	—	—
VODPU	Open-drain pull-up voltage (S32M27x devices) [4]	—	—	VDD_HV_A	V	—	—
IINJPAD_DC_OP	Continuous DC input current (positive/negative) that can be injected into an I/O pin (S32M24x devices) [5]	-3	—	3	mA	—	—
IINJSUM_DC_OP	Sum of absolute value of injected currents on all the I/O pins (continuous DC limit) (S32M24x devices) [5]	-30	—	30	mA	—	—
IINJPAD_DC_OP	Continuous DC input current (positive/negative) that can be injected into an I/O pin (S32M27x devices) [5]	-3	—	3	mA	VDD_HV_A >= 3.6V	—
IINJPAD_DC_OP	Continuous DC input current (positive/negative) that can be injected into an I/O pin (S32M27x devices) [5]	-2	—	3	mA	VDD_HV_A >= 2.97V	—
IINJSUM_DC_OP	Sum of absolute value of injected currents on all the I/O pins (continuous DC limit) (S32M27x devices) [5]	-30	—	30	mA	VDD_HV_A >= 3.6V	—
IINJSUM_DC_OP	Sum of absolute value of injected	-20	—	30	mA	VDD_HV_A >= 2.97V	—

Table continues on the next page...

Table 5. Voltage and current operating requirements (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	currents on all the I/O pins (continuous DC limit) (S32M27x devices) [5]						
Vramp_slow	Supply ramp rate (slow) [6]	0.5	—	—	V/min	—	—
Vramp_fast	Supply ramp rate (fast) [6]	—	—	100	V/ms	—	—

1. Normal operating range is 5.5V - 18V. Continuous operation at 40V is not allowed. Only Transient Conditions (Load Dump) single pulse tmax<400ms. Operation down to 3.5V is guaranteed without reset, however some electrical parameters are specified only in the range above 4.5V. Operation up to 32.5V (with the GDU off) is limited to 1 hour over lifetime of the device. In this range the device continues to function but electrical parameters are degraded. When bit GDUCTR_GHHDLVL is set, the GDU can operate in the range 20V < VSUP < 32.5V, also limited to 1 hour over lifetime of the device due to the over-voltage protection based on the HD pin voltage level.
2. VDD and VDDA must be shorted to a common source on PCB. The differential voltage between VDD and VDDA is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC.
3. VREFH should always be equal to or less than the supply rail + 0.1 V (VDDA + 0.1V and VDD + 0.1 V, or VDD_HV_A + 0.1V)
4. Open-drain outputs must be pulled respectively to their supply rail (VDD or VDD_HV_A).
5. When input pad voltage levels are close to the supply rails (VDD or VDD_HV_A) or VSS, practically no current injection is possible.
6. This is the device supply ramp rate, applicable to the main supply (VSUP).

6.3 Thermal operating characteristics

Table 6. Thermal operating characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Tamb_V	Ambient temperature, V-Grade parts	-40	—	105	°C	—	—
Tamb_M	Ambient temperature, M-Grade parts	-40	—	125	°C	—	—
Tamb_W	Ambient temperature, W-Grade parts	-40	—	150	°C	—	—
TJ	Junction temperature, MCU, S32M242 and S32M241	-40	—	135	°C	—	—
TJ	Junction temperature, MCU,	-40	—	150	°C	—	—

Table continues on the next page...

Table 6. Thermal operating characteristics (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	S32M276 and S32M274						
TJ	Junction temperature, MCU, S32M244 and S32M243	-40	—	170	°C	—	—
TJ	Junction temperature, AE subsystem	-40	—	175	°C	—	—

6.4 ESD and Latch-up Protection Characteristics

Table 7. ESD and Latch-up Protection Characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VHBM	Electrostatic discharge voltage, human body model (HBM), LIN pin [1,2,3]	-6000	—	6000	V	—	—
VHBM	Electrostatic discharge voltage, human body model (HBM), CANH and CANL pins [1,2,4]	-8000	—	8000	V	—	—
VHBM	Electrostatic discharge voltage, human body model (HBM), HVI0 pin [1,2,3]	-4000	—	4000	V	—	—
VHBM	Electrostatic discharge voltage, human body model (HBM), All other pins [1,2]	-2000	—	2000	V	—	—
VCDM	Electrostatic discharge voltage, charged-device model (CDM), all pins except corner [2,5]	-500	—	500	V	—	—
VCDM	Electrostatic discharge voltage, charged-device	-750	—	750	V	—	—

Table continues on the next page...

Table 7. ESD and Latch-up Protection Characteristics (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	model (CDM), corner pins [2,5]						
VESDIEC	Direct contact discharge IEC61000-4-2 (R=330, C=150pF), LIN pin, with and with out 220pF capacitor [2]	-6000	—	6000	V	—	—
VESDIEC	Direct contact discharge IEC61000-4-2 (R=330, C=150pF), HVI0 pin [2,6]	-6000	—	6000	V	Through external 10Kohm series resistor	—
VESDIEC	Direct contact discharge IEC61000-4-2 (R=330, C=150pF), CANH and CANL pins [2]	-8000	—	8000	V	—	—
ILAT	Latch-up current, MCU GPIO pins [7]	-100	—	100	mA	—	—
ILAT	Latch-up current, AE pins: CP, CP1, BST, LIN, CANH, CANL, HS, HG, LG, LS, HVI, GCTL, AMPM, AMPP, AMPOUT, VDDE, RESET_B [7,8]	-100	—	100	mA	—	—

1. This parameter is tested in conformity with AEC-Q100-002.
2. Device failure is defined as: "If after exposure to ESD pulses, the device does not meet specification requirements."
3. Pins stressed to reference group containing all ground pins.
4. Pins stressed to reference group containing all ground and supply pins.
5. This parameter is tested in conformity with AEC-Q100-011.
6. To further improve ESD/EMI robustness in case the signal to the HVI pin comes from an off-board (global) source, a 10nF GUN/ESD/ISO pulse filter capacitor can be added to the off-board HVI signal (before the 10 KΩ series resistor), placed at the off-board pin location.
7. This parameter is tested in conformity with AEC-Q100-004.
8. Positive current injection is not possible for the following pins: BST, LSx, HSx.

All ESD testing conforms with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

7 IDD current consumption and modes

See next page for IDD current consumption and modes.

Table 8. IDD current consumption

Modes	Chip		@ 25 °C			@ 85 °C			@ 105 °C			@ 125 °C			@ 150 °C		
		Unit	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
RUN Mode, core at 48 MHz	S32M242, S32M241	mA	-	47.4	TBD	-	47.7	51	-	48.5	53	-	TBD	55.7	N/A		
RUN Mode, core at 48 MHz	S32M244, S32M243	mA	-	49.7	TBD	-	TBD	TBD	-	50.2	53.5	-	51.4	57.4	-	TBD	68.5
RUN Mode, core at 48 MHz	S32M276, S32M274	mA	-	52.8	TBD	-	TBD	TBD	-	TBD	TBD	-	TBD	TBD	N/A		
RUN Mode, core at 80 MHz	S32M242, S32M241	mA	-	60.3	TBD	-	60.5	62.8	-	60.8	63.5	-	TBD	66.6	N/A		
RUN Mode, core at 80 MHz	S32M244, S32M243	mA	-	62.4	TBD	-	TBD	TBD	-	63.3	66.4	-	63.8	70.1	-	TBD	80
RUN Mode, core at 80 MHz[1]	S32M276, S32M274	mA	-	92.8	102.8	-	TBD	TBD	-	TBD	TBD	-	TBD	152.8	N/A		
RUN Mode, core at 120 MHz[1]	S32M276, S32M274	mA	-	102.8	114.8	-	TBD	TBD	-	TBD	TBD	-	TBD	162.8	N/A		
SLEEP Mode	S32M242, S32M241	µA	-	100	TBD	-	TBD	TBD	-	TBD	TBD	-	TBD	TBD	N/A		
SLEEP Mode	S32M244, S32M243	µA	-	102	TBD	-	TBD	TBD	-	TBD	TBD	-	TBD	TBD	-	TBD	TBD
DEEP_SLEEP Mode	S32M242, S32M241	µA	-	60	TBD	-	TBD	TBD	-	TBD	TBD	-	TBD	TBD	N/A		
DEEP_SLEEP Mode	S32M244, S32M243	µA	-	60	TBD	-	TBD	TBD	-	TBD	TBD	-	TBD	TBD	-	TBD	TBD
DEEP_SLEEP Mode	S32M276, S32M274	µA	-	60	TBD	-	TBD	TBD	-	TBD	TBD	-	TBD	TBD	N/A		

1. VPRE using external ballast transistor

Table 9. IDD modes

	RUN Mode, core at 48 MHz	RUN Mode, core at 80 MHz	RUN Mode, core at 120 MHz	SLEEP Mode	DEEP_SLEEP Mode
MCU supply	ON	ON	ON	ON	OFF
PLL	OFF	ON	ON	OFF	n/a (MCU unpowered)
SPI	1x LPSPI at 10Mbps, transmitting every 5 ms	1x LPSPI at 10Mbps, transmitting every 5 ms	1x LPSPI at 10Mbps, transmitting every 5 ms	OFF	n/a (MCU unpowered)
UART[1]	1x LPUART at 19200bps, every 100ms	1x LPUART at 19200bps, every 100ms	1x LPUART at 19200bps, every 100ms	OFF	n/a (MCU unpowered)
CAN-FD[2]	1x FlexCAN in loopback mode at 500 Kbit/s	1x FlexCAN in loopback mode at 500 Kbit/s	1x FlexCAN in loopback mode at 500 Kbit/s	OFF	n/a (MCU unpowered)
ADC	Converting single channel every 3 ms	Converting single channel every 3 ms	Converting single channel every 3 ms	OFF	n/a (MCU unpowered)
PWM (FTM/ eMIOS)	6x channels at 20 KHz	6x channels at 20 KHz	6x channels at 20 KHz	OFF	n/a (MCU unpowered)
Periodic Interrupt Timer (LPIT, PIT)	ON, 1ms interrupt timer	ON, 1ms interrupt timer	ON, 1ms interrupt timer	OFF	n/a (MCU unpowered)
LINPHY[1]	Connected to LPUART and transmitting	Connected to LPUART and transmitting	Connected to LPUART and transmitting	wakeup enabled	wakeup enabled
CANPHY[2]	Connected to FlexCAN and transmitting	Connected to FlexCAN and transmitting	Connected to FlexCAN and transmitting	wakeup enabled	wakeup enabled
HVM	Enabled	Enabled	Enabled	wakeup enabled	wakeup enabled

1. LINPHY devices
2. CANPHY devices

8 Application extension electrical specifications

8.1 Power management

8.1.1 PMC Electrical Specifications

Table 10. PMC Electrical Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VVPRE	VPRE output voltage	—	6.4	—	V	Internal regulation mode or external ballast mode (Internal regulator off)	—
VPRE_TON	VPRE turn on time, no external ballast	—	—	500	us	CVPRE = 2.2uF	—

Table continues on the next page...

Table 10. PMC Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
CVPRE	VPRE external load capacitor, nominal capacitance [1]	—	2.2 or 4.7	—	uF	—	—
VVLS	VLS output voltage	9.45	10	10.55	V	typ VSUP = 12.8V	—
IVLS_LD	VLS load current	—	20	40	mA	—	—
IVLS_lim	VLS current limitation	40	75	120	mA	—	—
VLS_TON	VLS turn on time	—	600	700	us	—	—
CVLS	VLS external load capacitor, nominal capacitance [1]	—	2.2 or 4.7	—	uF	—	—
V_VDD_5Vmode	VDD output voltage, in 5V mode	4.89	5	5.17	V	sel5V_3V3b=0, load conditions implemented at tester: iload = 100 mA variation over temperature range	—
V_VDD_3Vmode	VDD output voltage, in 3.3V mode	3.234	3.3	3.366	V	sel5V_3V3b=1, load conditions implemented at tester: iload = 100 mA variation over temperature range	—
IVDD_LD_FP	VDD load current, Full Power Mode	—	—	140	mA	max load current	—
IVDD_LD_LP	VDD load current, Low Power Mode	—	—	5	mA	max load current in Low Power mode	—
IVDD_ILIM	VDD current limitation	180	300	400	mA	—	—
VDD_TON	VDD turn on time	60	—	300	us	—	—
CVDD	VDD external load capacitor, nominal capacitance [1]	—	2.2 or 4.7	—	uF	—	—
VDD_REG_DYN	VDD Global regulation (peak ripple voltage)	-200	—	200	mV	Once trimmed, under dynamic load current profile	—
VDDC	VDDC output voltage	4.91	5.1	5.3	V	VPRE>=6V load conditions applied during ATE trimming: iload = 50 mA. variation over temperature range	—

Table continues on the next page...

Table 10. PMC Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IVDDC_LD	VDDC load current	—	—	70	mA	—	—
IVDDC_lim	VDDC current limitation	90	—	—	mA	—	—
VDDC_TON	VDDC turn on time	60	—	300	us	—	—
CVDDC	VDDC external load Capacitor	—	2.2 or 4.7	—	uF	Maximum deviation allowed=20%	—
VREF_FRO_FREQ	Free-running oscillator output frequency, trimmed	110	150	190	KHz	VREF_IN 2,9->5,5	—

1. All capacitors must be low ESR ceramic capacitors (for example, X7R) with 20% maximum deviation allowed.

8.1.2 Voltage Monitors in Application Extension PMC

Table 11. Voltage Monitors in Application Extension PMC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_OV1	VDD_MCU Overvoltage threshold, case1	—	—	5.55	V	5V regulation scheme	—
VDD_OV2	VDD_MCU Overvoltage threshold, case2	—	3.5	3.7	—	3.3V regulation scheme	—
VDDC_UV	VDDC (CAN-FD PHY) Undervoltage threshold	4.52	4.7	4.9	V	—	—
VLS_UV1	VLS Undervoltage threshold (alternative)	4.8	5.5	6.2	V	—	—
VLS_UV2	VLS Undervoltage threshold (default)	5.75	6.5	7.25	V	—	—

8.2 I/O Parameters

8.2.1 Application Extension IO DC electrical specifications

The following table includes the specifications for the I/O pads of the Application Extension.

Table 12. Application Extension IO DC electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IO_VIH	IO Input high voltage	0.65 * VDD_AE10	—	VDD_AE10 + 0.3	V	—	—
IO_VIL	IO Input low voltage	VSS - 0.3	—	0.35 * VDD_AE10	V	—	—
IO_VHYS_IN	IO Input voltage hysteresis	—	400	—	mV	—	—
IO_RESET_ILKG	RESET pad leakage current [1]	-2	—	2	uA	External pull up resistor of 1kohm	—
IO_RESET_FILTERED_PULSE	RESET input filtered pulse width	—	—	10	ns	—	—
IO_RESET_NOT_FILTERED_PULSE	RESET input not filtered pulse width	200	—	—	ns	—	—
IO_VDDE_ILKG	VDDE input leakage current [1]	-10	—	10	uA	—	—
IO_VDDE_IOCD	Over-current detect threshold, VDDE	—	—	175	mA	—	—
IO_VDDE_IOH_50	Maximum allowed continuous current on VDDE @ supply = 5 V	—	—	30	mA	IO_VDDE_VOH = VDD_AE10 - 0.1 V, VDD_AE10 = 5 V	—
IO_VDDE_IOH_33	Maximum allowed continuous current on VDDE @ supply = 3.3 V	—	—	20	mA	IO_VDDE_VOH = VDD_AE10 - 0.08 V, VDD_AE10 = 3.3 V	—
IO_VDDE_IOL_50	VDDE output low current @ supply = 5 V	5.5	—	—	mA	IO_VDDE_VOL = 0.8 V, VDD_AE10 = 5.0 V	—
IO_VDDE_IOL_33	VDDE output low current @supply = 3.3 V	3.5	—	—	mA	IO_VDDE_VOL = 0.8 V, VDD_AE10 = 3.3 V	—
IO_AMPOUT_ILKG	AMPOUT input leakage current [1]	-2	—	2	uA	—	—
IO_AMPOUT_IOH_50	AMPOUT output high current @ supply = 5 V	5.5	—	—	mA	IO_VOH = VDD_AE10 - 0.8 V, VDD_AE10 = 5.0 V	—
IO_AMPOUT_IOH_33	AMPOUT output high current @ supply = 3.3 V	4	—	—	mA	IO_VOH = VDD_AE10 - 0.8 V, VDD_AE10 = 3.3 V	—

Table continues on the next page...

Table 12. Application Extension IO DC electrical specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IO_AMPOUT_IOL_50	AMPOUT output low current @ supply = 5 V	6	—	—	mA	IO_VOL = 0.8 V, VDD_AE10 = 5.0 V	—
IO_AMPOUT_IOL_33	AMPOUT output low current @ supply = 3.3 V	4.5	—	—	mA	IO_VOL = 0.8 V, VDD_AE10 = 3.3 V	—

1. A positive value is leakage flowing into pin with pin at the GPIO supply level; a negative value is leakage flowing out the pin with the pin at ground.

8.2.2 High Voltage Input

The table below gives the specification for the High Voltage Input (HVI) and the Voltage Monitor (VM).

Table 13. High Voltage Input

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
HVM_ANAIV50	Analog supply current consumed by enabled analog input function [1]	—	480	—	uA	incl. Voltage divider current	—
HVM_HLWIV50	Analog supply current consumed by enabled High/Low Voltage Warning function [1]	—	360	—	uA	incl. Voltage divider current	—
HVM_DIGIV50	Additional analog supply current consumed by enabled digital input function if not near switching threshold.	—	—	1	uA	—	—
HVI_R	HVI Pin Series Resistor (external) [2]	9.5	—	10.5	kOhm	—	—
HVM_RATIO16	Input Voltage Divider Ratio16 [2,3]	—	16	—	—	—	—
HVM_RATIO11	Input Voltage Divider Ratio11 [2,3]	—	11	—	—	—	—
HVM_RATIO6	Input Voltage Divider Ratio6 [2,3]	—	6	—	—	—	—
HVM_RATIO2	Input Voltage Divider Ratio2 [2,3]	—	2	—	—	—	—
HVM_RATIO1	Input Voltage Divider Ratio1 [2,3]	—	1	—	—	—	—

Table continues on the next page...

Table 13. High Voltage Input (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
HVM_AIM	HVM Voltage Divider Matching [4]	-5	—	+5	%	Ratio 2, 6, 11, 16	—
HVM_AIM	HVM Voltage Divider Matching [4]	-8	—	+8	%	Ratio 1	—
HVM_IMP1	HVM_RATIO1 Input Impedance [5]	—	450	—	kOhm	—	—
HVM_PDIMP2	HVM Pull Down to Ground Impedance of Ratio2 Recommended ratio for external pull up open load detection. [5]	—	900	—	kOhm	—	—
HVM_PDIMP6	HVM Pull Down to Ground Impedance of Ratio6 [5]	—	540	—	kOhm	—	—
HVM_PDIMP11	HVM Pull Down to Ground Impedance of Ratio11 [5]	—	495	—	kOhm	—	—
HVM_PDIMP16	HVM Pull Down to Ground Impedance of Ratio16 [5]	—	480	—	kOhm	—	—
HVM_PUIMP2	HVM Pull Up to VDDINT Supply Impedance of Ratio2 Recommended ratio for external pull down open load detection. [5]	—	905	—	kOhm	—	—
HVM_PUIMP6	HVM Pull Up to VDDINT Supply Impedance of Ratio6 [5]	—	638	—	kOhm	—	—
HVM_PUIMP11	HVM Pull Up to VDDINT Supply Impedance of Ratio11 [5]	—	597	—	kOhm	—	—
HVM_PUIMP16	HVM Pull Up to VDDINT Supply Impedance of Ratio16 [5]	—	583	—	kOhm	—	—
HVM_PDA	HVM Post Divider Accuracy [6]	-30	—	30	mV	—	—

Table continues on the next page...

Table 13. High Voltage Input (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
HVM_VTH	HVM Digital Input Threshold HVM_VTH when down divided to: V(HVM_R)/ HVM_RATIOx The threshold is dependent of the VDDINT supply.	1	—	3.3	V	—	—
HVM_VTHT50	HVM Digital Input Typical Condition Threshold HVM_VTHT50 when down divided to: V(HVM_R)/ HVM_RATIOx	—	2.3	—	V	—	—
VM_LBI1A	Low Voltage Warning (LBI 1), Assert (Pin falling edge)	4.75	5.5	6	V	Ratio = 11 (fixed by design)	—
VM_LBI1D	Low Voltage Warning (LBI 1), Deassert (Pin rising edge)	—	—	6.5	V	Ratio = 11 (fixed by design)	—
VM_LBI1H	Low Voltage Warning (LBI 1), Hysteresis	—	0.8	—	V	Ratio = 11 (fixed by design)	—
VM_LBI2A	Low Voltage Warning (LBI 2), Assert (Pin falling edge)	5.5	6.6	7.5	V	Ratio = 11 (fixed by design)	—
VM_LBI2D	Low Voltage Warning (LBI 2), Deassert (Pin rising edge)	—	—	8	V	Ratio = 11 (fixed by design)	—
VM_LBI2H	Low Voltage Warning (LBI 2), Hysteresis	—	0.8	—	V	Ratio = 11 (fixed by design)	—
VM_LBI3A	Low Voltage Warning (LBI 3), Assert (Pin falling edge)	7	7.7	8.5	V	Ratio = 11 (fixed by design)	—
VM_LBI3D	Low Voltage Warning (LBI 3),	—	—	9	V	Ratio = 11 (fixed by design)	—

Table continues on the next page...

Table 13. High Voltage Input (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	Deassert (Pin rising edge)						
VM_LBI3H	Low Voltage Warning (LBI 3), Hysteresis	—	0.8	—	V	Ratio = 11 (fixed by design)	—
VM_LBI4A	Low Voltage Warning (LBI 4), Assert (Pin falling edge)	8	8.8	10	V	Ratio = 11 (fixed by design)	—
VM_LBI4D	Low Voltage Warning (LBI 4), Deassert (Pin rising edge)	—	—	10.5	V	Ratio = 11 (fixed by design)	—
VM_LBI4H	Low Voltage Warning (LBI 4), Hysteresis	—	0.8	—	V	Ratio = 11 (fixed by design)	—
VM_HBI1A	High Voltage Warning (HBI 1), Assert (Pin rising edge)	15.5	17	18.5	V	Ratio = 11 (fixed by design)	—
VM_HBI1D	High Voltage Warning (HBI 1), Deassert (Pin falling edge)	14.5	—	—	V	Ratio = 11 (fixed by design)	—
VM_HBI1H	High Voltage Warning (HBI 1), Hysteresis	—	1.35	—	V	Ratio = 11 (fixed by design)	—
VM_HBI2A	High Voltage Warning (HBI 2), Assert (Pin rising edge)	23.5	25.5	27	V	Ratio = 11 (fixed by design)	—
VM_HBI2D	High Voltage Warning (HBI 2), Deassert (Pin falling edge)	22.5	—	—	V	Ratio = 11 (fixed by design)	—
VM_HBI2H	High Voltage Warning (HBI 2), Hysteresis	—	1.35	—	V	Ratio = 11 (fixed by design)	—
HVM_EN_UNC	Enable Stabilization Time [7]	—	—	10	us	—	—
VM_VWPW_FILT	Voltage Warning Pulse Width Filtered	—	—	0.2	us	Ratio = 11 (fixed by design)	—

Table continues on the next page...

Table 13. High Voltage Input (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VM_VWPW_PASS	Voltage Warning Pulse Width Passing	2.5	—	—	us	Ratio = 11 (fixed by design)	—
HVM_DIPW_FILT	HVM Digital Input Pulse Width Filtered	—	—	3	us	—	—
HVM_DIPW_PASS	HVM Digital Input Pulse Width Passing	20	—	—	us	—	—

1. Analog supply currents consumed by pull up or pull down function can be calculated out of selected impedance values.
2. A resistor with value of HVI_R is required to be placed externally at HVI pin. If the signal connected to HVI_R resistor is intended to be robust versus GUN stress, the resistor type need to be capable of it. For example, the physical sizing of resistor type "0805" is large enough to avoid arching during GUN.
3. HVM_RATIO = V(HVI_R) / V(SENSE_INT). V(HVI_R) is the voltage at the resistor HVI_R. V(SENSE_INT) is the down divided internal voltage.
4. HVM_AIM=(V(HVM_R)/HVM_RATIO - V(VSENSE_INT))/(V(HVM_R)/HVM_RATIO). 0.7V < V(VSENSE_INT) < 2.3V.
5. Value includes resistor HVI_R.
6. HVM_PDA=V(SENSE_INT)-V(ADC). 0.7V<V(VSENSE_INT)<2.3V. Use for the ADC sampling time the longest available and chose the highest ADC resolution.
7. Any enable/disable of a function has the effect, for this function and also other functions, to wait for the signal to stabilize. Same applies also in case of switching the input sources.

8.3 42 MHz RC Oscillator electrical specifications

Table 14. 42 MHz RC Oscillator electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fosc	Oscillator frequency	39.28	42.24	45.19	MHz	functional mode, over PVT	—

8.4 CANPHY Electrical Specifications

Table 15. CANPHY Electrical Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
V(CANH-CANL)	Voltage between pin CANH and pin CANL	-40	—	40	V	—	—
I(VSUP)_ CANPHY_dom	VSUP current adder for CANPHY in normal mode, dominant state	—	—	62	mA	—	—
I(VSUP)_ CANPHY_rec	VSUP current adder for CANPHY in normal mode, recessive state	—	—	6	mA	—	—
VO(dom)_CANH	Dominant output voltage, pin CANH	2.75	3.5	4.5	V	RL = 50 Ω to 65 Ω	—

Table continues on the next page...

Table 15. CANPHY Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VO(dom)_CANL	Dominant output voltage, pin CANL	0.5	1.5	2.25	V	RL = 50 Ω to 65 Ω	—
VO(rec)	Recessive output voltage, pins CANH & CANL, normal mode	2	2.5	3	V	VTXD = VDD; no load	—
VO(rec)	Recessive output voltage, pins CANH & CANL, listen-only mode	2	2.5	3	V	VTXD = VDD; no load	—
VO(rec)	Recessive output voltage, pins CANH & CANL, standby mode	-0.1	—	0.1	V	no load	—
VTXsym	Transmitter voltage symmetry (VTXsym = VCANH + VCANL)	0.9 * VDDC	VDDC	1.1 * VDDC	V	CSPLIT = 4.7nF; fTXD = 250 KHz, 1 MHz or 2.5 MHz	—
VO(diff)_dom	Differential output voltage, dominant	1.5	—	3	V	RL = 45 Ω to 70 Ω; VTXD = 0 V; t< tto(dom)TXD; VDDC >= 4.75 V	—
VO(diff)_dom	Differential output voltage, dominant	1.5	—	5	V	RL = 2240 Ω; VTXD = 0 V; t< tto(dom)TXD; VDDC >= 4.75 V	—
VO(diff)_rec	Differential output voltage, recessive	-500	—	50	mV	Normal mode; VTXD = VDD; no load	—
VO(diff)_rec	Differential output voltage, recessive	-200	—	200	mV	Standby mode; no load	—
| IO(sc) |	Short-circuit output current (absolute value)	—	—	115	mA	-3 V <= VCANH <= +27 V; -15 V <= VCANL <= +10 V	—
Io(sc)rec	Recessive short-circuit output current	-3	—	3	mA	CAN Normal/Listen-only modes; -27 V <= (VCANL = VCANH) <= +32 V	—
Vth(RX)dif	Differential receiver threshold voltage, Normal or Listen only mode	0.5	0.7	0.9	V	-12 V <= VCANH <= +12 V; -12 V <= VCANL <= +12 V	—
Vth(RX)dif	Differential wake-up receiver threshold voltage	0.4	0.7	1.15	V	-12 V <= VCANH <= +12 V; -12 V <= VCANL <= +12 V	—

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Table 15. CANPHY Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Vhys(RX)dif	Differential receiver hysteresis voltage, Normal or Listen only mode	50	200	400	mV	-12 V <= VCANH <= +12 V; -12 V <= VCANL <= +12 V	—
Ri	Input resistance	—	40	50	kOhm	-2 V <= VCANH <= +7 V; -2 V <= VCANL <= +7 V	—
Ri(dif)	Input resistance deviation	-3	0	3	%	0 V <= VCANH <= +5 V; 0 V <= VCANL <= +5 V	—
td(TXDL-RXDL)	Delay time from TXD LOW to RXD LOW [1]	—	—	190	ns	RL = 45 Ω-70 Ω; CL = 100 pF; fTXD < 2,5 MHz; CRXD = 15 pF	—
td(TXDH-RXDH)	Delay time from TXD HIGH to RXD HIGH [1]	—	—	190	ns	RL = 45 Ω-70 Ω; CL = 100 pF; fTXD < 2,5 MHz; CRXD = 15 pF	—
tbit(bus)	Transmitted recessive bit width [1]	435	—	530	ns	tbit(TXD)=500 ns; RL=60 Ω; CL=100 pF; CRXD=15 pF	—
tbit(bus)	Transmitted recessive bit width [1]	155	—	210	ns	tbit(TXD)=200 ns; RL=60 Ω; CL=100 pF; CRXD=15 pF	—
Δtrec	Receiver timer symetry [1]	-65	—	+40	ns	tbit(TXD)=500 ns; RL=60 Ω; CL=100 pF; CRXD=15 pF	—
Δtrec	Receiver timer symetry [1]	-45	—	+15	ns	tbit(TXD)=200 ns; RL=60 Ω; CL=100 pF; CRXD=15 pF	—
td(TXD-busdom)	Delay time from TXD to bus dominant	—	—	80	ns	—	—
td(TXD-busrec)	Delay time from TXD to bus recessive	—	—	80	ns	—	—
td(busdom-RXD)	Delay time from bus dominant to RXD	—	—	110	ns	—	—
td(busrec-RXD)	Delay time from bus recessive to RXD	—	—	110	ns	—	—
tCPTXDDT	TXD dominant timeout	0.8	2	9	ms	NORMAL	—

1. CRXD is applied onto the AMPOUT pin with CAN-PHY configuring in certification mode (AE IO_FUNCMUX_CFG[AMPOUT_SEL]=001b, and VDD_AE10 is in 5V mode (PMC_AE CONFIG[VDD_SEL5V]=1).

8.5 LINPHY Electrical Specifications

Table 16. LINPHY Electrical Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ΔIVSUP_LIN_rec	Additional VSUP_LIN current from LIN transceiver, recessive state	—	—	1.35	mA	LIN active mode; recessive state	—
ΔIVSUP_LIN_dom	Additional VSUP_LIN current from LIN transceiver, dominant state	—	—	2.7	mA	LIN active mode; dominant state	—
IBUS_LIM	Current limitation for the LIN driver in dominant state.	40	—	200	mA	VVSUP_LIN = VLIN = 18 V; LIN Active mode; VTXD = 0 V	—
IBUS_PAS_dom	Receiver dominant input leakage current including pull-up resistor	-1	—	—	mA	VVSUP_LIN = 12 V; VLIN = 0 V; The Tx signal is set recessive	—
IBUS_PAS_rec	Receiver recessive input leakage current	—	—	20	uA	8 V < VVSUP_LIN < 28 V; 8 V < VLIN < 28 V; The Tx signal is set recessive	—
IBUS_NO_GND	Loss-of-ground bus current	-1	—	1	mA	VVSUP_LIN = VGND = 12 V; 0 V < VLIN < 18 V	—
IBUS_NO_BAT	Loss-of-battery bus current	—	—	30	uA	VVSUP_LIN = 0 V; 0 V < VLIN < 18 V; VTXD = VDD	—
VBUSdom	Receiver dominant state	—	—	0.4*VVSUP_LIN	V	4.8 V < VVSUP_LIN < 28 V; LIN Active mode	—
VBUSrec	Receiver recessive state	0.6*VVSUP_LIN	—	—	V	4.8V < VVSUP_LIN < 28 V; LIN Active mode	—
VBUS_CNT	Receiver center voltage	0.475*VVSUP_LIN	0.5*VVSUP_LIN	0.525*VVSUP_LIN	V	VBUS_CNT = (VBUSrec + VBUSdom) / 2	—
VHYS	Receiver hysteresis volage	—	—	0.175*VVSUP_LIN	V	(VHYS = VBUSrec - VBUSdom)	—
VSerDiode	Voltage drop at the series diode	0.4	0.7	1	V	Idiode = 0.9 mA	—
Rslave	Slave resistance	20	30	60	kΩ	—	—
CLIN	LIN pin capacitance	—	—	20	pF	—	—

Table continues on the next page...

Table 16. LINPHY Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
D1	Duty Cycle 1 [1]	0.396	—	—	—	Vth(rec)(max) = 0.744*VVSUP_LIN; Vth(dom)(max) = 0.581*VVSUP_LIN; tbit = 50 µs; VVSUP_LIN = 7 V to 18 V	—
D1	Duty Cycle 1 [1]	0.396	—	—	—	Vth(rec)(max) = 0.665*VVSUP_LIN; Vth(dom)(max) = 0.499*VVSUP_LIN; tbit = 50 µs; VVSUP_LIN = 4.8 V to 7 V	—
D2	Duty Cycle 2 [1]	—	—	0.581	—	Vth(rec)(max) = 0.422*VVSUP_LIN; Vth(dom)(max) = 0.284*VVSUP_LIN; tbit = 50 µs; VVSUP_LIN = 7.6 V to 18 V	—
D2	Duty Cycle 2 [1]	—	—	0.581	—	Vth(rec)(max) = 0.496*VVSUP_LIN; Vth(dom)(max) = 0.361*VVSUP_LIN; tbit = 50 µs; VVSUP_LIN = 4.8 V to 7.6 V	—
D3	Duty Cycle 3 [1]	0.417	—	—	—	Vth(rec)(max) = 0.778*VVSUP_LIN; Vth(dom)(max) = 0.616*VVSUP_LIN; tbit = 96 µs; VVSUP_LIN = 7 V to 18 V	—
D3	Duty Cycle 3 [1]	0.417	—	—	—	Vth(rec)(max) = 0.665*VVSUP_LIN; Vth(dom)(max) = 0.499*VVSUP_LIN; tbit = 96 µs; VVSUP_LIN = 4.8 V to 7 V	—
D4	Duty Cycle 4 [1]	—	—	0.59	—	Vth(rec)(max) = 0.389*VVSUP_LIN; Vth(dom)(max) = 0.251*VVSUP_LIN; tbit = 96 µs; VVSUP_LIN = 7.6 V to 18 V	—
D4	Duty Cycle 4 [1]	—	—	0.59	—	Vth(rec)(max) = 0.496*VVSUP_LIN; Vth(dom)(max) =	—

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Table 16. LINPHY Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
						0.361*VVSUP_LIN; tbit = 96 µs; VVSUP_LIN = 4.8 V to 7.6 V	
trx_pd	Receiver propagation delay	—	—	6	us	Rising and falling; CRXD = 20 pF; RRXD = 2.4 KΩ	—
trx_sym	Receiver propagation delay symmetry	-2	—	2	us	Rising edge with respect to falling edge; CRXD = 20 pF; RRXD = 2.4 KΩ	—
Cslave	Maximum capacitance allowed on slave node	—	220	250	pF	—	—
t_wake_dom_lin	LIN dominant wake-up time	30	80	150	us	—	—
t_to_dom_TXDL	TXDL dominant time-out time	5	7.2	8.6	ms	LIN active mode; VTXDL = 0 V.	—
t_det_sc	Short-circuit detection time	20	25	30	us	—	—

1. The device is compliant with LIN 2.2a.

8.6 DPGA Electrical Specifications

Table 17. DPGA Electrical Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Vin	Input voltage range[1]	0	—	Vvdda-2	V	—	—
Vout	Output voltage range	0.25	—	Vvdda-0.25	V	—	—
Vos	DPGA total input referred offset (before offset compensation) [2]	-17.5	—	17.5	mV	Tj=25C	—
Vos_comprange	DPGA offset compensation range	—	+/- 21	—	mV	—	—
Vos_compstep	DPGA input referred offset compensation step [3]	2.1	3	4	mV	—	—

Table continues on the next page...

Table 17. DPGA Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Vos_final	DPGA total input referred offset (after offset compensation)	-2	—	2	mV	Tj=25°C	—
Vos_drift	DPGA total offset voltage temperature drift over full temperature range	-7.62	—	7.62	mV	—	—
Vref	DPGA reference voltage	Vvdda/ 12-0.025	Vvdda/12	Vvdda/ 12+0.025	V	Vref=Vvdda/12, Tj=25C	—
Vref	DPGA reference voltage	Vvdda/ 6-0.03	Vvdda/6	Vvdda/ 6+0.03	V	Vref=Vvdda/6, Tj=25C	—
Vref	DPGA reference voltage	Vvdda/ 4-0.035	Vvdda/4	Vvdda/ 4+0.035	V	Vref=Vvdda/4, Tj=25C	—
Vref	DPGA reference voltage	Vvdda/ 2-0.035	Vvdda/2	Vvdda/ 2+0.035	V	Vref=Vvdda/2, Tj=25C	—
Gain	Programmable gain	7.83	7.99	8.15	—	Gain=8	—
Gain	Programmable gain	15.54	15.86	16.18	—	Gain=16	—
Gain	Programmable gain	23.81	24.30	24.79	—	Gain=24	—
Gain	Programmable gain	31.24	31.88	32.52	—	Gain=32	—
Gain	Programmable gain	38.65	39.44	40.23	—	Gain=40	—
Gain	Programmable gain	48.59	49.58	50.58	—	Gain=50	—
Gain	Programmable gain	63.43	64.72	66.02	—	Gain=65	—
Gain	Programmable gain	78.25	79.84	81.44	—	Gain=80	—
Egain	Programmable gain error	-2	—	+2	%	Gain=24	—
Elin	Linearity error [4]	-10	—	+10	mV	—	—
UGF	Unity gain band-width	—	3.5	—	MHz	Gain=8	—
UGF	Unity gain band-width	—	3.3	—	MHz	Gain=16	—
UGF	Unity gain band-width	—	2.9	—	MHz	Gain=24	—
UGF	Unity gain band-width	—	2.2	—	MHz	Gain=32	—
UGF	Unity gain band-width	—	1.8	—	MHz	Gain=40	—

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Table 17. DPGA Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
UGF	Unity gain band-width	—	1.4	—	MHz	Gain=50	—
UGF	Unity gain band-width	—	1.1	—	MHz	Gain=65	—
UGF	Unity gain band-width	—	0.9	—	MHz	Gain=80	—
Tsettle	Settling time from 1% to 99%	—	—	1.2	us	Gain=8	—
Tsettle	Settling time from 1% to 99%	—	—	1.2	us	Gain=16	—
Tsettle	Settling time from 1% to 99%	—	—	1.2	us	Gain=24	—
Tsettle	Settling time from 1% to 99%	—	—	1.6	us	Gain=32	—
Tsettle	Settling time from 1% to 99%	—	—	1.8	us	Gain=40	—
Tsettle	Settling time from 1% to 99%	—	—	2.2	us	Gain=50	—
Tsettle	Settling time from 1% to 99%	—	—	3	us	Gain=65	—
Tsettle	Settling time from 1% to 99%	—	—	3.6	us	Gain=80	—
Trecover	Recovery time from ADC sampling within 1% error	—	—	330	ns	Gain=8	—
Trecover	Recovery time from ADC sampling within 1% error	—	—	410	ns	Gain=16	—
Trecover	Recovery time from ADC sampling within 1% error	—	—	500	ns	Gain=24	—
Trecover	Recovery time from ADC sampling within 1% error	—	—	560	ns	Gain=32	—
Trecover	Recovery time from ADC sampling within 1% error	—	—	610	ns	Gain=40	—
Trecover	Recovery time from ADC sampling within 1% error	—	—	660	ns	Gain=50	—

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Table 17. DPGA Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Trecover	Recovery time from ADC sampling within 1% error	—	—	730	ns	Gain=65	—
Trecover	Recovery time from ADC sampling within 1% error	—	—	870	ns	Gain=80	—
Cload	Output load capacitance	—	—	25	pF	—	—
Ilscs	Level shifting current source	42.5	50	57.5	uA	50uA config	—
Ilscs	Level shifting current source	85	100	115	uA	100uA config	—
Ilscs	Level shifting current source	170	200	230	uA	200uA config	—
Ilscs_os	Level shifting current source mismatch	-1	—	+1	%	Tj=25C	—
Ilscs_os_drift	Level shifting current source mismatch temperature drift over full temperature	-1	—	1	%	—	—
Ilscs_trim	Level shifting current source trim step	—	0.25	—	%	—	—
Ilscs_trim_range	Level shifting current source trim range	-8	—	+8	%	—	—
Vpos_ref	Positive reference voltage	Vvdda*(48/64)	—	Vvdda*(63/64)	V	—	—
Vpos_ref_error	Positive reference voltage error	-0.005*Vvdda	—	0.005*Vvdda	V	—	—
Vneg_ref	Negative reference voltage	Vvdda*(1/64)	—	Vvdda*(16/64)	V	—	—
Vneg_ref_error	Negative reference voltage error	-0.005*Vvdda	—	0.005*Vvdda	V	—	—
Vos_cmp	Comparator offset voltage	-20	—	20	mV	—	—
tdelay_cmp	Comparator propagation delay	—	—	300	ns	Vov=10mV	—
tdelay_digi_filter	Digital time filter delay	0.35	—	2.5	us	—	—

Table continues on the next page...

Table 17. DPGA Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tdelay_ana_filter	Analog time filter delay	2.5	—	8	us	—	—

1. VIN spec is the voltage range of each individual pin (AMPP,AMPM)
2. This is the initial value after production; aging drift is not included.
3. The step can be further reduced by utilizing level shifting current source trimming.
4. Using best fit approach.

8.7 GDU Electrical Specifications

Table 18. GDU Electrical Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VHD_NOM	HD supply range MOSFETs can be turned on (normal range)	7	14	20	V	—	—
VHD_EXT	HD supply range MOSFETs can be turned on (extended range)	3.5	14	30.65	V	Operation in the range from 3.5V to 7V needs the boost regulator option to be enabled.	—
VVGS	External MOSFET VGS drive	5.5	9.3	12	V	—	—
QG	External MOSFET total gate charge @ 10 V, 40 KHz [1]	—	—	75	nC	—	—
RHSpul	Pull resistance between HGx and HSx	60	80	120	kΩ	—	—
RLSpul	Pull resistance between LGx and LSx	60	80	120	kΩ	—	—
VHVHDLA	HD high voltage monitor assert trippoint low	20	21	22.8	V	—	—
VHVHDLD	HD high voltage monitor deassert trippoint low	19.5	20.5	22.3	V	—	—
VHVHDHA	HD high voltage monitor assert trippoint high	30.65	32.5	34.6	V	—	—

Table continues on the next page...

Table 18. GDU Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VHVHDHD	HD high voltage monitor deassert trippoint high	29.65	31.5	33.6	V	—	—
tHVHD	HD high voltage monitor filter time	—	3	—	us	—	—
ADIVlow3p3	Phase & HD signal division ratio low, MCU@3.3V [2]	6.1	6.72	7.4	—	—	—
ADIVlow5p0	Phase & HD signal division ratio low, MCU@5.0V [3]	4	4.42	4.85	—	—	—
ADIVhigh3p3	Phase & HD signal division ratio high, MCU@3.3V [4]	9.5	10.5	11.5	—	—	—
ADIVhigh5p0	Phase & HD signal division ratio high, MCU@5.0V [5]	6.1	6.72	7.4	—	—	—
tGON16	HG/LG turn on time vs 7.5nF load (slew=16) [6]	—	600	—	ns	—	—
tGON23	HG/LG turn on time vs 7.5nF load (slew=23) [6]	—	300	—	ns	—	—
tGON31	HG/LG turn on time vs 7.5nF load (slew=31) [6]	—	190	—	ns	—	—
tGOFF16	HG/LG turn off time vs 7.5nF load (slew=16) [7]	—	650	—	ns	—	—
tGOFF23	HG/LG turn off time vs 7.5nF load (slew=23) [7]	—	340	—	ns	—	—
tGOFF31	HG/LG turn off time vs 7.5nF load (slew=31) [7]	—	210	—	ns	—	—
tdelon	PWM channel to HG/LG start of turn on delay [8]	—	—	500	ns	—	—
tdeloff	PWM channel to HG/LG start of turn off delay [8]	—	—	500	ns	—	—

Table continues on the next page...

Table 18. GDU Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tdelon,HS-tdeloff,LS	Inherent driver deadtime	-200	—	200	ns	—	—
tdelon,LS-tdeloff,HS	Inherent driver deadtime	-200	—	200	ns	—	—
tdeldrift	individual driver delay drift over temperature	-65	—	65	ns	—	—
tminpulse	Minimum PWM driver on/off pulse width (fastest slew)	1	—	—	us	—	—
IDRVOFF0	Gate Driver turn off current (slew=0)	1	7.2	14	mA	—	—
IDRVOFF16	Gate Driver turn off current (slew=16)	60	100	140	mA	—	—
IDRVOFF23	Gate Driver turn off current (slew=23)	140	200	270	mA	—	—
IDRVOFF31	Gate Driver turn off current (slew=31)	290	425	560	mA	—	—
IDRVON0	Gate Driver turn on current (slew=0)	-14	-7.2	-1	mA	—	—
IDRVON16	Gate Driver turn on current (slew=16)	-140	-100	-60	mA	—	—
IDRVON23	Gate Driver turn on current (slew=23)	-270	-200	-140	mA	—	—
IDRVON31	Gate Driver turn on current (slew=31)	-560	-425	-290	mA	—	—
IDRV_STEP_0_16	Gate driver current step from slew=0 to slew=16	—	6	—	mA	—	—
IDRV_STEP_16_23	Gate driver current step from slew=16 to slew=23	—	15	—	mA	—	—
IDRV_STEP_23_31	Gate driver current step from slew=23 to slew=31	—	30	—	mA	—	—
IHD	HD input current when GDU is disabled	—	0.5	—	uA	—	—
IVBS	VBSx current while high side inactive	—	—	1000	uA	—	—

Table continues on the next page...

Table 18. GDU Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ICPCG	CP driver charge current	50	112	190	mA	—	—
ICPDCG	CP driver discharge current	60	122	210	mA	—	—
fCP	Charge Pump operating frequency	62.5	—	500	kHz	—	—
fBOOST	Boost converter operating frequency	62.5	—	2500	kHz	—	—
DCBOOST	Boost converter operating duty-cycle	25	50	75	%	—	—
ICOIL0	Boost coil current limit (lowest setting)	65	135	210	mA	—	—
ICOIL7	Boost coil current limit (highest setting)	420	530	700	mA	—	—
ICOIL_STEP	Boost coil current setting step	—	56	—	mA	—	—
VBSTON	VSUP boost turn on trip point	9.5	10.1	10.8	V	—	—
VBSTOFF	VSUP boost turn off trip point	9.8	10.4	11.1	V	—	—
τdesatls	LS desaturation comparator filter time	2	4	7	us	—	—
τdesaths	HS desaturation comparator filter time	2	4	7	us	—	—
Vdesatls	LS desaturation comparator level, option 0	0.09	0.18	0.27	V	—	—
Vdesatls	LS desaturation comparator level, option 1	0.18	0.28	0.39	V	—	—
Vdesatls	LS desaturation comparator level, option 2	0.25	0.38	0.51	V	—	—
Vdesatls	LS desaturation comparator level, option 3	0.32	0.48	0.63	V	—	—

Table continues on the next page...

Table 18. GDU Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Vdesatls	LS desaturation comparator level, option 4	0.46	0.7	0.94	V	—	—
Vdesatls	LS desaturation comparator level, option 5	0.64	0.95	1.26	V	—	—
Vdesatls	LS desaturation comparator level, option 6	0.8	1.2	1.6	V	—	—
Vdesatls	LS desaturation comparator level, option 7	1	1.45	1.9	V	—	—
Vdesaths	HS desaturation comparator level (VHD-VHSx), option 0	0.09	0.18	0.27	V	—	—
Vdesaths	HS desaturation comparator level (VHD-VHSx), option 1	0.18	0.28	0.39	V	—	—
Vdesaths	HS desaturation comparator level (VHD-VHSx), option 2	0.25	0.38	0.51	V	—	—
Vdesaths	HS desaturation comparator level (VHD-VHSx), option 3	0.32	0.48	0.63	V	—	—
Vdesaths	HS desaturation comparator level (VHD-VHSx), option 4	0.46	0.7	0.94	V	—	—
Vdesaths	HS desaturation comparator level (VHD-VHSx), option 5	0.64	0.95	1.26	V	—	—
Vdesaths	HS desaturation comparator level (VHD-VHSx), option 6	0.8	1.2	1.6	V	—	—
Vdesaths	HS desaturation comparator level	1	1.45	1.9	V	—	—

Table continues on the next page...

Table 18. GDU Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	(VHD-VHSx), option 7						
ROSD_pu	Off-state diagnostics, pull-up resistor [9]	5	10.5	15	kΩ	—	—
ROSD_pd	Off-state diagnostics, pull-down resistor [9]	5	10.5	15	kΩ	—	—

1. Total gate charge spec is only a recommendation. FETs with higher gate charge can be used when resulting slew rates are tolerable by the application and resulting power dissipation does not lead to thermal overload.
2. max VHSx | VHD =20V, ADC supply=3.3V
3. max VHSx | VHD =20V, ADC supply=5V
4. max VHSx | VHD =30.65V, ADC supply=3.3V
5. max VHSx | VHD =30.65V, ADC supply=5V
6. (VBSx - HSx) = 10V respectively VLSx=10V, measured from 1V to 9V HGx/LGx vs HSx/LSx
7. (VBSx - HSx) = 10V respectively VLSx=10V, measured from 9V to 1V HGx/LGx vs HSx/LSx
8. The delay is dependent on slew rate configuration. The variation on a given device for a given slew setting is much less than the specified range.
9. ROSD_pu =~ROSD_pd, VSUP>=7V

8.8 Temperature Monitor Electrical Specifications

The table below gives the specification for the AE on-die Temperature Sensor. There are two temperature sensors, one instance located in vicinity of PMC block (TMON_PMC) and another one at the other side of AE device near the LIN and CAN physical layers (TMON_PHY).

Table 19. Temperature Monitor Electrical Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TTSENS_acc	Temperature monitor accuracy (sensor only) valid for TMON_PMC [1,2]	-5	—	5	°C	85°C < Tj < 175°C	—
TTSENS_acc	Temperature monitor accuracy (sensor only) valid for TMON_PMC [1,2,3]	-10	—	10	°C	-40°C < Tj <= 85°C	—
TTSENS_acc_offset	Temperature monitor accuracy offset (sensor only) for TMON_PHY relative to TMON_PMC	-2	—	2	°C	-40°C < Tj < 175°C	—
TOT_1	Over-temperature flag trip point, threshold 1 [3]	80	85	—	°C	—	—

Table continues on the next page...

Table 19. Temperature Monitor Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TOT_2	Over-temperature flag trip point, threshold 2	125	—	—	°C	—	—
TOT_3	Over-temperature flag trip point, threshold 3	150	—	—	°C	—	—
TOT_4	Over-temperature flag trip point, threshold 4	175	—	—	°C	—	—

1. The error caused by ADC conversion and provided temperature calculation formula is not included.
2. TMON_PHY measurements can deviate by TTSENS_acc_offset from the accuracy achievable by TMON_PMC.
3. In the lowest temperature quadrant (up to 85°C) the temperature sensor accuracy is relaxed to +/- 10°C. This includes the thresholds.

9 S32M27x MCU electrical specifications

9.1 Glitch Filter

The glitch filter parameters in the following table apply to the filters of WKPU pins and TRGMUX inputs 60-63.

Table 20. Glitch Filter

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TFILT	Glitch filter max filtered pulse width [1,2,3]	—	—	20	ns	—	—
TUNFILT	Glitch filter min unfiltered pulse width [1,3,4]	400	—	—	ns	—	—

1. An input signal pulse is defined by the duration between the input signal's crossing of a Vil/Vih threshold voltage level, and the next crossing of the opposite level.
2. Pulses shorter than defined by the maximum value are guaranteed to be filtered (not passed).
3. Pulses in between the max filtered and min unfiltered may or may not be passed through.
4. Pulses larger than defined by the minimum value are guaranteed to not be filtered (passed).

9.2 Power management

9.2.1 Supply Monitoring

Table 21. Supply Monitoring

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
LVR_VDD_HV_A	LVR on VDD_HV_A, assert threshold (in FPM)	2.77	2.85	2.93	V	—	—
LVR_VDD_HV_A	LVR on VDD_HV_A, assert threshold (in RPM)	2.77	2.85	2.93	V	—	—
—	VDD_HV_A LVR monitor hysteresis	—	18.75	—	mV	—	—
HVD_VDD_HV_A	HVD on VDD_HV_A, assert threshold (in FPM)	5.787	5.887	5.987	V	—	—
—	VDD_HV_A HVD monitor hysteresis	—	37.5	—	mV	—	—
LVD_VDD_HV_A	Low Voltage Detect (LVD5A) on VDD_HV_A, assert threshold (in FPM)	4.33	4.41	4.49	V	—	—
—	VDD_HV_A LVD monitor hysteresis	—	37.5	—	mV	—	—
VPOR_VDD_HV_A	Power-On-Reset (VPOR) on VDD_HV_A, deassert threshold	0.9	1.5	2.2	V	—	—
VREF12	Bandgap reference, trimmed	1.18	1.2	1.22	V	—	—

9.3 I/O parameters

9.3.1 GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)

Table 22. GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high level DC voltage threshold	0.70 x VDD_HV_A/B	—	VDD_HV_A/B + 0.3	V	VDD_HV_A/B = 3.3V	—

Table continues on the next page...

Table 22. GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIL	Input low level DC voltage threshold	VSS - 0.3	—	0.30 x VDD_HV_A/B	V	VDD_HV_A/B = 3.3V	—
WFRST	RESET Input Filtered pulse width [1]	—	—	33	ns	—	—
WNFRST	RESET Input not filtered pulse width [2]	100	—	—	ns	—	—
ILKG_33_S0	3.3V input leakage current for Standard GPIO [3]	-160	—	600	nA	Pins with Analog Function Count = 0	—
ILKG_33_S1	3.3V input leakage current for Standard GPIO [3]	-1020	—	870	nA	Pins with Analog Function Count = 1	—
ILKG_33_S2	3.3V input leakage current for Standard GPIO [3]	-1880	—	1140	nA	Pins with Analog Function Count = 2, plus PTA12, PTD1	—
ILKG_33_S3	3.3V input leakage current for Standard GPIO [3]	-2740	—	1410	nA	Pins with Analog Function Count = 3, plus PTD0	—
ILKG_33_SP0	3.3V input leakage current for Standard Plus GPIO and RESET IO [3]	-420	—	1270	nA	Pins with Analog Function Count = 0	—
ILKG_33_SP1	3.3V input leakage current for Standard Plus GPIO and RESET IO [3]	-1270	—	1530	nA	Pins with Analog Function Count = 1	—
ILKG_33_SP2	3.3V input leakage current for Standard Plus GPIO and RESET IO [3]	-2130	—	1800	nA	Pins with Analog Function Count = 2	—
ILKG_33_M0	3.3V GPIO input leakage current for Medium GPIO [3]	-710	—	1630	nA	Pins with Analog Function Count = 0	—
ILKG_33_M1	3.3V GPIO input leakage current for Medium GPIO [3]	-1560	—	1900	nA	Pins with Analog Function Count = 1, plus PTC16, PTD5	—
ILKG_33_I	3.3V input leakage current for GPI [3]	-120	—	120	nA	—	—
VHYS_33	Input hysteresis voltage	0.06 x VDD_HV_A/B	—	—	mV	Always enabled.	—

Table continues on the next page...

Table 22. GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
CIN	GPIO Input capacitance	2	4	6	pF	add 2pF for package/ parasitic	—
IPU_33	3.3V GPIO pull up/ down resistance	20	—	60	kΩ	pull up @ 0.3 x VDD_ HV_A/B, pull down @ 0.7 x VDD_HV_A/B	—
IOH_33_S	3.3V output high current for Standard GPIO [4,5]	1.0	—	—	mA	VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_SP	3.3V output high current for Standard Plus GPIO and RESET IO [4,5]	1.5	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_M	3.3V output high current for Medium GPIO [4,5]	3	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_SP	3.3V output high current for Standard Plus GPIO and RESET IO [4,5]	3	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_M	3.3V output high current for Medium GPIO [4,5]	6	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOL_33_S	3.3V output low current for Standard GPIO [4,5]	1.0	—	—	mA	VOL <= 0.7V	—
IOL_33_SP	3.3V output low current for Standard Plus GPIO and RESET IO [4,5]	1.5	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_33_M	3.3V output low current for Medium GPIO [4,5]	3.0	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_33_SP	3.3V output low current for Standard Plus GPIO and RESET IO [4,5]	3	—	—	mA	DSE =1, VOL <= 0.7V	—
IOL_33_M	3.3V output low current for Medium GPIO [4,5]	6	—	—	mA	DSE =1, VOL <= 0.7V	—
FMAX_33_S	3.3V maximum frequency for Standard GPIO [4,6]	—	—	10	MHz	2.9V - 3.6V, internal 5pF, PCB trace ~10pF	—

Table continues on the next page...

Table 22. GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
						and external 10pF, total 25pF load	
FMAX_33_SP	3.3V maximum frequency for Standard Plus GPIO [4,6]	—	—	25	MHz	2.9V - 3.6V, internal 5pF, PCB trace ~10pF and external 10pF, total 25pF load	—
FMAX_33_M	3.3V maximum frequency for Medium GPIO [4,6]	—	—	50	MHz	2.9V - 3.6V, internal 5pF, PCB trace ~10pF and external 10pF, total 25pF load	—

1. Maximum length of RESET pulse will be filtered by an internal filter on this pin.
2. Minimum length of RESET pulse, guaranteed not to be filtered by the internal filter.
3. A positive value is leakage flowing into pin with pin at VDD_HV_A/B (the GPIO supply level); a negative value is leakage flowing out the pin with the pin at ground.
4. GPIO output transition time information can be obtained from the device IBIS model. IBIS models are recommended for system level simulations, as discrete values for I/O transition times are not representative of the I/O pad behavior when connected to an actual transmission line load.
5. I/O output current specifications are valid for the given reference load figure, and the constraints given in the Operating Conditions of this document.
6. I/O timing specifications are valid for the un-terminated transmission line reference load given in the figure below. A lumped 8pF load is assumed at the end of a 5 inch microstrip trace on standard FR4 with approximately 1.5pF/inch (25pF total with margin). For signals with frequency greater than 63MHz, a maximum 2 inch PCB trace is assumed.

To determine total switching current on any I/O supply, current values per output pin should not be incrementally summed. I/O interfaces on the device are asynchronous to each other, so not all switching occurs at the same instant. Actual use case must be considered.

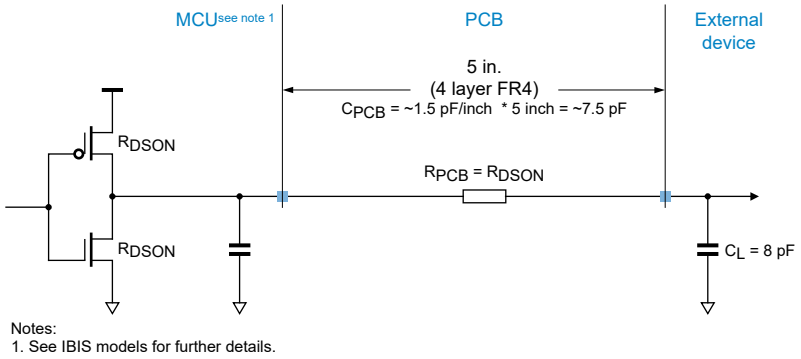


Figure 4. Reference Load Diagram

9.3.2 GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)

Table 23. GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high level DC voltage threshold	0.65 x VDD_HV_A/B	—	VDD_HV_A/B + 0.3	V	VDD_HV_A/B = 5.0V	—
VIL	Input low level DC voltage threshold	VSS - 0.3	—	0.35 x VDD_HV_A/B	V	VDD_HV_A/B = 5.0V	—
WFRST	RESET Input filtered pulse width [1]	—	—	33	ns	—	—
WNFRST	RESET Input not filtered pulse width [2]	100	—	—	ns	—	—
ILKG_50_S0	5.0V input leakage current for Standard GPIO [3]	-250	—	800	nA	Pins with Analog Function Count = 0	—
ILKG_50_S1	5.0V input leakage current for Standard GPIO [3]	-1300	—	1100	nA	Pins with Analog Function Count = 1	—
ILKG_50_S2	5.0V input leakage current for Standard GPIO [3]	-2300	—	1450	nA	Pins with Analog Function Count = 2, plus PTA12, PTD1	—
ILKG_50_S3	5.0V input leakage current for Standard GPIO [3]	-3300	—	1750	nA	Pins with Analog Function Count = 3, plus PTD0	—
ILKG_50_SP0	5.0V input leakage current for Standard Plus GPIO and RESET IO [3]	-660	—	1760	nA	Pins with Analog Function Count = 0	—
ILKG_50_SP1	5.0V input leakage current for Standard Plus GPIO and RESET IO [3]	-1510	—	2030	nA	Pins with Analog Function Count = 1	—
ILKG_50_SP2	5.0V input leakage current for Standard Plus GPIO and RESET IO [3]	-2450	—	2290	nA	Pins with Analog Function Count = 2	—
ILKG_50_M0	5.0V input leakage current for Medium GPIO [3]	-1110	—	2270	nA	Pins with Analog Function Count = 0	—
ILKG_50_M1	5.0V input leakage current for Medium GPIO [3]	-1970	—	2540	nA	Pins with Analog Function Count = 1, plus PTC16, PTD5	—

Table continues on the next page...

Table 23. GPIO DC electrical specifications, 5.0V (4.5V - 5.5V) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ILKG_50_I	5.0V input leakage current for GPI [3]	-150	—	150	nA	—	—
VHYS_50	input hysteresis voltage	0.06 x VDD_HV_A/B	—	—	mV	Always enabled.	—
CIN	GPIO Input capacitance	2	4	6	pF	add 2pF for package/ parasitic	—
IPU_50	5.0V GPIO pull up/ down resistance	20	—	55	kΩ	pull up @ 0.3 * VDD_HV_*, pull down @ 0.7 * VDD_HV_*	—
IOH_50_S	5.0V output high current Standard GPIO [4,5]	1.6	—	—	mA	VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_SP	5.0V output high current Standard Plus GPIO and RESET IO [4,5]	2.5	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_M	5.0V output high current for Medium GPIO [4,5]	4.0	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_SP	5.0V output high current for Standard Plus GPIO and RESET IO [4,5]	5.0	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_M	5.0V output high current for Medium GPIO [4,5]	8.0	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOL_50_S	5.0V output low current for Standard GPIO [4,5]	1.6	—	—	mA	VOL <= 0.7V	—
IOL_50_SP	5.0V output low current for Standard Plus GPIO and RESET IO [4,5]	2.5	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_50_M	5.0V output low current for Medium GPIO [4,5]	4.0	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_50_SP	5.0V output low current for Standard Plus GPIO and RESET IO [4,5]	5.0	—	—	mA	DSE =1, VOL <= 0.7V	—

Table continues on the next page...

Table 23. GPIO DC electrical specifications, 5.0V (4.5V - 5.5V) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOL_50_M	5.0V output low current for medium GPIO [4,5]	8.0	—	—	mA	DSE =1, VOL <= 0.7V	—
FMAX_50_S	5.0V maximum frequency for Standard GPIO [4,6]	—	—	10	MHz	3.6V - 5.5V, total 25pF load includes internal 5pF, PCB trace ~10pF and external 10pF.	—
FMAX_50_SP	5.0V maximum frequency for Standard Plus GPIO [4,6]	—	—	25	MHz	3.6V - 5.5V, total 25pF load includes internal 5pF, PCB trace ~10pF and external 10pF.	—
FMAX_50_M	5.0V maximum frequency for Medium GPIO [4,6]	—	—	25	MHz	3.6V - 5.5V, total 25pF load includes internal 5pF, PCB trace ~10pF and external 10pF	—

1. Maximum length of RESET pulse will be filtered by an internal filter on this pin.
2. Minimum length of RESET pulse, guaranteed not to be filtered by the internal filter.
3. A positive value is leakage flowing into pin with pin at VDD_HV_A/B (the GPIO supply level); a negative value is leakage flowing out the pin with the pin at ground.
4. GPIO output transition time information can be obtained from the device IBIS model. IBIS models are recommended for system level simulations, as discrete values for I/O transition times are not representative of the I/O pad behavior when connected to an actual transmission line load.
5. I/O output current specifications are valid for the given reference load figure, and the constraints given in the Operating Conditions of this document.
6. I/O timing specifications are valid for the un-terminated transmission line reference load given in the figure below. A lumped 8pF load is assumed at the end of a 5 inch microstrip trace on standard FR4 with approximately 1.5pF/inch (25pF total with margin).

To determine total switching current on any I/O supply, current values per output pin should not be incrementally summed. I/O interfaces on the device are asynchronous to each other, so not all switching occurs at the same instant. Actual use case must be considered.

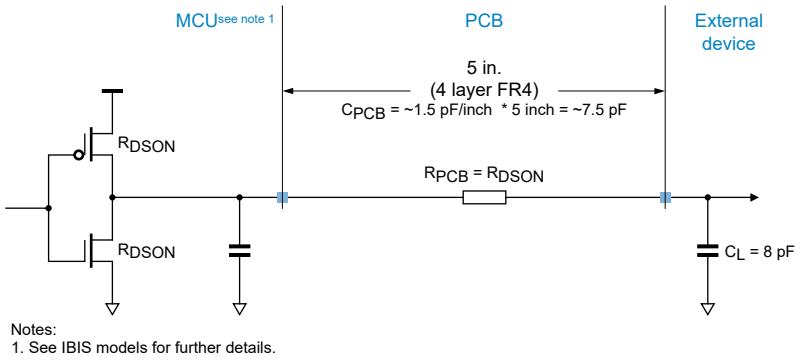


Figure 5. Reference Load Diagram

9.3.3 3.3V (2.97V - 3.63V) GPIO Output AC Specification

Table 24. 3.3V (2.97V - 3.63V) GPIO Output AC Specification

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_33_S	3.3V Standard GPIO rise/fall time	6.5	—	28	ns	Capacitance=25pF	—
TR_TF_33_S	3.3V Standard GPIO rise/fall time	11	—	43	ns	Capacitance=50pF	—
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time	4	—	17.5	ns	DSE=0, Capacitance=25pF	—
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time	2.0	—	10	ns	DSE=1, Capacitance=25pF	—
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time	8.9	—	27	ns	DSE=0, Capacitance=50pF	—
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time	4.1	—	15	ns	DSE=1, Capacitance=50pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time	2.2	—	12.3	ns	DSE=0, SRE=0, Capacitance=25pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time	3.0	—	14	ns	DSE=0, SRE=1, Capacitance=25pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time	0.8	—	6.6	ns	DSE=1, SRE=0, Capacitance=25pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time	2.4	—	10.5	ns	DSE=1, SRE=1, Capacitance=25pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time	5.1	—	17.3	ns	DSE=0, SRE=0, Capacitance=50pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time	5.8	—	19.8	ns	DSE=0, SRE=1, Capacitance=50pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time	2.2	—	10	ns	DSE=1, SRE=0, Capacitance=50pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time	3.7	—	13.9	ns	DSE=1, SRE=1, Capacitance=50pF	—

9.3.4 5.0V (4.5V - 5.5V) GPIO Output AC Specification

Table 25. 5.0V (4.5V - 5.5V) GPIO Output AC Specification

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_50_S	5.0V Standard GPIO rise/fall time	5	—	21	ns	Capacitance=25pF	—
TR_TF_50_S	5.0V Standard GPIO rise/fall time	10	—	31	ns	Capacitance=50pF	—

Table continues on the next page...

Table 25. 5.0V (4.5V - 5.5V) GPIO Output AC Specification (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time	3.5	—	13.2	ns	DSE=0, Capacitance=25pF	—
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time	1.2	—	7.1	ns	DSE=1, Capacitance=25pF	—
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time	7.1	—	18.8	ns	DSE=0, Capacitance=50pF	—
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time	3.4	—	11	ns	DSE=1, Capacitance=50pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time	1.8	—	8.2	ns	DSE=0, SRE=0, Capacitance=25pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time	2.5	—	9.8	ns	DSE=0, SRE=1, Capacitance=25pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time	0.8	—	4.5	ns	DSE=1, SRE=0, Capacitance=25pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time	1.8	—	7.2	ns	DSE=1, SRE=1, Capacitance=25pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time	4.3	—	13.2	ns	DSE=0, SRE=0, Capacitance=50pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time	4.6	—	13.8	ns	DSE=0, SRE=1, Capacitance=50pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time	1.6	—	7.1	ns	DSE=1, SRE=0, Capacitance=50pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time	2.7	—	9.6	ns	DSE=1, SRE=1, Capacitance=50pF	—

9.4 Flash memory specification

9.4.1 Flash memory program and erase specifications

Table 26. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3,4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 100,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	102	122	129	111	150		µs
t_{ppgm}	Page (256 bits) program time	142	171	180	157	200		µs
t_{qppgm}	Quad-page (1024 bits) program time	314	377	396	341	450		µs
t_{8kpgm}	8 KB Sector program time	20	24	26	22	30		ms
t_{8kers}	8 KB Sector erase time	4.8	8.5	10.6	6.5	30		ms
$t_{256kbers}$	256KB Block erase time	22.8	27.4	28.8	24.4	40	—	ms
$t_{512kbers}$	512KB Block erase time	25.4	30.5	32.1	27.9	45	—	ms
t_{1mbers}	1MB Block erase time	30.6	36.8	38.7	33.6	50	—	ms
t_{2mbers}	2MB Block erase time	41.1	49.3	51.8	45.2	60	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Sector program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 25 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤T_J ≤150°C, full spec voltage.

9.4.2 Flash memory Array Integrity and Margin Read specifications

Table 27. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1,2]	Units[3]
$t_{ai256kseq}$	Array Integrity time and Margin Read time for sequential sequence on 256KB block.	—	—	8192 x Tperiod x Nread (plus 40uS adder required if User Margin Read)	—

Table continues on the next page...

Table 27. Flash memory Array Integrity and Margin Read specifications (continued)

Symbol	Characteristic	Min	Typical	Max[1 2]	Units[3]
$t_{ai512kseq}$	Array Integrity time and Margin Read time for sequential sequence on 512KB block.	—	—	16384 x Tperiod x Nread (plus 40uS adder required if User Margin Read)	—
$t_{ai1mseq}$	Array Integrity time and Margin Read time for sequential sequence on 1MB block.	—	—	32768 x Tperiod x Nread (plus 40uS adder required if User Margin Read)	—
$t_{ai2mseq}$	Array Integrity time and Margin Read time for sequential sequence on 2MB block.	—	—	65536 x Tperiod x Nread (plus 40uS adder required if User Margin Read)	—
$t_{ai256kprop}$	Array Integrity time for proprietary sequence on 256KB block.	—	—	106496 x Tperiod x Nread	—
$t_{ai512kprop}$	Array Integrity time for proprietary sequence on 512KB block.	—	—	229376 x Tperiod x Nread	—
$t_{ai1mprop}$	Array Integrity time for proprietary sequence on 1MB block.	—	—	491520 x Tperiod x Nread	—
$t_{ai2mprop}$	Array Integrity time for proprietary sequence on 2MB block.	—	—	1048576 x Tperiod x Nread	—

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including single read, dual read, quad read contribution. Thus for a read setup that requires 6 clocks to read Nread would equal 6.
2. Array Integrity times are actual hardware execution times and do not include software overhead or system code execution overhead.
3. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

9.4.3 Flash memory module life specifications

Table 28. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 256 KB and 512 KB blocks using Sector Erase.	—	100,000	—	P/E cycles
	Number of program/erase cycles per block for 1 MB and 2 MB blocks using Sector Erase.	—	1,000	—	P/E cycles
	Number of program/erase cycles per block using Block Erase[1]	—	25	—	P/E cycles

Table continues on the next page...

Table 28. Flash memory module life specifications (continued)

Symbol	Characteristic	Conditions	Min	Typical	Units
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	20	—	Years
		Blocks with 100,000 P/E cycles.	10	—	Years

1. Program and erase supported for factory conditions. Nominal supply values and operation at 25°C.

9.4.3.1 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure.

The spec window represents qualified limits.

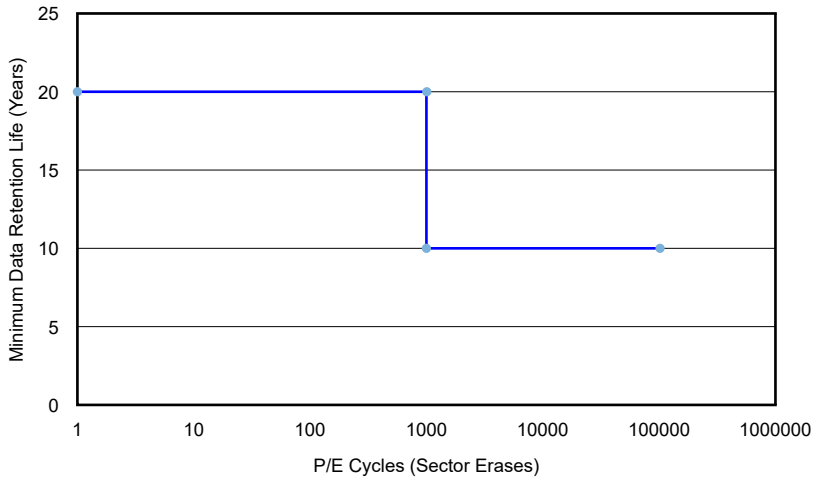


Figure 6. Data retention vs program/erase cycles

9.4.4 Flash memory AC timing specifications

Table 29. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{done}	Time from 0 to 1 transition on the MCR[EHV] bit initiating a program/erase until the MCR[DONE] bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR[EHV] bit aborting a program/erase until the MCR[DONE] bit is set to a 1.	5 plus four system clock periods	—	22 plus four system clock periods[1]	µs
t_{drcv}	Time to recover once exiting low power mode.	14 plus seven system clock periods[2]	17.5 plus seven system clock periods	21 plus seven system clock periods	µs

Table continues on the next page...

Table 29. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
$t_{aistart}$	Time from 0 to 1 transition of UT0[AIE] initiating a Margin Read or Array Integrity until the UT0[AID] bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing UT0[AISUS] or clearing UT0[NAIBP]	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0[AIE] initiating an Array Integrity abort until the UT0[AID] bit is set. This time also applies to the UT0[AISUS] to UT0[AID] setting in the event of a Array Integrity suspend request.	—	—	50 system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0[AIE] initiating a Margin Read abort until the UT0[AID] bit is set. This time also applies to the UT0[AISUS] to UT0[AID] setting in the event of a Margin Read suspend request.	—	—	26 plus fifteen system clock periods	µs

1. For Block Erase, Tdones times may be 3x max spec.
2. In extreme cases (1 block configurations) Tdrcv min may be faster (12uS plus seven system clocks)

9.4.5 Flash memory read timing parameters

Table 30. Flash Read Wait State Settings (S32M27x)

Flash Frequency	RWSC setting
250 KHz < Freq ≤ 66 MHz	1
66 MHz < Freq ≤ 100 MHz	2
100 MHz < Freq ≤ 133 MHz	3
133 MHz < Freq ≤ 167 MHz	4
167 MHz < Freq ≤ 200 MHz	5
200 MHz < Freq ≤ 233 MHz	6
233 MHz < Freq ≤ 250 MHz	7

9.5 Analog modules

9.5.1 SAR ADC

All below specs are applicable only when one ADC instance is in operation and averaging is used or multiple ADC instances are operational at the same time but sampling different channels. Best performance can be achieved if only one ADC is operational at a time sampling one channel

Table 31. SAR ADC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_HV_A	ADC Supply Voltage [1]	2.97	—	5.5	V	—	—
DVREFL	VSS / VREFL Voltage Difference [2]	-100	—	100	mV	—	—
VAD_INPUT	ADC Input Voltage [3]	VREFL	—	VREFH	V	—	—
fAD_CK	ADC Clock Frequency	10	—	120	MHz	—	—
tSAMPLE	ADC Input Sampling Time	275	—	—	ns	—	—
tCONV	ADC Total Conversion Time	1	—	—	us	12-bit result	—
tCONV	ADC Total Conversion Time	0.9	—	—	us	10-bit result	—
CAD_INPUT	ADC Input Capacitance	—	—	13.8	pF	ADC component plus pad capacitance (~2pF)	—
RAD_INPUT	ADC Input Resistance	—	—	4.6	KΩ	ADC + mux+SOC routing	—
RS	Source Impedance, precision channels	—	20	—	Ω	—	—
RS	Source Impedance, standard channels	—	20	—	Ω	—	—
TUE	ADC Total Unadjusted Error [4,5]	—	+/-4	+/-6	LSB	without adjacent pin current injection	—
TUE	ADC Total Unadjusted Error [4]	—	+/-4	+/-8	LSB	with up to +/-3mA of current injection on adjacent pins	—
IAD_REF	Current Consumption on ADC Reference pin, VREFH.	—	—	200	uA	Per ADC for dedicated or shared reference pins	—
IDDA	Current Consumption on ADC Supply, VDD_HV_A	—	2.1	—	mA	Current consumption per ADC module, ADC enabled and converting	—
CS	Sampling Capacitance	6.4 (gain=0) 9.72 pF(gain=max)	7.36 (gain=0) 11.12 pF(gain=max)	8.32 (gain=0) 12.52 (gain=max)	pF	all channels	—

Table continues on the next page...

Table 31. SAR ADC (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
RAD	Sampling Switch Impedance	80	170	520	Ohm	all channels	—
CP1	Pin capacitance	1.42	—	5.30	pF	all channels	—
CP1	Pin capacitance	1.42	—	4.38	pF	Precision channels	—
CP1	Pin capacitance	1.61	—	5.30	pF	Standard channels	—
CP2	Analog Bus Capacitance	0.32	—	4.18	pF	all channels	—
CP2	Analog Bus Capacitance	0.32	—	1.42	pF	Precision channels	—
CP2	Analog Bus Capacitance	0.497	—	4.18	pF	Standard channels	—
RSW1	Channel selection Switch impedance	65.9	—	1410	Ohm	all channels	—
RSW1	Channel selection Switch impedance	65.9	—	712	Ohm	Precision channels	—
RSW1	Channel selection Switch impedance	65.9	—	1410	Ohm	Standard channels	—

1. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC.
2. VSS and VREFL should be shorted on PCB. 100mV difference between VSS and VREFL is for transient only (not for DC).
3. This is ADC Input range for ADC accuracy guaranteed in this input range only. For SoC Pin capability, see Operation Condition Section.
4. TUE spec for precision and standard channels is based on 12-bit level resolution.
5. Spec valid if potential difference between VDD_HV_A and VREFH should follow VDD_HV_A +0.1V >=VREFH >= VDD_HV_A -1.5V

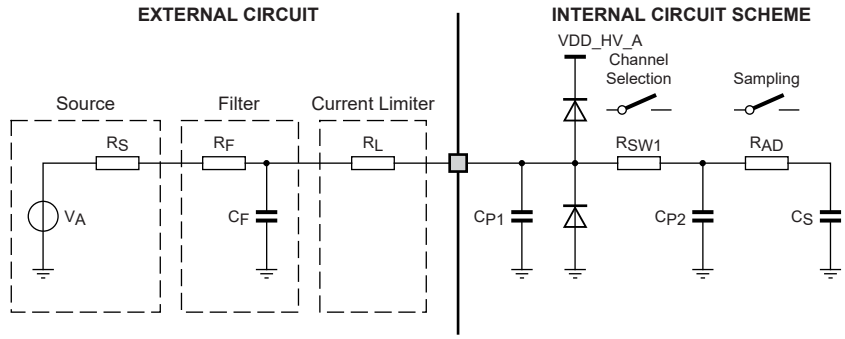


Figure 7. SAR ADC Input Circuit

9.5.2 Low Power Comparator (LPCMP)

Table 32. Low Power Comparator (LPCMP)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
idda(IDHSS)	vdda Supply Current, High Speed Mode [1,2]	—	240	—	uA	—	—
idda(IDLSS)	vdda Supply Current, Low Speed Mode [1,2]	—	17	—	uA	—	—
idda(IDHSS)	vdda Supply Current, high speed mode, DAC only [1]	—	10	—	uA	—	—
idda_lkg	vdda Supply Current, module disabled [1]	—	2	—	nA	vdda=5.5V, T=25C	—
TDHSB	Propagation Delay, High Speed Mode [3]	—	—	200	ns	—	—
TDLSB	Propagation Delay, Low Speed mode [3]	—	—	2	us	—	—
TDHSS	Propagation Delay, High Speed Mode [4]	—	—	400	ns	—	—
TDLSS	Propagation Delay, Low Speed mode [4]	—	—	5	us	—	—
TIDHS	Initialization Delay, High Speed Mode [5]	—	—	3	us	—	—
TIDLS	Initialization Delay, Low Speed mode [5]	—	—	30	us	—	—
VAIO	Analog Input Offset Voltage, High Speed Mode	-25	+/-1	25	mV	—	—
VAIO	Analog Input Offset Voltage, Low Speed mode	-40	+ /- 5	40	mV	—	—
VAHYST0	Analog Comparator Hysteresis, High Speed Mode	—	0	—	mV	HYSTCTR[1:0]= 2'b00	—
VAHYST1	Analog Comparator Hysteresis, High Speed Mode	—	14	41	mV	HYSTCTR[1:0]= 2'b01	—
VAHYST2	Analog Comparator Hysteresis, High Speed Mode	—	27	76	mV	HYSTCTR[1:0]= 2'b10	—

Table continues on the next page...

Table 32. Low Power Comparator (LPCMP) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VAHYST3	Analog Comparator Hysteresis, High Speed Mode	—	40	111	mV	HYSTCTR[1:0]= 2'b11	—
VAHYST0	Analog Comparator Hysteresis, Low Speed mode	—	0	—	mV	HYSTCTR[1:0]= 2'b00	—
VAHYST1	Analog Comparator Hysteresis, Low Speed mode	—	8	60	mV	HYSTCTR[1:0]= 2'b01	—
VAHYST2	Analog Comparator Hysteresis, Low Speed mode	—	15	113	mV	HYSTCTR[1:0]= 2'b10	—
VAHYST3	Analog Comparator Hysteresis, Low Speed mode	—	23	165	mV	HYSTCTR[1:0]= 2'b11	—
INL	DAC integral linearity [1,6,7]	-1	—	1	LSB	vrefh_cmp = vdda, vrefl_cmp = vss	—
INL	DAC integral linearity [1,6,7]	-1.5	—	1.5	LSB	vrefh_cmp < vdda	—
DNL	DAC differential linearity [1,6]	-1	—	1	LSB	vrefh_cmp = vdda, vrefl_cmp = vss	—
DNL	DAC differential linearity [1,6]	-1.5	—	1.5	LSB	vrefh_cmp < vdda	—
tDDAC	DAC Initialization time	—	—	30	us	—	—
VAIN	Analog input voltage	0	—	VDDA	V	—	—

1. vdda is comparator HV supply and internally shorted to VDD_HV_A pin. vss is comparator ground
2. Difference at input > 200mV
3. Applied +/- (100 mV + VAHYST0/1/2/3 + max. of VAIO) around switch point
4. Applied +/- (30 mV + VAHYST0/1/2/3 + max. of VAIO) around switch point
5. Applied ± (100 mV + VAHYST0/1/2/3).
6. 1 LSB = (vrefh_cmp - vrefl_cmp) /256. vrefh_cmp and vrefl_cmp are comparator reference high and low
7. Calculation method used: Linear Regression Least Square Method

For Comparator IN signals adjacent to VDD_HV_A/VDD_HV_B/VSS or XTAL/EXTAL or switching pins cross coupling may happen and hence hysteresis settings can be used to obtain the desired Comparator performance. Additionally an external capacitor to ground (1nF) should be used to filter noise on input signal. Also source drive should not be weak (Signal with <50K pull up/down is recommended).

For devices where the VDD_HV_B domain is present, LPCMP0 channels must only be selected/enabled when VDD_HV_A >= VDD_HV_B. These channels must be disabled when VDD_HV_A goes below VDD_HV_B.

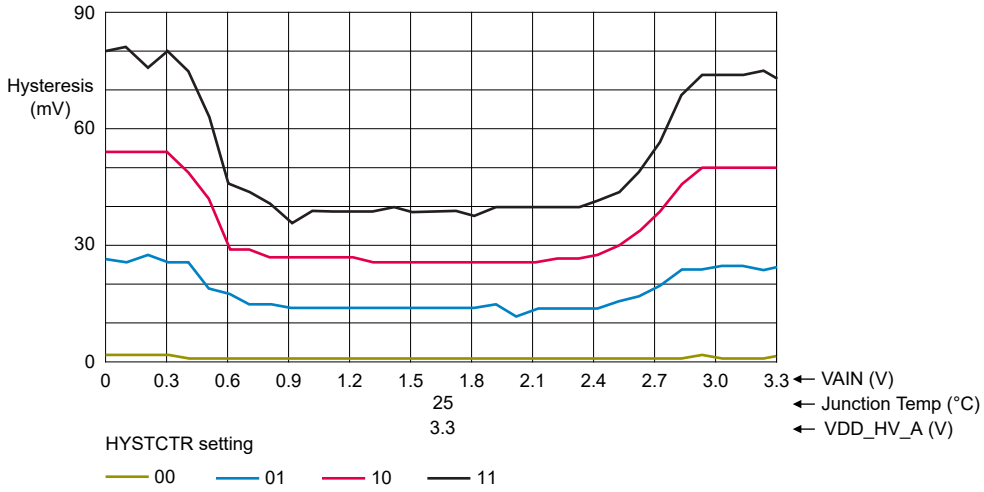


Figure 8. Typical Hysteresis vs VAIN (VDD_HV_A = 3.3 V, High Speed Mode)

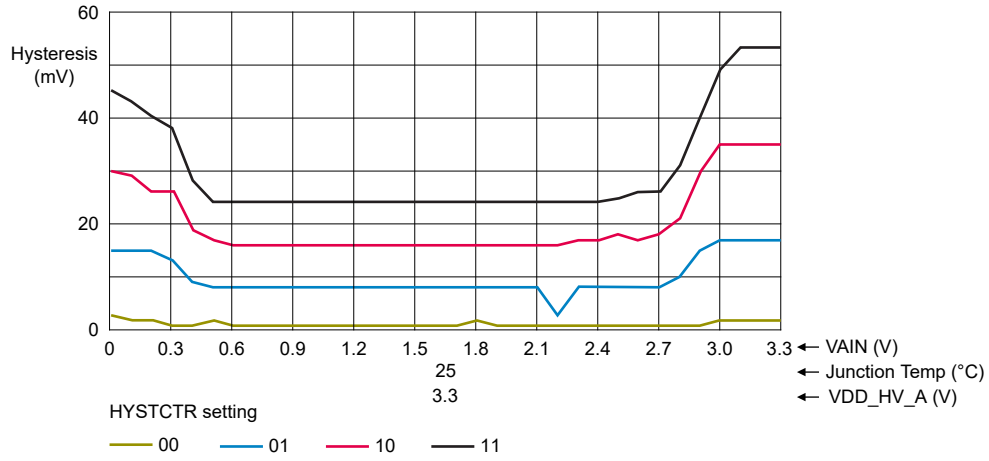


Figure 9. Typical Hysteresis vs VAIN (VDD_HV_A = 3.3 V, Low Speed Mode)

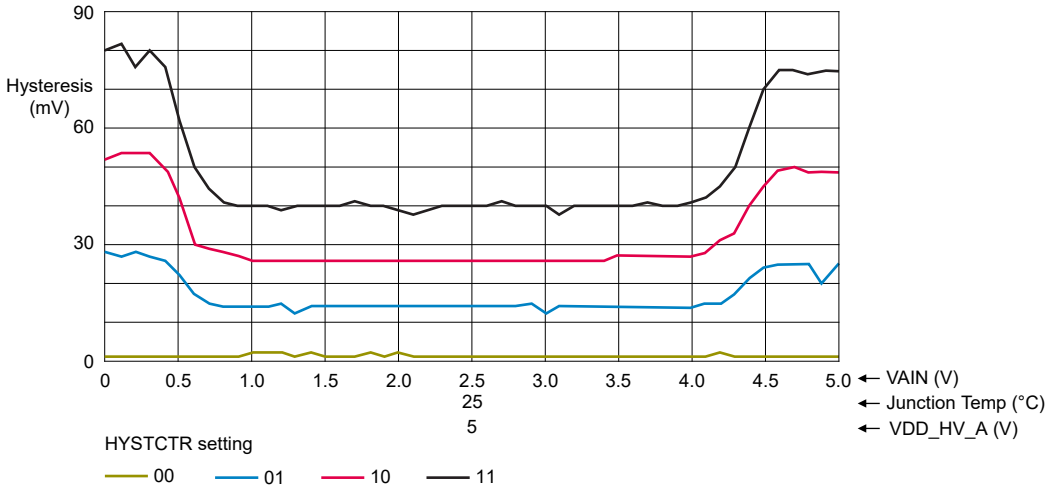


Figure 10. Typical Hysteresis vs VAIN (VDD_HV_A = 5 V, High Speed Mode).png

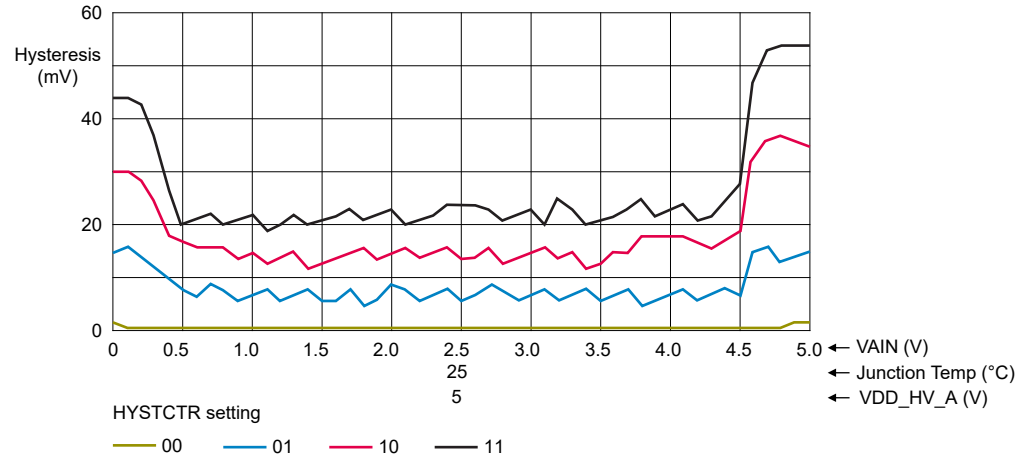


Figure 11. Typical Hysteresis vs VAIN (VDD_HV_A = 5 V, Low Speed Mode).png

9.5.3 Temperature Sensor

The table below gives the specification for the MCU on-die temperature sensor.

Table 33. Temperature Sensor

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TS_TJ	Junction temperature monitoring range	-40	—	150	°C	—	—
TS_IV25	ON state current consumption on V25	—	400	—	µA	ETS_EN=1	—
TS_ACC1	Temperature output error at circuit output (Voltage) [1,2,3]	-5	0	+5	°C	100 °C < Tj <= 150 °C	—
TS_ACC2	Temperature output error at circuit output (Voltage) [1,2,3]	-10	0	+10	°C	-40 °C <= Tj <=100 °C	—
TS_TSTART	Circuit start up time	—	4	30	µs	—	—
TS_TADCSA	Required ADC sampling time [1]	1.2	—	—	µs	—	—

1. Required ADC sampling time specified by parameter TS_TADCSA needs to be used at the ADC conversion to guarantee the specified accuracy. A smaller sampling time leads to a less accurate result.
2. Note: The temperature sensor measures the junction temperature Tj at the location where it is placed on die. The local Tj is modulated by current and previous active state of the circuit elements on die.
3. The error caused by ADC conversion and provided temperature calculation formula is not included.

9.5.4 Supply Diagnosis

The table below gives the specification for the on die supply diagnosis.

Table 34. Supply Diagnosis

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
AN_ACC	Offset to internally monitored supply at ADC input [1,2,3]	-5	0	5	%	—	—
AN_T_on	Switching time from closed (OFF) to conducting (ON) [3]	—	2.5	12	ns	—	—
AN_TADCSA	Required ADC sampling time [1]	1.2	—	—	µs	—	—

1. Required ADC sampling time specified by parameter AN_TADCSA needs to be used at the ADC conversion to guarantee the specified accuracy. A smaller sampling time leads to a less accurate result.
2. If V15 > VDD_HV_A +100mV then the V15 measurement via anamux may be imprecise.
3. These specs will have degraded performance when used in extended supply voltage operation range, i.e. normal supply voltage range specification is exceeded.

9.6 Clocking modules

9.6.1 FIRC

Table 35. FIRC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fFIRC	FIRC nominal Frequency	—	48	—	MHz	—	—
FACC	FIRC Frequency deviation across process, voltage, and temperature after trimming	-5	—	5	%	—	—
TSTART	Startup Time [1]	—	10	25	us	—	—

1. Startup time is for reference only.

9.6.2 SIRC

Table 36. SIRC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSIRC	SIRC nominal Frequency	—	32	—	KHz	—	—
fSIRC_ACC	SIRC Frequency deviation across process, voltage, and temperature after trimming	-10	—	10	%	—	—

Table continues on the next page...

Table 36. SIRC (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TSIRC_start	SIRC Startup Time [1]	—	—	3	ms	—	—
TSIRC_DC	SIRC duty cycle	30	—	70	%	—	—

1. Startup time is for information only.

9.6.3 Fast External Oscillator (FXOSC)

Table 37. Fast External Oscillator (FXOSC)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FREQ_BYPASS	Input clock frequency in bypass mode [1]	—	—	50	MHz	—	—
TRF_BYPASS	Input clock rise/fall time in bypass mode [1]	—	—	5	ns	—	—
CLKIN_DUTY_BYPASS	Input clock duty cycle in bypass mode [1]	47.5	—	52.5	%	—	—
FXOSC_CLK	output clock frequency in crystal mode	8	—	40	MHz	—	—
TFXOSC	Fxosc start up time (ALC enabled) [2]	—	—	2	ms	—	—
IFXOSC	Oscillator Analog circuit supply current, V25 supply (ALC enable)	—	—	1	mA	using 8, 16 or 40 MHz crystal	—
IFXOSC	Oscillator Analog circuit supply current, V25 supply (ALC disabled)	—	—	2.7	mA	using 8, 16 or 40 MHz crystal	—
EXTAL_SWING_PP	Peak-to-peak voltage swing on EXTAL pin in crystal oscillator mode (ALC enabled)	0.3	—	1.4	V	—	—
EXTAL_SWING_PP	Peak-to-peak voltage swing on EXTAL pin in crystal oscillator mode (ALC disabled) [3]	1.2	—	2.75	V	—	—

Table continues on the next page...

Table 37. Fast External Oscillator (FXOSC) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
CLKIN_VIL_ EXTAL_BYPASS	Input clock low level in bypass mode	0	—	vref-0.5	V	vref=0.5*VDD_HV_A	—
CLKIN_VIH_ EXTAL_BYPASS	Input clock high level in bypass mode	vref+0.5	—	VDD_HV _A	V	vref=0.5*VDD_HV_A	—
VSB	Self Bias Voltage	350	—	850	mV	—	—
GM	Amplifier Transconductance	9.7	—	18.5	mA/V	GM_SEL[3:0] = 4`b1111	—

1. For bypass mode applications, the EXTAL pin should be driven low when FXOSC is in off/disabled state.
2. The startup time specification is valid only when the recommended crystal and load capacitors are used. For higher load capacitances, the actual startup time might be higher.
3. The recommended gm setting to ensure extal swing < 2.75V at 8MHz in ALC-disabled mode is gm=4'b0010. Recommended gm settings in ALC-disabled mode for all other supported frequencies and crystals remain the same.

To ensure stable oscillations, FXOSC incorporates the feedback resistance internally.

Drive level is a crystal specification and if crystal load capacitance is increased beyond the recommended value, it may violate the crystal drive level rating. In such cases, contact NXP sales representative for selecting the correct crystal.

Crystal oscillator circuit provides stable oscillations when gmXOSC > 5 * gm_crit. The gm_crit is defined as:

$gm\_crit = 4 * (ESR + RS) * (2\pi F)^2 * (C0 + CL)^2$

where:

- gmXOSC is the transconductance of the internal oscillator circuit
- ESR is the equivalent series resistance of the external crystal
- RS is the series resistance connected between XTAL pin and external crystal for current limitation
- F is the external crystal oscillation frequency
- C0 is the shunt capacitance of the external crystal
- CL is the external crystal total load capacitance. CL = Cs+ [C1*C2/(C1+C2)]
- Cs is stray or parasitic capacitance on the pin due to any PCB traces
- C1, C2 external load capacitances on EXTAL and XTAL pins

See manufacture datasheet for external crystal component values

Figure 12. Oscillation build-up equation

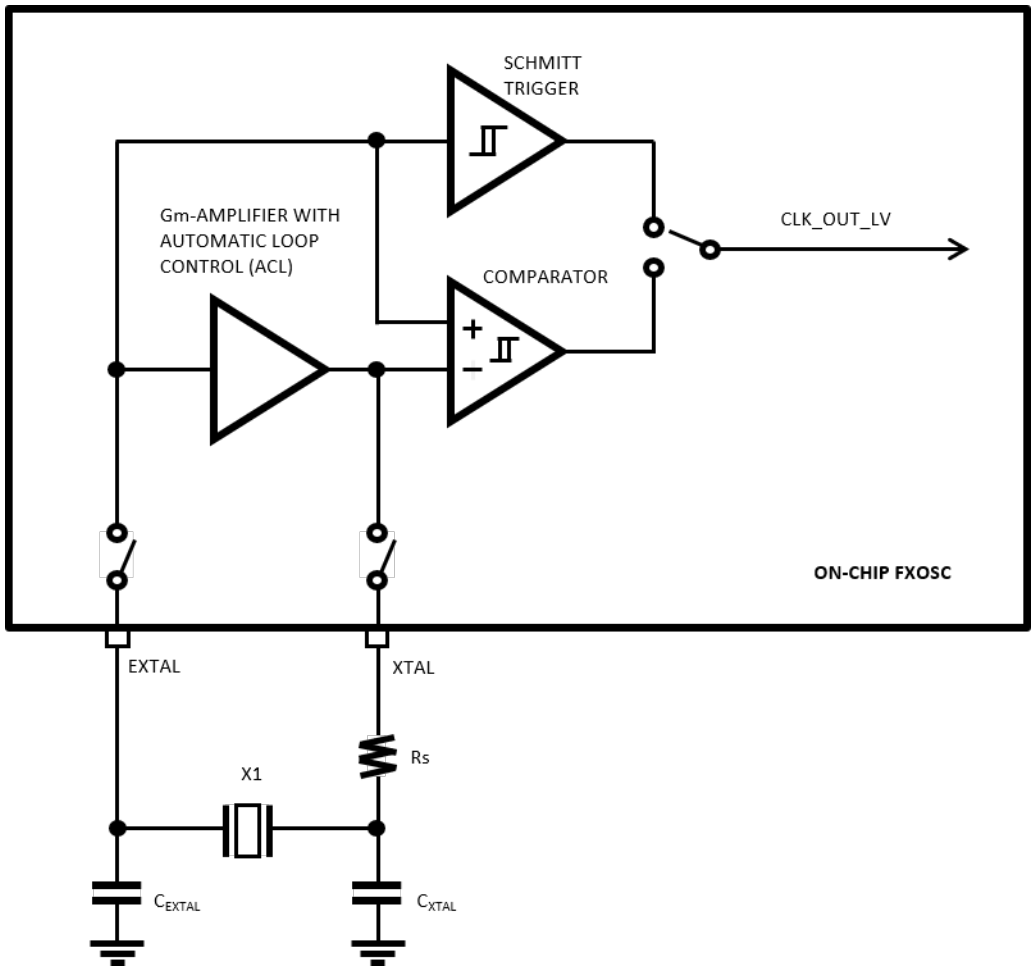


Figure 13. Block diagram

9.6.4 PLL

Jitter values specified in this table are applicable for FXOSC reference clock input only.

Table 38. PLL

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FPLL_in	PLL input frequency	8	—	40	MHz	This is the frequency after the Reference Divider within the PLL	—
FPLL_out	PLL output frequency (PLL_PHIn_CLK)	48	—	320	MHz	—	—
FPLL_vcoRange	VCO Frequency range	640	—	1280	MHz	—	—
FPLL_DS	Modulation Depth (down spread)	-0.5	—	-3	%	—	—

Table continues on the next page...

Table 38. PLL (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FPLL_FM	Modulation frequency	—	—	32	KHz	—	—
TPLL_start	PLL lock time	—	—	1	ms	—	—
JPLL_cyc	PLL period jitter (pk-pk) [1,2,3]	—	—	353	ps	FPLL_out = 120MHz, Integer Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [1,2,3]	—	—	853	ps	FPLL_out = 120MHz, Fractional Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [1,2,3]	—	—	840	ps	FPLL_out = 120MHz, Integer Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [1,2,3]	—	—	1680	ps	FPLL_out = 120MHz, Fractional Mode	—

1. Jitter numbers are valid only at IP boundary and does not include any degradation due to IO pad for clock measurement.
2. Jitter numbers calculated by extrapolating RMS jitter numbers to +/- 7 sigma .
3. For SSCG, jitter due to systematic modulation needs to be added as per applied modulation. Accumulated jitter specification is not valid with SSCG

9.7 Communication modules

9.7.1 LPSPI

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following table provides timing characteristics for classic LPSPI timing modes.

1. All timing is shown with respect to 50% VDD_HV_A/B thresholds.

2. All measurements are with maximum output load of 30 pF, input transition of 1 ns and pad configured with fastest slew setting (DSE = 1'b1).

Table 39. LPSPI

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fperiph	Peripheral Frequency [1,2,3]	—	—	40	MHz	Master	—
fperiph	Peripheral Frequency [1,2,3]	—	—	40	MHz	Slave	—
fperiph	Peripheral Frequency [1,3,4]	—	—	80	MHz	Master Loopback	—
fop	Operating frequency	—	—	15	MHz	Slave	1
fop	Operating frequency	—	—	15	MHz	Master	1
fop	Operating frequency [5]	—	—	10	MHz	Slave_10Mbps	1
fop	Operating frequency [5]	—	—	10	MHz	Master_10Mbps	1

Table continues on the next page...

Table 39. LPSPI (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fop	Operating frequency [4,6]	—	—	20	MHz	Master Loopback	1
tSPSCK	SPSCK period	66	—	—	ns	Slave	2
tSPSCK	SPSCK period	66	—	—	ns	Master	2
tSPSCK	SPSCK period [4]	50	—	—	ns	Master Loopback	2
tSPSCK	SPSCK period	100	—	—	ns	Master_10Mbps	2
tSPSCK	SPSCK period	100	—	—	ns	Slave_10Mbps	2
tLEAD	Enable lead time (PCS to SPSCK delay) [7]	tSPCK/2	—	—	ns	Slave	3
tLEAD	Enable lead time (PCS to SPSCK delay) [7]	30	—	—	ns	Master	3
tLEAD	Enable lead time (PCS to SPSCK delay) [4,7]	30	—	—	ns	Master Loopback	3
tLAG	Enable lag time (After SPSCK delay) [8]	tSPCK/2	—	—	ns	Slave	4
tLAG	Enable lag time (After SPSCK delay) [8]	30	—	—	ns	Master	4
tLAG	Enable lag time (After SPSCK delay) [4,8]	30	—	—	ns	Master Loopback	4
tWSPCK	Clock (SPSCK) time (SPSCK duty cycle) [9]	tSPSCK/ 2 - 3	—	tSPSCK/ 2 + 3	ns	Slave	5
tWSPCK	Clock (SPSCK) time (SPSCK duty cycle) [9]	tSPSCK/ 2 - 3	—	tSPSCK/ 2 + 3	ns	Master	5
tWSPCK	Clock (SPSCK) time (SPSCK duty cycle) [4,9]	tSPSCK/ 2 - 3	—	tSPSCK/ 2 + 3	ns	Master Loopback	5
tSU	Data setup time(inputs)	6	—	—	ns	Slave	6
tSU	Data setup time(inputs)	25	—	—	ns	Master	6

Table continues on the next page...

Table 39. LPSPI (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSU	Data setup time(inputs)	5	—	—	ns	Slave_10Mbps	6
tSU	Data setup time(inputs)	36	—	—	ns	Master_10Mbps	6
tSU	Data setup time(inputs) [4]	6	—	—	ns	Master_Loopback	6
tHI	Data hold time(inputs)	3	—	—	ns	Slave	7
tHI	Data hold time(inputs)	0	—	—	ns	Master	7
tHI	Data hold time(inputs)	4	—	—	ns	Slave_10Mbps	7
tHI	Data hold time(inputs)	0	—	—	ns	Master_10Mbps	7
tHI	Data hold time(inputs) [4]	3	—	—	ns	Master Loopback	7
tA	Slave access time	—	—	50	ns	Slave	8
tDIS	Slave MISO (SOUT) disable time	—	—	50	ns	Slave	9
tV	Data valid (after SPSCK edge) [10]	—	—	26	ns	Slave	10
tV	Data valid (after SPSCK edge) [10]	—	—	14	ns	Master	10
tV	Data valid (after SPSCK edge) [10]	—	—	36	ns	Slave_10Mbps	10
tV	Data valid (after SPSCK edge) [10]	—	—	21	ns	Master_10Mbps	10
tV	Data valid (after SPSCK edge) [4,10]	—	—	17.5	ns	Master Loopback	10
tHO	Data hold time (outputs) [10]	3	—	—	ns	Slave	11
tHO	Data hold time (outputs) [10]	-8	—	—	ns	Master	11
tHO	Data hold time (outputs) [10]	3	—	—	ns	Slave_10Mbps	11
tHO	Data hold time (outputs) [10]	-15	—	—	ns	Master_10Mbps	11

Table continues on the next page...

Table 39. LPSPI (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tHO	Data hold time (outputs) [4,10]	-2	—	—	ns	Master Loopback	11
tRI/FI	Rise/Fall time input [11]	—	—	1	ns	Slave	12
tRI/FI	Rise/Fall time input [11]	—	—	1	ns	Master	12
tRI/FI	Rise/Fall time input [4,11]	—	—	1	ns	Master Loopback	12

1. tperiph = 1/fperiph
2. For LPSPI0 instance, max. peripheral frequency is equal to AIPS_PLAT_CLK.
3. fperiph = LPSPI peripheral clock
4. Master Loopback mode: In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1.
5. These specifications apply to the SPI operation, as master or slave, at up to 10 Mbps for the combinations not indicated in the table below. Unless otherwise noted, all other ‘master’ and ‘slave’ specifications are also applicable in the 10Mbps configurations. See table "LPSPI 20 MHz and 15 MHz Combinations.
6. LPSPI0 support up to 20MHz on fast pin.
7. Minimum configuration value for CR[PCSSCK] field is 3(0x00000011).
8. Minimum configuration value for CCR[SCKPCS] field is 3(0x00000011).
9. While selecting odd dividers, ensure Duty Cycle is meeting this parameter.
10. Output rise/fall time is determined by the output load and GPIO pad drive strength setting. See the GPIO specifications for detail.
11. The input rise/fall time specification applies to both clock and data, and is required to guarantee related timing parameters.

fperiph = LPSPI peripheral clock

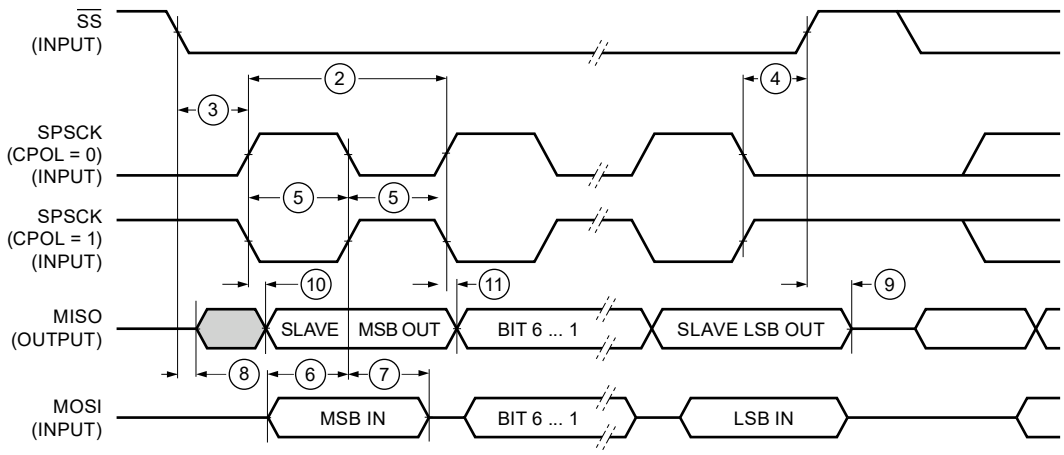


Figure 14. LPSPI Slave Mode Timing (CPHA=1)

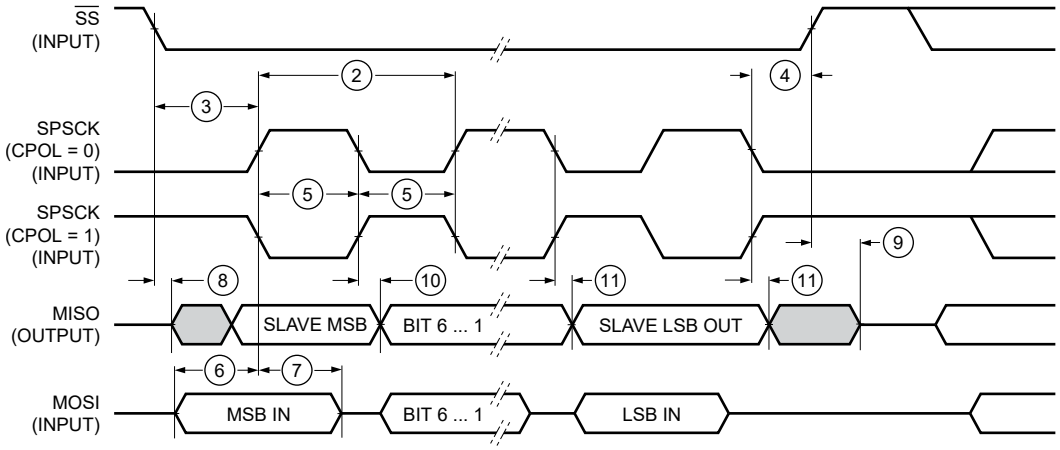


Figure 15. LPSPI Slave Mode Timing (CPHA=0)

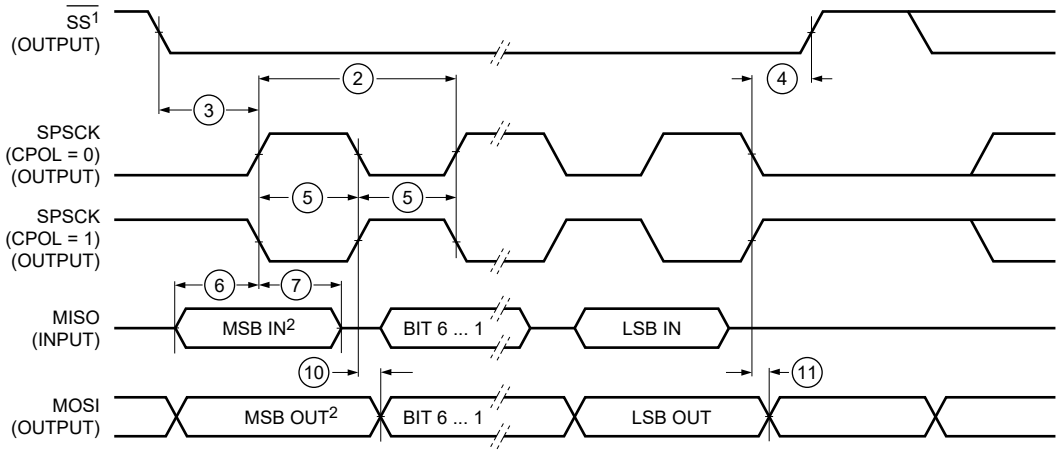


Figure 16. LPSPI Master Mode Timing (CPHA=0)

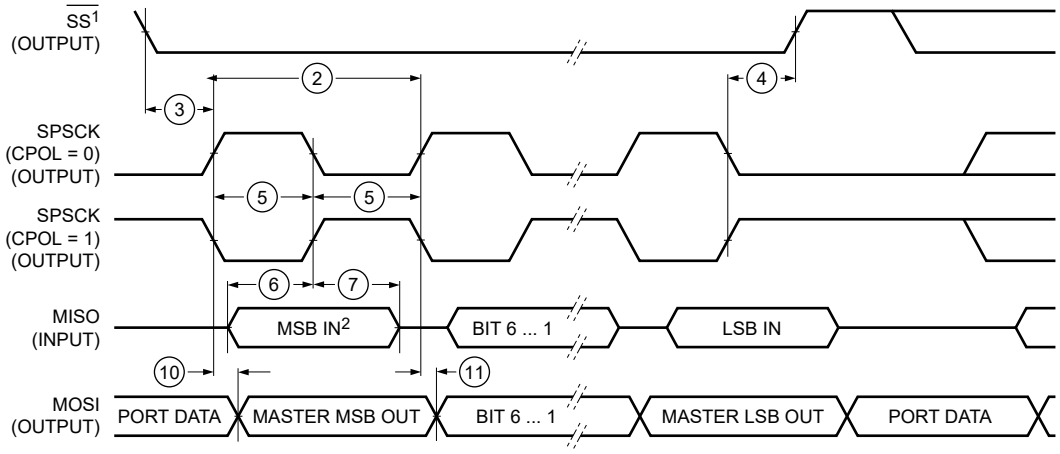


Figure 17. LPSPI Master Mode Timing (CPHA=1)

9.7.2 I2C

See I/O parameters for I^2C specification.

For supported baud rate see section 'Chip-specific LPI2C information' of the Reference Manual.

9.7.3 FlexCAN characteristics

See I/O parameters for FlexCAN specification.

For supported baud rate, see section 'Protocol timing' of the Reference Manual.

9.7.4 LPUART specifications

See I/O parameters for LPUART specifications.

9.8 Debug modules

9.8.1 JTAG electrical specifications

The following table describes the JTAG electrical characteristics. These specifications apply to JTAG and boundary scan. Measurements are with maximum output load of 30pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0.

Table 40. JTAG electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tJCYC	TCK cycle time [1,2]	30	—	—	ns	—	1
tJDC	TCK clock pulse width	40	—	60	%	—	2
tTCKRISE	TCK rise/fall times (40%-70%)	—	—	1	ns	—	3
tTMSS, tTDIS	TMS, TDI data setup time	5	—	—	ns	—	4
tTMSH, tTDIH	TMS, TDI data hold time	5	—	—	ns	—	5
tTDOV	TCK low to TDO data valid [3]	—	—	22	ns	—	6
tTDOI	TCK low to TDO data invalid	0	—	—	ns	—	7
tTDOHZ	TCK low to TDO high impedance	—	—	22	ns	—	8
tBSDV	TCK falling edge to output valid [4]	—	—	600	ns	—	11
tBSDVZ	TCK falling edge to output valid out of high impedance	—	—	600	ns	—	12
tBSDHZ	TCK falling edge to output high impedance	—	—	600	ns	—	13

Table continues on the next page...

Table 40. JTAG electrical specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tBSDST	Boundary scan input valid to TCK rising edge	15	—	—	ns	—	14
tBSDHT	TCK rising edge to boundary scan input invalid	15	—	—	ns	—	15

1. Cycle time is 30ns assuming full cycle timing. Cycle time is 60ns assuming half cycle timing.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

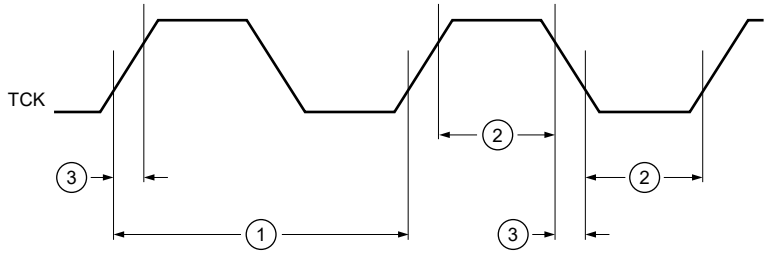


Figure 18. JTAG TCK Input Timing

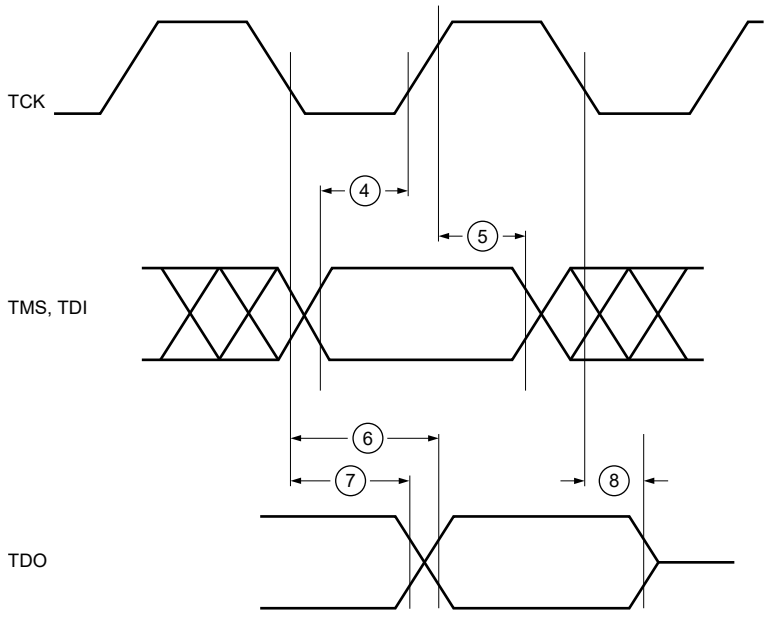


Figure 19. JTAG Test Access Port Timing

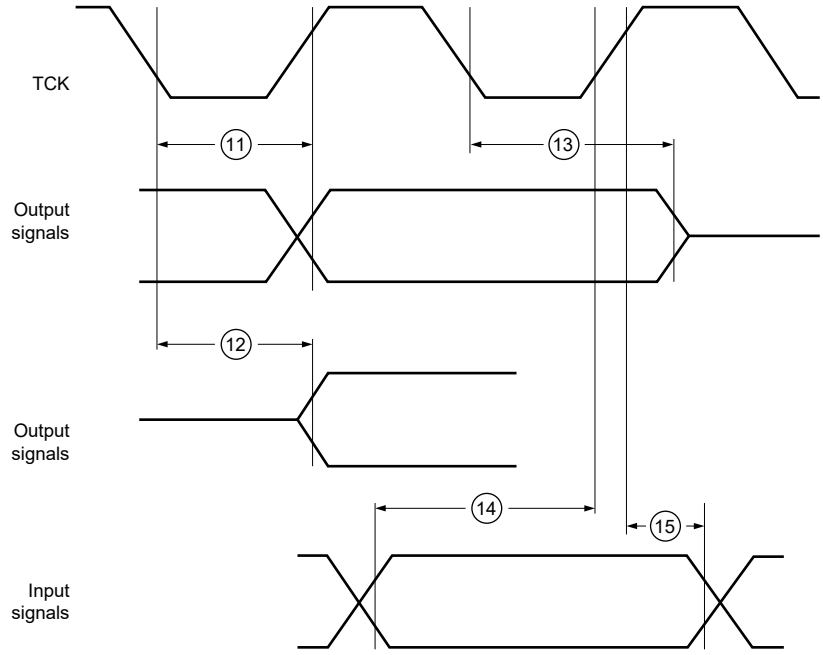


Figure 20. Boundary Scan Timing

9.8.2 SWD electrical specifications

The following table describes the SWD electrical characteristics. Measurements are with maximum output load of 30pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0.

Table 41. SWD electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S1	SWD_CLK frequency	—	—	33	MHz	—	S1
S2	SWD_CLK cycle period	1 / S1	—	—	ns	—	S2
S3	SWD_CLK pulse width	40	—	60	%	—	S3
S4	SWD_CLK rise and fall times	—	—	1	ns	—	S4
S9	SWD_DIO input data setup time to SWD_CLK rise	5	—	—	ns	—	S9
S10	SWD_DIO input data hold time after SWD_CLK rising edge	5	—	—	ns	—	S10

Table continues on the next page...

Table 41. SWD electrical specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S11	SWD_CLK high to SWD_DIO output data valid	—	—	22	ns	—	S11
S12	SWD_CLK high to SWD_DIO output data hi-Z	—	—	22	ns	—	S12
S13	SWD_CLK high to SWD_DIO output data invalid	0	—	—	ns	—	S13

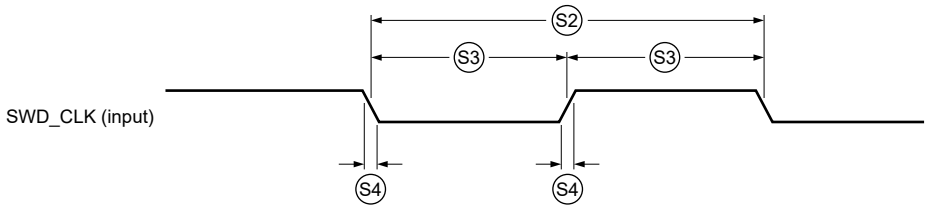


Figure 21. SWD Input Clock Timing

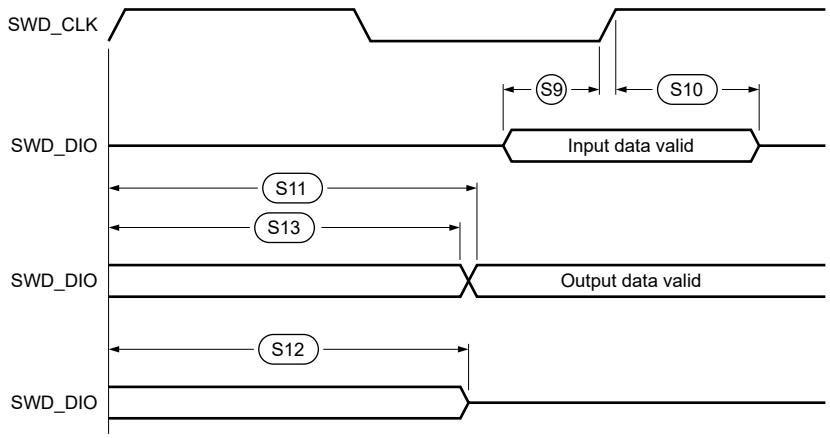


Figure 22. SWD Output Data Timing

10 S32M24x MCU electrical specifications

10.1 General

10.1.1 LVR, LVD and POR operating requirements

Table 42. V_{DD} supply LVR, LVD and POR operating requirements for S32M241 and S32M242 series[1]

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and falling V_{DD} POR detect voltage	1.1	1.6	2.0	V	

Table continues on the next page...

Table 42. V_{DD} supply LVR, LVD and POR operating requirements for S32M241 and S32M242 series[1] (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVR}	LVR falling threshold (RUN, HSRUN, and STOP modes)	2.50	2.58	2.7	V	
V_{LVR_HYST}	LVR hysteresis	—	45	—	mV	[2]
V_{LVR_LP}	LVR falling threshold (VLPS/VLPR modes)	1.97	2.22	2.44	V	
V_{LVD}	Falling low-voltage detect threshold	2.8	2.875	3	V	
V_{LVD_HYST}	LVD hysteresis	—	50	—	mV	[2]
V_{LVW}	Falling low-voltage warning threshold	4.19	4.305	4.5	V	
V_{LVW_HYST}	LVW hysteresis	—	75	—	mV	[2]
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	

1. In 3.3 V range, the VLVW is always set since supply remains below VLVW range. Hence PMC.LVDSC2[LVWIE] should remain cleared while device operates in 3.3 V range.
2. Rising threshold is the sum of falling threshold and hysteresis voltage.

Table 43. V_{DD} supply LVR and POR operating requirements for S32M243 and S32M244 series[1]

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and falling V_{DD} POR detect voltage	1.1	1.6	2.0	V	
V_{LVR}	LVR falling threshold (RUN and STOP modes)	2.95	3.02	3.07	V	
V_{LVR_HYST}	LVR hysteresis	—	45	—	mV	[2]
V_{LVR_LP}[3]	LVR falling threshold (VLPS/VLPR modes)	2.06	2.26	2.46	V	
V_{LVW}	Falling low-voltage warning threshold	4.17	4.305	4.5	V	
V_{LVW_HYST}	LVW hysteresis	—	75	—	mV	[2]
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	

1. In 3.3 V range, the VLVW is always set since supply remains below VLVW range. Hence PMC.LVDSC2[LVWIE] should remain cleared while device operates in 3.3 V range.
2. Rising threshold is the sum of falling threshold and hysteresis voltage.
3. An internal monitor could reset the chip at a higher supply level, but 3.13 V onward the chip is fully functional.

10.1.2 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration:

Table 44. Clock configuration

	S32M241 and S32M242	S32M243 and S32M244
RUN mode		
Clock source	FIRC	FIRC

Table continues on the next page...

Table 44. Clock configuration (continued)

	S32M241 and S32M242	S32M243 and S32M244
SYS_CLK/CORE_CLK	48 MHz	48 MHz
BUS_CLK	48 MHz	48 MHz
FLASH_CLK	24 MHz	16 MHz
VLPR mode		
Clock source	SIRC	SIRC
SYS_CLK/CORE_CLK	4 MHz	1 MHz
BUS_CLK	4 MHz	1 MHz
FLASH_CLK	1 MHz	0.25
STOP1/STOP2 mode		
Clock source	FIRC	FIRC
SYS_CLK/CORE_CLK	48 MHz	48 MHz
BUS_CLK	48 MHz	48 MHz
FLASH_CLK	24 MHz	16 MHz
VLPS mode		
	All clock source disabled	

Table 45. Power mode transition operating behaviors for S32M241 and S32M242 series

Symbol	Description	Min.	Typ.	Max.	Unit
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 2.7 V to execution of the first instruction across the operating temperature range of the chip.	—	325	—	µs
	VLPS → RUN	8	—	17	µs
	STOP1 → RUN	0.07	0.075	0.08	µs
	STOP2 → RUN	0.07	0.075	0.08	µs
	VLPR → RUN	19	—	26	µs
	VLPR → VLPS	5.1	5.7	6.5	µs
	VLPS → VLPR	18.8	23	27.75	µs
	RUN → Compute operation	0.72	0.75	0.77	µs
	RUN → STOP1	0.35	0.38	0.4	µs
	RUN → STOP2	0.2	0.23	0.25	µs
	RUN → VLPS	0.3	0.35	0.4	µs
	RUN → VLPR	3.5	3.8	5	µs
	VLPS → Asynchronous DMA Wakeup	105	110	125	µs
	STOP1 → Asynchronous DMA Wakeup	1	1.1	1.3	µs

Table continues on the next page...

Table 45. Power mode transition operating behaviors for S32M241 and S32M242 series (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	STOP2 → Asynchronous DMA Wakeup	1	1.1	1.3	µs
	Pin reset → Code execution	—	214	—	µs

Table 46. Power mode transition operating behaviors for S32M243 and S32M244 series

Symbol	Description	Min.	Typ.	Max.	Unit
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 3.13 V to execution of the first instruction across the operating temperature range of the chip.	—	375	—	µs
	VLPS → RUN	8	—	17	µs
	STOP1 → RUN	0.07	0.075	0.08	µs
	STOP2 → RUN	0.07	0.075	0.08	µs
	VLPR → RUN	152	—	208	µs
	VLPR → VLPS	25	34	39	µs
	VLPS → VLPR	18.8	23	27.75	µs
	RUN → Compute operation	0.72	0.75	0.77	µs
	RUN → STOP1	0.35	0.38	0.4	µs
	RUN → STOP2	0.2	0.23	0.25	µs
	RUN → VLPS	0.3	0.35	0.4	µs
	RUN → VLPR	7	7.6	10	µs
	VLPS → Asynchronous DMA Wakeup	105	110	125	µs
	STOP1 → Asynchronous DMA Wakeup	1	1.1	1.3	µs
	STOP2 → Asynchronous DMA Wakeup	1	1.1	1.3	µs
	Pin reset → Code execution	—	255	—	µs

10.2 I/O parameters

10.2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

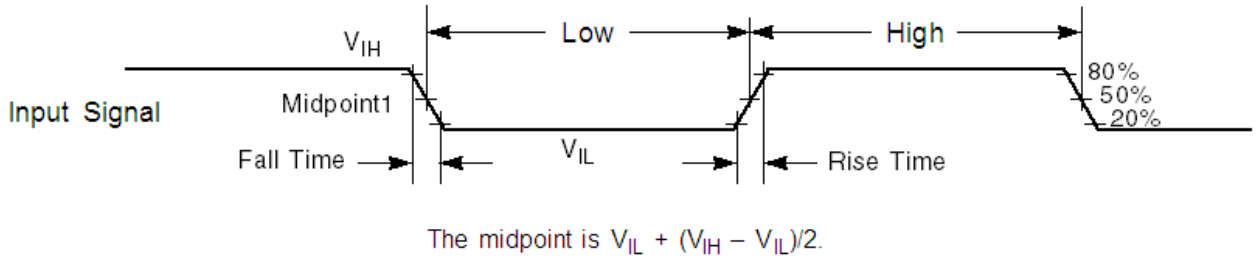


Figure 23. Input signal measurement reference

10.2.2 General AC specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 47. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	3
WFRST	$\overline{\text{RESET}}$ input filtered pulse	—	10	ns	4
WNFRST	$\overline{\text{RESET}}$ input not filtered pulse	Maximum of (100 ns, bus clock period)	—	ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop and VLPS modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. Maximum length of $\overline{\text{RESET}}$ pulse which will be the filtered by internal filter only if PCR_PTA5[PFE] is at its reset value of 1'b1.
5. Minimum length of $\overline{\text{RESET}}$ pulse, guaranteed not to be filtered by the internal filter only if PCR_PTA5[PFE] is at its reset value of 1'b1. This number depends on the bus clock period also. In this case, minimum pulse width which will cause reset is 250 ns. For faster clock frequencies which have clock period less than 100 ns, the minimum pulse width not filtered will be 100 ns. After this filtering mechanism, the software has an option to put additional filtering in addition to this, by means of PCM_RPC register and/or PORT_DFER register for PTA5.

10.2.3 DC electrical specifications at 3.3 V Range

NOTE

For details on the pad types defined in Table 48 and Table 50, see Reference Manual section *IO Signal Table* and IO Signal Description Input Multiplexing sheet(s) attached with Reference Manual.

Table 48. DC electrical specifications at 3.3 V Range for S32M242 series

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	2.7	3.3	4	V	
V_{ih}	Input Buffer High Voltage	0.7 × V_{DD}	—	V_{DD} + 0.3	V	1
V_{il}	Input Buffer Low Voltage	V_{SS} − 0.3	—	0.3 × V_{DD}	V	2
V_{hys}	Input Buffer Hysteresis	0.06 × V_{DD}	—	—	V	
Ioh_{GPIO} $Ioh_{GPIO\text{-}HD\_DSE\_0}$	I/O current source capability measured when pad V_{oh} = (V_{DD} − 0.8 V)	3.5	—	—	mA	
Iol_{GPIO} $Iol_{GPIO\text{-}HD\_DSE\_0}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	3	—	—	mA	
$Ioh_{GPIO\text{-}HD\_DSE\_1}$	I/O current source capability measured when pad V_{oh} = (V_{DD} − 0.8 V)	14	—	—	mA	3
$Iol_{GPIO\text{-}HD\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	12	—	—	mA	3
$Ioh_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{oh}=V_{DD}-0.8 V	9.5	—	—	mA	4
$Iol_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	10	—	—	mA	4
$Ioh_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{oh}=V_{DD}-0.8 V	16	—	—	mA	4
$Iol_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	15.5	—	—	mA	4
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 3.3 V	—	5	500[5]	nA	6
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins		0.010	0.5	µA	
R_{PU}	Internal pullup resistors	20		60	kΩ	7
R_{PD}	Internal pulldown resistors	20		60	kΩ	8

1. For reset pads, same V_{ih} levels are applicable
2. For reset pads, same V_{il} levels are applicable
3. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
4. For refernce only. Run simulations with the IBIS model and custom board for accurate results.
5. Typical leakage is given at room temperature. Maximum is given for 125°C. Leakage numbers increase with temperature, approximately every 12 – 14°C the value doubles. Leakage is tested at hot temperature. We ensure maximums are not exceeded. Please note that when the ADC module samples a pin, additional currents beyond the leakage number are drawn to charge the sample and hold capacitances and internal analog busses. These are difficult to predict.
6. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details see IO Signal Description Input Multiplexing sheet(s) attached with the *Reference Manual*.
7. Measured at input V = V_{SS}

8. Measured at input V = V_{DD}

Table 49. DC electrical specifications at 3.3 V Range for S32M244 series

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	3.13	3.3	4	V	
V_{ih}	Input Buffer High Voltage	0.7 × V_{DD}	—	V_{DD} + 0.3	V	1
V_{il}	Input Buffer Low Voltage	V_{SS} − 0.3	—	0.3 × V_{DD}	V	2
V_{hys}	Input Buffer Hysteresis	0.06 × V_{DD}	—	—	V	
Ioh_{GPIO} $Ioh_{GPIO\text{-}HD\_DSE\_0}$	I/O current source capability measured when pad V_{oh} = (V_{DD} − 0.8 V)	3.5	—	—	mA	
Iol_{GPIO} $Iol_{GPIO\text{-}HD\_DSE\_0}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	3	—	—	mA	
$Ioh_{GPIO\text{-}HD\_DSE\_1}$	I/O current source capability measured when pad V_{oh} = (V_{DD} − 0.8 V)	14	—	—	mA	3
$Iol_{GPIO\text{-}HD\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	12	—	—	mA	3
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 3.3 V					4
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins (excluding XTAL pin)		0.010	0.5	µA	
	XTAL pin (PTB6) temperature ≤ 125° C		0.010	0.5	µA	
	XTAL pin (PTB6) temperature ≥ 125° C			1.1	µA	
R_{PU}	Internal pullup resistors	20		60	kΩ	5
R_{PD}	Internal pulldown resistors	20		60	kΩ	6

1. For reset pads, same V_{ih} levels are applicable
2. For reset pads, same V_{il} levels are applicable
3. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
4. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details see IO Signal Description Input Multiplexing sheet(s) attached with the *Reference Manual*.
5. Measured at input V = V_{SS}
6. Measured at input V = V_{DD}

10.2.4 DC electrical specifications at 5.0 V Range

Table 50. DC electrical specifications at 5.0 V Range for S32M242 series

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage	0.65 x V_{DD}	—	V_{DD} + 0.3	V	1
V_{il}	Input Buffer Low Voltage	V_{SS} − 0.3	—	0.35 x V_{DD}	V	2
V_{hys}	Input Buffer Hysteresis	0.06 x V_{DD}	—	—	V	
Ioh_{GPIO} $Ioh_{GPIO\text{-}HD\_DSE\_0}$	I/O current source capability measured when pad V_{oh}= (V_{DD} - 0.8 V)	5	—	—	mA	
Iol_{GPIO} $Iol_{GPIO\text{-}HD\_DSE\_0}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	5	—	—	mA	
$Ioh_{GPIO\text{-}HD\_DSE\_1}$	I/O current source capability measured when pad V_{oh} = V_{DD} - 0.8 V	20	—	—	mA	3
$Iol_{GPIO\text{-}HD\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	20	—	—	mA	3
$Ioh_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{oh} = V_{DD} - 0.8 V	14.0	—	—	mA	4
$Iol_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	14.5	—	—	mA	4
$Ioh_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{oh} = V_{DD} - 0.8 V	21	—	—	mA	4
$Iol_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	20.5	—	—	mA	4
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 3.3 V	—	5	500[5]	nA	6
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins (excluding XTAL pin)		0.010	0.5	µA	
	XTAL pin (PTB6) temperature ≤ 125° C		0.010	0.5	µA	
	XTAL pin (PTB6) temperature ≥ 125° C			1.1	µA	
R_{PU}	Internal pullup resistors	20		50	kΩ	7
R_{PD}	Internal pulldown resistors	20		50	kΩ	8

1. For reset pads, same V_{ih} levels are applicable
2. For reset pads, same V_{il} levels are applicable
3. The strong pad I/O pin is capable of switching a 50 pF load up to 40 MHz.
4. For refernce only. Run simulations with the IBIS model and custom board for accurate results.

5. Typical leakage is given at room temperature. Maximum is given for 125°C. Leakage numbers increase with temperature, approximately every 12 – 14°C the value doubles. Leakage is tested at hot temperature. We ensure maximums are not exceeded. Please note that when the ADC module samples a pin, additional currents beyond the leakage number are drawn to charge the sample and hold capacitances and internal analog busses. These are difficult to predict.
6. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details see IO Signal Description Input Multiplexing sheet(s) attached with the *Reference Manual*.
7. Measured at input V = V_{SS}
8. Measured at input V = V_{DD}

Table 51. DC electrical specifications at 5.0 V Range for S32M244 series

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage	0.65 x V_{DD}	—	V_{DD} + 0.3	V	1
V_{il}	Input Buffer Low Voltage	V_{SS} − 0.3	—	0.35 x V_{DD}	V	2
V_{hys}	Input Buffer Hysteresis	0.06 x V_{DD}	—	—	V	
Ioh_{GPIO} $Ioh_{GPIO\text{-}HD\_DSE\_0}$	I/O current source capability measured when pad V_{oh}= (V_{DD} - 0.8 V)	5	—	—	mA	
Iol_{GPIO} $Iol_{GPIO\text{-}HD\_DSE\_0}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	5	—	—	mA	
$Ioh_{GPIO\text{-}HD\_DSE\_1}$	I/O current source capability measured when pad V_{oh} = V_{DD} - 0.8 V	20	—	—	mA	3
$Iol_{GPIO\text{-}HD\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	20	—	—	mA	3
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 5.5 V					4
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins		0.010	0.5	µA	
R_{PU}	Internal pullup resistors	20		50	kΩ	5
R_{PD}	Internal pulldown resistors	20		50	kΩ	6

1. For reset pads, same V_{ih} levels are applicable
2. For reset pads, same V_{il} levels are applicable
3. The strong pad I/O pin is capable of switching a 50 pF load up to 40 MHz.
4. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details see IO Signal Description Input Multiplexing sheet(s) attached with the *Reference Manual*
5. Measured at input V = V_{SS}
6. Measured at input V = V_{DD}

10.2.5 AC electrical specifications at 3.3 V range

Table 52. AC electrical specifications at 3.3 V Range for S32M242 series

Symbol	DSE	Rise time (nS) [1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max.	Min.	Max.	
tRF_{GPIO}	NA	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
$tRF_{GPIO-HD}$	0	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
	1	1.5	5.8	1.7	6.1	25
		2.4	8.0	2.6	8.3	50
		6.3	22.0	6.0	23.8	200
$tRF_{GPIO-FAST}$	0	0.6	2.8	0.5	2.8	25
		3.0	7.1	2.6	7.5	50
		12.0	27.0	10.3	26.8	200
	1	0.4	1.3	0.38	1.3	25
		1.5	3.8	1.4	3.9	50
		7.4	14.9	7.0	15.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

Table 53. AC electrical specifications at 3.3 V Range for S32M244 series

Symbol	DSE	Rise time (nS) [1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max.	Min.	Max.	
tRF_{GPIO}	NA	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
$tRF_{GPIO-HD}$	0	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
	1	1.5	5.8	1.7	6.1	25
		2.4	8.0	2.6	8.3	50
		6.3	22.0	6.0	23.8	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different. For protocol specific AC specifications, see respective sections.

10.2.6 AC electrical specifications at 5 V range

Table 54. AC electrical specifications at 5 V Range for S32M242 series

Symbol	DSE	Rise time (nS) [1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max .	Min.	Max.	
tRF_{GPIO}	NA	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50
		17.3	54.8	17.6	59.7	200
$tRF_{GPIO-HD}$	0	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50
		17.3	54.8	17.6	59.7	200
	1	1.1	4.6	1.1	5.0	25
		2.0	5.7	2.0	5.8	50
		5.4	16.0	5.0	16.0	200
$tRF_{GPIO-FAST}$	0	0.42	2.2	0.37	2.2	25
		2.0	5.0	1.9	5.2	50
		9.3	18.8	8.5	19.3	200
	1	0.37	0.9	0.35	0.9	25
		1.2	2.7	1.2	2.9	50
		6.0	11.8	6.0	12.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

Table 55. AC electrical specifications at 5 V Range for S32M244 series

Symbol	DSE	Rise time (nS) [1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max .	Min.	Max.	
tRF_{GPIO}	NA	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50
		17.3	54.8	17.6	59.7	200
$tRF_{GPIO-HD}$	0	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50
		17.3	54.8	17.6	59.7	200
	1	1.1	4.6	1.1	5.0	25
		2.0	5.7	2.0	5.8	50
		5.4	16.0	5.0	16.0	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different. For protocol specific AC specifications, see respective sections.

10.2.7 Standard input pin capacitance

Table 56. Standard input pin capacitance

Symbol	Description	Min.	Max.	Unit
C_{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to External System Oscillator electrical specifications for EXTAL/XTAL pins.

10.2.8 Device clock specifications

Table 57. Device clock specifications [1]

Symbol	Description	Min.	Max.	Unit
Normal run mode (S32M242 series) [2]				
f_{SYS}	System and core clock	—	80	MHz
f_{BUS}	Bus clock	—	40[3]	MHz
f_{FLASH}	Flash clock	—	26.67	MHz
Normal run mode (S32M244 series) [2]				
f_{SYS}	System and core clock	—	80	MHz
f_{BUS}	Bus clock	—	40[3]	MHz
f_{FLASH}	Flash clock	—	20	MHz
VLPR mode (S32M242 series)[4]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	4	MHz
f_{FLASH}	Flash clock	—	1	MHz
VLPR mode (S32M244 series)[4]				
f_{SYS}	System and core clock	—	1	MHz
f_{BUS}	Bus clock	—	1	MHz
f_{FLASH}	Flash clock	—	0.25	MHz

1. Refer to the section Feature comparison for the availability of modes and other specifications.
2. With SPLL as system clock source.
3. 48 MHz when f_{SYS} is 48 MHz
4. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

10.3 Peripheral operating requirements and behaviors

10.3.1 System modules

There are no electrical specifications necessary for the device's system modules.

10.3.2 Clock interface modules

10.3.2.1 External System Oscillator electrical specifications

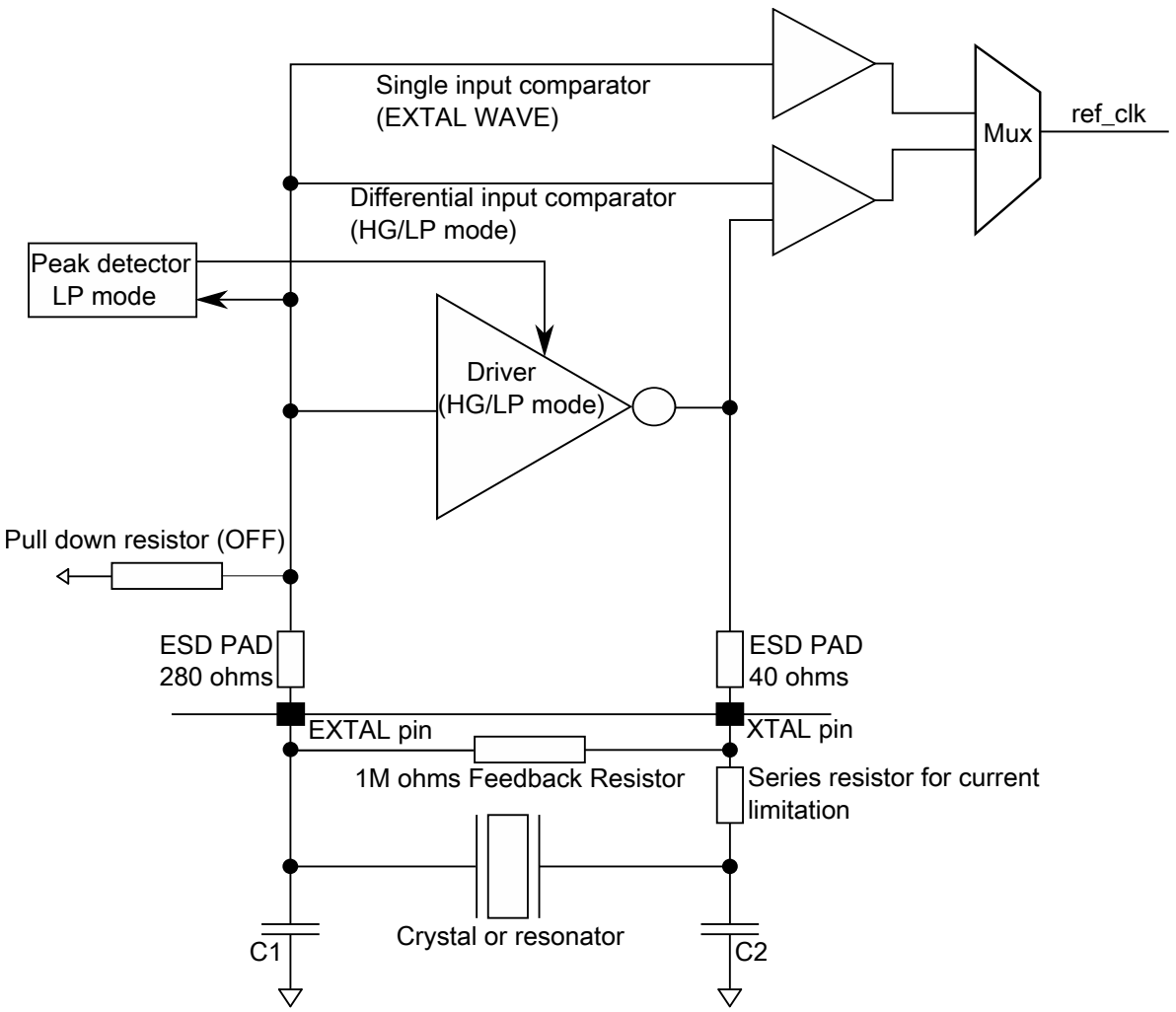


Figure 24. Oscillator connections scheme

Table 58. External System Oscillator electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
g_{mXOSC}	Crystal oscillator transconductance					
	SCG_SOSCCFG[RANGE]=2'b10 for 4-8 MHz	2.2	—	13.7	mA/V	
	SCG_SOSCCFG[RANGE]=2'b11 for 8-40 MHz	16	—	47	mA/V	
V_{IL}	Input low voltage — EXTAL pin in external clock mode	V_{SS}	—	1.15	V	
V_{IH}	Input high voltage — EXTAL pin in external clock mode	0.7 * V_{DD}	—	V_{DD}	V	
C_1	EXTAL load capacitance	—	—	—		1

Table continues on the next page...

Table 58. External System Oscillator electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
C_2	XTAL load capacitance	—	—	—		1
R_F	Feedback resistor					2
	Low-gain mode (HGO=0)	—	—	—	MΩ	
	High-gain mode (HGO=1)	—	1	—	MΩ	
R_S 3	Series resistor					
	Low-gain mode (HGO=0)	—	0	—	kΩ	
	High-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp_XTAL}	Peak-to-peak amplitude of oscillation (oscillator mode) at XTAL					4
	Low-gain mode (HGO=0)	—	1.0	—	V	
	High-gain mode (HGO=1)	—	3.3	—	V	
V_{pp_EXTAL}	Peak-to-peak amplitude of oscillation (oscillator mode) at EXTAL					4 5
	Low-gain mode (HGO=0)	0.8	—	—	V	
	High-gain mode (HGO=1), V_{DD}= 4.0 V to 5.5 V	1.7	—	—	V	
V_{SOSCOP}	Oscillation operating point					4
	High-gain mode (HGO=1)	1.15	—	—	V	

1. Crystal oscillator circuit provides stable oscillations when g_{mXOSC} > 5 * gm_crit. The gm_crit is defined as:

   $gm\_crit = 4 * (ESR + R_S) * (2\pi F)^2 * (C_0 + C_L)^2$

   where:

   - g_{mXOSC} is the transconductance of the internal oscillator circuit
   - ESR is the equivalent series resistance of the external crystal
   - R_S is the series resistance connected between XTAL pin and external crystal for current limitation
   - F is the external crystal oscillation frequency
   - C_0 is the shunt capacitance of the external crystal
   - C_L is the external crystal total load capacitance. $C_L = C_s + [C_1 * C_2/(C_1+C_2)]$
   - C_s is stray or parasitic capacitance on the pin due to any PCB traces
   - C_1, C_2 external load capacitances on EXTAL and XTAL pins

   See manufacture datasheet for external crystal component values
2. - When low-gain is selected, internal R_F will be selected and external R_F should not be attached.
   - When high-gain is selected, external R_F (1 M Ohm) needs to be connected for proper operation of the crystal. For external resistor, up to 5% tolerance is allowed.
3. R_S should be selected carefully to have appropriate oscillation amplitude for both protecting crystal or resonator device and satisfying proper oscillation startup condition.
4. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.
5. Minimum value is shown as a reference only, however the HW design needs to ensure it reaches the maximum value by following the guidelines given in above notes (notes 1, 2, and 3) and performs the required robustness testing at the application level. During testing, a low capacitance probe (< 5 pF) must be used to avoid any decrease in the V_{pp_EXTAL} value.

10.3.2.2 External System Oscillator frequency specifications

Table 59. External System Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_hi}	Oscillator crystal or resonator frequency	4	—	40 [1] [2]	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	[3], [2], [4]
t_{dc_extal}	Input clock duty cycle (external clock mode)	48	50	52	%	[3], [2], [4]
t_{cst}	Crystal Start-up Time					
	8 MHz low-gain mode (HGO=0)	—	1.5	—	ms	[5]
	8 MHz high-gain mode (HGO=1)	—	2.5	—		
	40 MHz low-gain mode (HGO=0)	—	2	—		
	40 MHz high-gain mode (HGO=1)	—	2	—		

1. For an ideal clock of 40 MHz, if permitted by application requirements, an error of +/- 5% is supported with 50% duty cycle.
2. (S32M244) At 40 MHz to 36 MHz when sourcing for ADC clock please use divider ADCn.ADC_CFG1[ADICLK] to ½ or lower for the specific ADC instance. This will help achieve duty cycle requirement. For 36 MHz and 32 MHz 45-55% or better duty cycle to be maintained. For frequencies lower than 32 MHz, please maintain duty cycle of 40-50% or better.
3. Frequencies below 40 MHz can be used for degraded duty cycle upto 40-60%. When using for ADC clock further restrictions apply. At 50 MHz to 45 MHz when sourcing for ADC clock please use divider ADCn.ADC_CFG1[ADICLK] to ½ or lower for the specific ADC instance. This will help achieve duty cycle requirement. for 45 MHz and 41 MHz 45-55% or higher duty cycle should be maintained.
4. (S32M244) The limits to source ADC clock are 40 MHz, so in cases the input clock is higher than 40 MHz, it cannot be used as a source of ADC clock.
5. Proper PC board layout procedures must be followed to achieve specifications.

10.3.2.3 System Clock Generation (SCG) specifications

10.3.2.3.1 Fast internal RC Oscillator (FIRC) electrical specifications

Table 60. Fast internal RC Oscillator electrical specifications for S32M242 series

Symbol	Parameter[1]	Value			Unit
		Min.	Typ.	Max.	
F_{FIRC}	FIRC target frequency	—	48	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	±0.5	±1	$\%F_{FIRC}$
ΔF125	Frequency deviation across process, voltage, and temperature < 125°C	—	±0.5	±1.1	$\%F_{FIRC}$
$T_{Startup}$	Startup time		3.4	5	µs[2]
T_{JIT}[3]	Cycle-to-Cycle jitter	—	300	500	ps
T_{JIT}[3]	Long term jitter over 1000 cycles	—	0.04	0.1	$\%F_{FIRC}$

1. With FIRC regulator enable
2. Startup time is defined as the time between clock enablement and clock availability for system use.
3. FIRC as system clock

Table 61. Fast internal RC Oscillator electrical specifications for S32M244 series

Symbol	Parameter[1]	Value			Unit
		Min.	Typ.	Max.	
F_{FIRC}	FIRC target frequency	—	48	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature	—	±0.5	±1.4	$\%F_{FIRC}$
$T_{Startup}$	Startup time		3.4	5	µs[2]
T_{JIT}[3]	Cycle-to-Cycle jitter	—	300	500	ps
T_{JIT}[3]	Long term jitter over 1000 cycles	—	0.04	0.1	$\%F_{FIRC}$

1. With FIRC regulator enable
2. Startup time is defined as the time between clock enablement and clock availability for system use.
3. FIRC as system clock

NOTE

Fast internal RC oscillator is compliant with LIN when device is used as a slave node.

10.3.2.3.2 Slow internal RC oscillator (SIRC) electrical specifications

Table 62. Slow internal RC oscillator (SIRC) electrical specifications for S32M242 series

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{SIRC}	SIRC target frequency	—	8	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	—	±3	$\%F_{SIRC}$
ΔF125	Frequency deviation across process, voltage, and temperature < 125°C	—	—	±3.3	$\%F_{SIRC}$
$T_{Startup}$	Startup time	—	9	12.5	µs[1]

1. Startup time is defined as the time between clock enablement and clock availability for system use.

Table 63. Slow internal RC oscillator (SIRC) electrical specifications for S32M244 series

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{SIRC}	SIRC target frequency	—	8	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature	—	—	±3.3	$\%F_{SIRC}$
$T_{Startup}$	Startup time	—	9	12.5	µs[1]

1. Startup time is defined as the time between clock enablement and clock availability for system use.

10.3.2.4 Low Power Oscillator (LPO) electrical specifications

Table 64. Low Power Oscillator (LPO) electrical specifications

Symbol	Parameter	Value				Unit
		Min.	Typ.	Max.		
		S32M242/ S32M244	S32M242/ S32M244	S32M242	S32M244	
F_{LPO}	Internal low power oscillator frequency	113	128	139	141	kHz
$T_{startup}$	Startup Time	—	—	20		µs

10.3.2.5 SPLL electrical specifications

Table 65. SPLL electrical specifications

Symbol	Parameter	Min.	Typ.	Max.		Unit
		S32M242/ S32M244	S32M242/ S32M244	S32M242	S32M244	
F_{SPLL_REF} [1]	PLL Reference Frequency Range	8	—	16		MHz
F_{SPLL_Input} [2]	PLL Input Frequency	8	—	40	48	MHz
F_{VCO_CLK}	VCO output frequency	180	—	320		MHz
F_{SPLL_CLK}	PLL output frequency	90	—	160		MHz
J_{CYC_SPLL}	PLL Period Jitter (RMS)[3]					
	at F_{VCO_CLK} 180 MHz	—	120	—		ps
	at F_{VCO_CLK} 320 MHz	—	75	—		ps
J_{ACC_SPLL}	PLL accumulated jitter over 1µs (RMS)[3]					
	at F_{VCO_CLK} 180 MHz	—	—	1350[4]		ps
	at F_{VCO_CLK} 320 MHz	—	—	600[4]		ps
D_{UNL}	Lock exit frequency tolerance	± 4.47	—	± 5.97		%
T_{SPLL_LOCK}	Lock detector detection time[5]	—	—	$150 \times 10^{-6} + 1075(1/F_{SPLL\_REF})$		s

1. F_{SPLL_REF} is PLL reference frequency range after the PREDIV. For PREDIV and MULT settings refer SCG_SPLLCFG register of Reference Manual.
2. F_{SPLL_Input} is PLL input frequency range before the PREDIV must be limited to the range 8 MHz to 40 MHz. This input source could be derived from a crystal oscillator or some other external square wave clock source using OSC bypass mode. For external clock source settings refer SCG_SOSCCFG register of Reference Manual.
3. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary
4. The behavior of the accumulated PLL jitter saturates over 1us.
5. Lock detector detection time is defined as the time between PLL enablement and clock availability for system use.

10.3.3 Memory and memory interfaces

10.3.3.1 Flash memory module (FTFC/FTFM) electrical specifications

This section describes the electrical characteristics of the flash memory module.

10.3.3.1.1 Flash timing specifications — commands

Table 66. Flash command timing specifications for S32M242 series

Symbol	Description[1]		Typ	Max	Unit	Notes
t_{rd1blk}	Read 1 Block execution time	32 KB flash	—	—	ms	
		64 KB flash	—	0.5		
		128 KB flash	—	—		
		256 KB flash	—	2		
		512 KB flash	—	—		
t_{rd1sec}	Read 1 Section execution time	2 KB flash	—	75	µs	
		4 KB flash	—	100		
t_{pgmchk}	Program Check execution time	—	—	95	µs	
t_{pgm8}	Program Phrase execution time	—	90	225	µs	
t_{ersblk}	Erase Flash Block execution time	32 KB flash	—	—	ms	2
		64 KB flash	30	550		
		128 KB flash	—	—		
		256 KB flash	250	2125		
		512 KB flash	—	—		
t_{ersscr}	Erase Flash Sector execution time	—	12	130	ms	2
$t_{pgmsec1k}$	Program Section execution time (1KB flash)	—	5	—	ms	
t_{rd1all}	Read 1s All Block execution time	—	—	2.8	ms	
t_{rdonce}	Read Once execution time	—	—	30	µs	
$t_{pgmonce}$	Program Once execution time	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	250	2800	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	35	µs	
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	250	2800	ms	2
$t_{pgmpart}$	Program Partition for EEPROM execution time	32 KB EEPROM backup	70	—	ms	3
		64 KB EEPROM backup	71	—		

Table continues on the next page...

Table 66. Flash command timing specifications for S32M242 series (continued)

Symbol	Description[1]		Typ	Max	Unit	Notes
t_{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	ms	3
		32 KB EEPROM backup	0.8	1.2		
		48 KB EEPROM backup	1	1.5		
		64 KB EEPROM backup	1.3	1.9		
t_{eewr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	µs	3,4
		48 KB EEPROM backup	430	1850		
		64 KB EEPROM backup	475	2000		
$t_{eewr16b}$	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	µs	3,4
		48 KB EEPROM backup	430	1850		
		64 KB EEPROM backup	475	2000		
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	2000	µs	
$t_{eewr32b}$	32-bit write to FlexRAM execution time	32 KB EEPROM backup	630	2000	µs	3,4
		48 KB EEPROM backup	720	2125		
		64 KB EEPROM backup	810	2250		
$t_{quickwr}$	32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF setting (32-bit write complete, ready for next 32-bit write)	1st 32-bit write	200	550	µs	4,5,6
		2nd through Next to Last (Nth-1) 32-bit write	150	550		
		Last (Nth) 32-bit write (time for write only, not cleanup)	200	550		
$t_{quickwrClnup}$	Quick Write Cleanup execution time	—	—	(# of Quick Writes) * 2.0	ms	7

1. All command times assumes 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3. For all EEPROM Emulation terms, the specified timing shown assumes previous record cleanup has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
4. 1st time EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2× the times shown.
5. Only after the Nth write completes will any data be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power on reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
6. Quick Write times may take up to 550 µs, as additional cleanup may occur when crossing sector boundaries.
7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

Table 67. Flash command timing specifications for S32M244 series

Symbol	Description[1]		Typ	Max	Unit	Notes
t_{rd1blk}	Read 1 Block execution time	64 KB flash	—	0.75	ms	
		256 KB flash	—	—		
		512 KB flash	—	2.5		
t_{rd1sec}	Read 1 Section execution time	2 KB flash	—	200	µs	
		4 KB flash	—	220		
t_{pgmchk}	Program Check execution time	—	—	175	µs	
t_{pgm8}	Program Phrase execution time	—	150	300	µs	
t_{ersblk}	Erase Flash Block execution time	64 KB flash	100	1000	ms	2
		256 KB flash	—	—		
		512 KB flash	700	8000		
t_{ersscr}	Erase Flash Sector execution time	—	20	250	ms	2
t_{pgmsec}	Program Section execution time	1 KB flash	7	—	ms	
t_{rd1all}	Read 1s All Block execution time	—	—	3.5	ms	
t_{rdonce}	Read Once execution time	—	—	35	µs	
$t_{pgmonce}$	Program Once execution time	—	150	—	µs	
t_{ersall}	Erase All Blocks execution time	—	825	9300	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	40	µs	
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	825	9300	ms	2

Table continues on the next page...

Table 67. Flash command timing specifications for S32M244 series (continued)

Symbol	Description[1]		Typ	Max	Unit	Notes
$t_{pgmpart}$	Program Partition for EEPROM execution time	32 KB EEPROM backup	98	—	ms	3
		64 KB EEPROM backup	100	—		
t_{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.125	—	ms	3
		32 KB EEPROM backup	1.0	1.5		
		48 KB EEPROM backup	1.2	1.8		
		64 KB EEPROM backup	1.4	2.1		
$t_{eewr32b}$	32-bit write to FlexRAM execution time	32 KB EEPROM backup	1250	4000	µs	3,4
		48 KB EEPROM backup	1500	4125		
		64 KB EEPROM backup	1700	4250		
$t_{quickwr}$	32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF setting (32-bit write complete, ready for next 32-bit write)	1st 32-bit write	300	1400	µs	4,5,6
		2nd through Next to Last (Nth-1) 32-bit write	275	1000		
		Last (Nth) 32-bit write (time for write only, not cleanup)	375	1200		
$t_{quickwrClnup}$	Quick Write Cleanup execution time	—	—	(# of Quick Writes) * 3.6	ms	7

1. All command times assume 20 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For all EEPROM Emulation terms, the specified timing shown assumes previous record cleanup has occurred ($t_{quickwrClnup}$). This may be verified by executing CCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
4. 1st time FlexRAM writes after a Reset or SETRAM may incur additional overhead for emulated EEPROM cleanup, resulting in up to 2× the times shown.
5. Only after the Nth write completes will any data be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power on reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
6. Quick Write times may take up to 1200 µs, as additional cleanup may occur when crossing sector boundaries.
7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution if command is requested at a later point.

10.3.3.1.2 Reliability specifications

Table 68. NVM reliability specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
When using as Program and Data Flash						
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	—	—	years	1
$n_{nvmcycp}$	Cycling endurance	1 K	—	—	cycles	2 3
When using FlexMemory feature : FlexRAM as Emulated EEPROM						
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	—	—	years	1 4
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	—	—	years	1
$n_{nvmwree16}$ $n_{nvmwree256}$	Write endurance • EEPROM backup to FlexRAM ratio = 16 • EEPROM backup to FlexRAM ratio = 256	100 K 1.6 M	— —	— —	writes writes	5 6 7

1. Data retention period per block begins upon initial user factory programming or after each subsequent erase.
2. Program and Erase for PFlash and DFlash are supported across product temperature specification.
3. Cycling endurance is per DFlash or PFlash Sector.
4. Background maintenance operations during normal FlexRAM usage extend effective data retention life beyond 5 years.
5. FlexMemory write endurance specified for 32-bit writes to FlexRAM and is supported across product temperature specification. Greater write endurance may be achieved with larger ratios of EEPROM backup to FlexRAM.
6. For usage of any emulated EEPROM driver other than the FlexMemory feature, the endurance spec will fall back to the specified endurance value of the DFlash specification (1K).
7. FlexMemory calculator tool is available at NXP web site for help in estimation of the maximum write endurance achievable at specific EEPROM/FlexRAM ratios. The "In Spec" portions of the online calculator refer to the NVM reliability specifications section of data sheet. This calculator only applies to the FlexMemory feature.

10.3.4 Analog modules

10.3.4.1 ADC electrical specifications

10.3.4.1.1 12-bit ADC operating conditions

NOTE

All the data mention in this table is only validated in a simulation and granted by NXP design team.

Table 69. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.		Unit	Notes
			S32M242/ S32M244	S32M242/ S32M244	S32M242	S32M244		
V_{REFH}	ADC reference voltage high		See voltage and current operating requirements for values	V_{DDA}	See voltage and current operating requirements for values		V	[2]
V_{REFL}	ADC reference voltage low		See voltage and current operating requirements for values	0	See voltage and current operating requirements for values		mV	[2]
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}		V	
R_S	Source impedendance	f_{ADCK} < 4 MHz	—	—	5		kΩ	
R_{SW1}	Channel Selection Switch Impedance		—	0.650	0.780		kΩ	
R_{AD}	Sampling Switch Impedance		—	0.155	1.0		kΩ	
C_{P1}	Pin Capacitance		—	2.1	2.5		pF	
C_{P2}	Analog Bus Capacitance		—	3	4		pF	
C_S	Sampling capacitance		—	5.1 (gain =0)... 7.2 (gain= max)	6.36 (gain =0)... 9.36 (gain= max)		pF	
f_{ADCK}	ADC conversion clock frequency	Normal usage	2	40	50	40	MHz	[3], [4]
f_{CONV}	ADC conversion frequency	No ADC hardware averaging.[5] Continuous conversions enabled, subsequent conversion time	46.4	928	1160		Ksps	[6] [7]
		ADC hardware averaging set to 32. [5] Continuous	1.45	29	36.25		Ksps	[6,7]

Table continues on the next page...

Table 69. 12-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.		Unit	Notes
			S32M242/ S32M244	S32M242/ S32M244	S32M242	S32M244		
		conversions enabled, subsequent conversion time						
	ADC power consumption	—	—	1.0	1.1		pF	[8]

1. Typical values assume V_{DDA} = 5 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. For packages without dedicated V_{REFH} and V_{REFL} pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SS}. To get maximum performance, reference supply quality should be better than SAR ADC. See application note AN5032 for details.
3. Clock and compare cycle need to be set according to the guidelines mentioned in the *Reference Manual* .
4. ADC conversion will become less reliable above maximum frequency.
5. When using ADC hardware averaging, see the *Reference Manual* to determine the most appropriate setting for AVGS.
6. Numbers based on the minimum sampling time of 275 ns.
7. For guidelines and examples of conversion rate calculation, see the *Reference Manual* section 'Calibration function'
8. Configuration used during the test to obtain this value is:
   - VDD=VDDA=VREFH=2.5 V, 2.7 V, 3 V ,5.5 V, (externally forced)
   - BUS CLK=48 MHz, ADC CLK=48MHz (FIRC Used), Calibration CLK=24MHz, Sample Time =14 Cyc, Averaging=32
   - Resolution= 12 bit
   - Conversion Mode: Continuous Conversion
   - Channel: ADC0_SE1
   - Temperatures: -40C, 25C, 135C

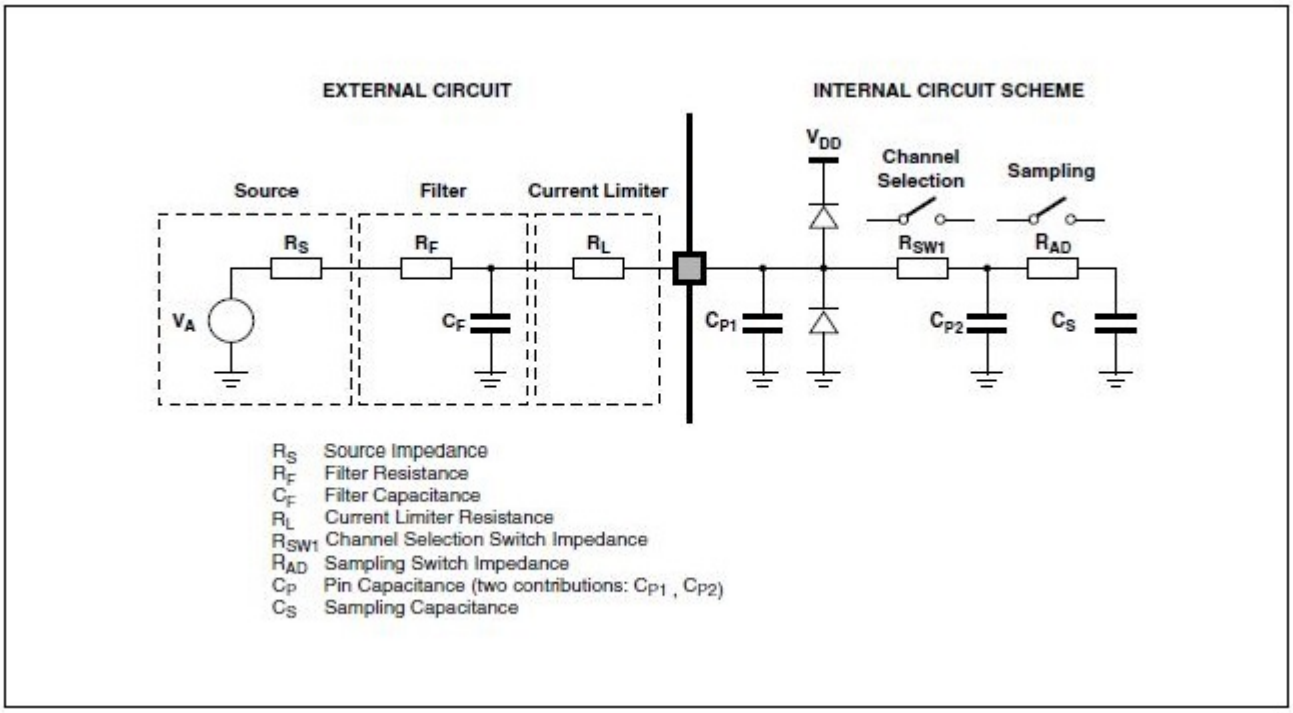


Figure 25. ADC input impedance equivalency diagram

10.3.4.1.2 12-bit ADC electrical characteristics

NOTE

- ADC performance specifications are documented using a single ADC. For parallel/simultaneous operation of both ADCs, either for sampling the same channel by both ADCs or for sampling different channels by each ADC, some amount of decrease in performance can be expected. Care must be taken to stagger the two ADC conversions, in particular the sample phase, to minimize the impact of simultaneous conversions.
- On reduced pin packages where ADC reference pins are shared with supply pins, ADC analog performance characteristics may be impacted. The amount of variation will be directly impacted by the external PCB layout and hence care must be taken with PCB routing. See AN5426 for details
- All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}=V_{DD}, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.

Table 70. 12-bit ADC characteristics (2.7 V to 3 V) (V_{REFH} = V_{DDA}, V_{REFL} = V_{SS}) [1]

Symbol	Description	Min.	Typ.[2]	Max.	Unit	Notes
V_{DDA}	Supply voltage	2.7	—	3	V	
I_{DDA_ADC}	Supply current per ADC	—	0.6	—	mA	[3]
SMPLTS	Sample Time	275	—	Refer to the *Reference Manual*	ns	
TUE[4]	Total unadjusted error	—	±4	±8	LSB[5]	[6], [7], [8], [9]
DNL	Differential non-linearity	—	±1.0	—	LSB[5]	[6], [7], [8], [9]
INL	Integral non-linearity	—	±2.0	—	LSB[5]	[6], [7], [8], [9]

1. This table is not applicable to S32M244.
2. Typical values assume V_{DDA} = 3 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

Table 71. 12-bit ADC characteristics (3 V to 5.5 V)(V_{REFH} = V_{DDA}, V_{REFL} = V_{SS})

Symbol	Description	Min.		Typ.[1]	Max.	Unit	Notes
		S32M242	S32M244	S32M242/ S32M244	S32M242/ S32M244		
V_{DDA}	Supply voltage	3	3.13	—	5.5	V	
I_{DDA_ADC}	Supply current per ADC	—		1	—	mA	[2]
SMPLTS	Sample Time	275		—	Refer to the *Reference Manual*	ns	
TUE[3]	Total unadjusted error	—		±4	±8	LSB[4]	[5], [6], [7], [8]
DNL	Differential non-linearity	—		±0.7	—	LSB[4]	[5], [6], [7], [8]
INL	Integral non-linearity	—		±1.0	—	LSB[4]	[5], [6], [7], [8]

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF unless otherwise stated.
2. The ADC supply current depends on the ADC conversion rate.
3. Represents total static error, which includes offset and full scale error.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
6. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
7. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
8. All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

- Due to triple bonding in lower pin packages like 64-LQFP degradation might be seen in ADC parameters.

Table 72. Pin mapping

Pin name	TGATE purpose
PTE8	CMP0_IN3
PTC3	ADC0_SE11/CMP0_IN4
PTC2	ADC0_SE10/CMP0_IN5

Table continues on the next page...

Table 72. Pin mapping (continued)

Pin name	TGATE purpose
PTD7	CMP0_IN6
PTD6	CMP0_IN7
PTD28	ADC1_SE22
PTD27	ADC1_SE21

10.3.4.2 CMP with 8-bit DAC electrical specifications

Table 73. Comparator with 8-bit DAC electrical specifications for S32M242 series

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode[1]				µA
	-40 - 125 °C	—	230	300	
I_{DDLS}	Supply current, Low-speed mode[1]				µA
	-40 - 105 °C	—	6	11	
	-40 - 125 °C		6	13	
V_{AIN}	Analog input voltage	0	0 - V_{DDA}	V_{DDA}	V
V_{AIO}	Analog input offset voltage, High-speed mode				mV
	-40 - 125 °C	-25	±1	25	
V_{AIO}	Analog input offset voltage, Low-speed mode				mV
	-40 - 125 °C	-40	±4	40	
t_{DHSB}	Propagation delay, High-speed mode[2]				ns
	-40 - 105 °C	—	35	200	
	-40 - 125 °C		35	300	
t_{DLSB}	Propagation delay, Low-speed mode[2]				µs
	-40 - 105 °C	—	0.5	2	
	-40 - 125 °C	—	0.5	3	
t_{DHSS}	Propagation delay, High-speed mode[3]				ns
	-40 - 105 °C	—	70	400	
	-40 - 125 °C	—	70	500	
t_{DLSS}	Propagation delay, Low-speed mode[3]				µs
	-40 - 105 °C	—	1	5	
	-40 - 125 °C	—	1	5	
t_{IDHS}	Initialization delay, High-speed mode[4]				µs

Table continues on the next page...

Table 73. Comparator with 8-bit DAC electrical specifications for S32M242 series (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	-40 - 125 ℃	—	1.5	3	
t_{IDLS}	Initialization delay, Low-speed mode[4]				µs
	-40 - 125 ℃	—	10	30	
V_{HYST0}	Analog comparator hysteresis, Hyst0				mV
	-40 - 125 ℃	—	0	—	
V_{HYST1}	Analog comparator hysteresis, Hyst1, High-speed mode				mV
	-40 - 125 ℃	—	19	66	
	Analog comparator hysteresis, Hyst1, Low-speed mode				
	-40 - 125 ℃	—	15	40	
V_{HYST2}	Analog comparator hysteresis, Hyst2, High-speed mode				mV
	-40 - 125 ℃	—	34	133	
	Analog comparator hysteresis, Hyst2, Low-speed mode				
	-40 - 125 ℃	—	23	80	
V_{HYST3}	Analog comparator hysteresis, Hyst3, High-speed mode				mV
	-40 - 125 ℃	—	46	200	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	-40 - 125 ℃	—	32	120	
I_{DAC8b}	8-bit DAC current adder (enabled)				
	3.3V Reference Voltage	—	6	9	µA
	5V Reference Voltage	—	10	16	µA
INL[5]	8-bit DAC integral non-linearity	–0.75	—	0.75	LSB[6]
DNL	8-bit DAC differential non-linearity	–0.5	—	0.5	LSB[6]
t_{DDAC}	Initialization and switching settling time	—	—	30	µs

1. Difference at input > 200mV
2. Applied ± (100 mV + $V_{HYST0/1/2/3}$+ max. of V_{AIO}) around switch point.
3. Applied ± (30 mV + 2 × $V_{HYST0/1/2/3}$+ max. of V_{AIO}) around switch point.
4. Applied ± (100 mV + $V_{HYST0/1/2/3}$).
5. Calculation method used: Linear Regression Least Square Method
6. 1 LSB = $V_{reference}$/256

Table 74. Comparator with 8-bit DAC electrical specifications for S32M244 series

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode[1]				µA
	-40 - 125 °C	—	230	300	
	-40 - 150 °C		230	300	
I_{DDLS}	Supply current, Low-speed mode[1]				µA
	-40 - 105 °C	—	6	11	
	-40 - 125 °C		6	13	
	-40 - 150 °C		6	13	
V_{AIN}	Analog input voltage	0	0 - V_{DDA}	V_{DDA}	V
V_{AIO}	Analog input offset voltage, High-speed mode				mV
	-40 - 125 °C	-25	±1	25	
	-40 - 150 °C	-50	±1	50	
V_{AIO}	Analog input offset voltage, Low-speed mode				mV
	-40 - 125 °C	-40	±4	40	
	-40 - 150 °C	-50	±4	50	
t_{DHSB}	Propagation delay, High-speed mode[2]				ns
	-40 - 105 °C	—	35	200	
	-40 - 125 °C		35	300	
	-40 - 150 °C		35	400	
t_{DLSB}	Propagation delay, Low-speed mode[2]				µs
	-40 - 105 °C	—	0.5	2	
	-40 - 125 °C	—	0.5	3	
	-40 - 150 °C	—	0.5	3	
t_{DHSS}	Propagation delay, High-speed mode[3]				ns
	-40 - 105 °C	—	70	400	
	-40 - 125 °C	—	70	500	
	-40 - 150 °C	—	70	600	
t_{DLSS}	Propagation delay, Low-speed mode[3]				µs
	-40 - 105 °C	—	1	5	
	-40 - 125 °C	—	1	5	
	-40 - 150 °C	—	1	5	
t_{IDHS}	Initialization delay, High-speed mode[4]				µs

Table continues on the next page...

Table 74. Comparator with 8-bit DAC electrical specifications for S32M244 series (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	-40 - 125 °C	—	1.5	3	
	-40 - 150 °C	—	1.5	3	
t_{IDLS}	Initialization delay, Low-speed mode[4]				µs
	-40 - 125 °C	—	10	30	
	-40 - 150 °C	—	10	30	
V_{HYST0}	Analog comparator hysteresis, Hyst0				mV
	-40 - 125 °C	—	0	—	
	-40 - 150 °C	—	0	—	
V_{HYST1}	Analog comparator hysteresis, Hyst1, High-speed mode				mV
	-40 - 125 °C	—	19	66	
	-40 - 150 °C	—	19	90	
	Analog comparator hysteresis, Hyst1, Low-speed mode				
	-40 - 125 °C	—	15	40	
	-40 - 150 °C	—	15	40	
V_{HYST2}	Analog comparator hysteresis, Hyst2, High-speed mode				mV
	-40 - 125 °C	—	34	133	
	-40 - 150 °C	—	34	186	
	Analog comparator hysteresis, Hyst2, Low-speed mode				
	-40 - 125 °C	—	23	80	
	-40 - 150 °C	—	23	80	
V_{HYST3}	Analog comparator hysteresis, Hyst3, High-speed mode				mV
	-40 - 125 °C	—	46	200	
	-40 - 150 °C	—	46	280	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	-40 - 125 °C	—	32	120	
	-40 - 150 °C	—	32	120	
I_{DAC8b}	8-bit DAC current adder (enabled)				
	3.3V Reference Voltage	—	6	9	µA

Table continues on the next page...

Table 74. Comparator with 8-bit DAC electrical specifications for S32M244 series (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	5V Reference Voltage	—	10	16	µA
INL[5]	8-bit DAC integral non-linearity				LSB[6]
	-40 - 125 °C	–0.75	—	0.75	
	-40 - 150 °C	-2	—	2	
DNL	8-bit DAC differential non-linearity	–0.5	—	0.5	LSB[6]
t_{DDAC}	Initialization and switching settling time	—	—	30	µs

1. Difference at input > 200mV
2. Applied ± (100 mV + $V_{HYST0/1/2/3}$+ max. of V_{AIO}) around switch point.
3. Applied ± (30 mV + 2 × $V_{HYST0/1/2/3}$+ max. of V_{AIO}) around switch point.
4. Applied ± (100 mV + $V_{HYST0/1/2/3}$).
5. Calculation method used: Linear Regression Least Square Method
6. 1 LSB = $V_{reference}$/256

NOTE

For comparator IN signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or switching pins cross coupling may happen and hence hysteresis settings can be used to obtain the desired comparator performance. Additionally, an external capacitor (1nF) should be used to filter noise on input signal. Also, source drive should not be weak (Signal with < 50 K pull up/down is recommended).

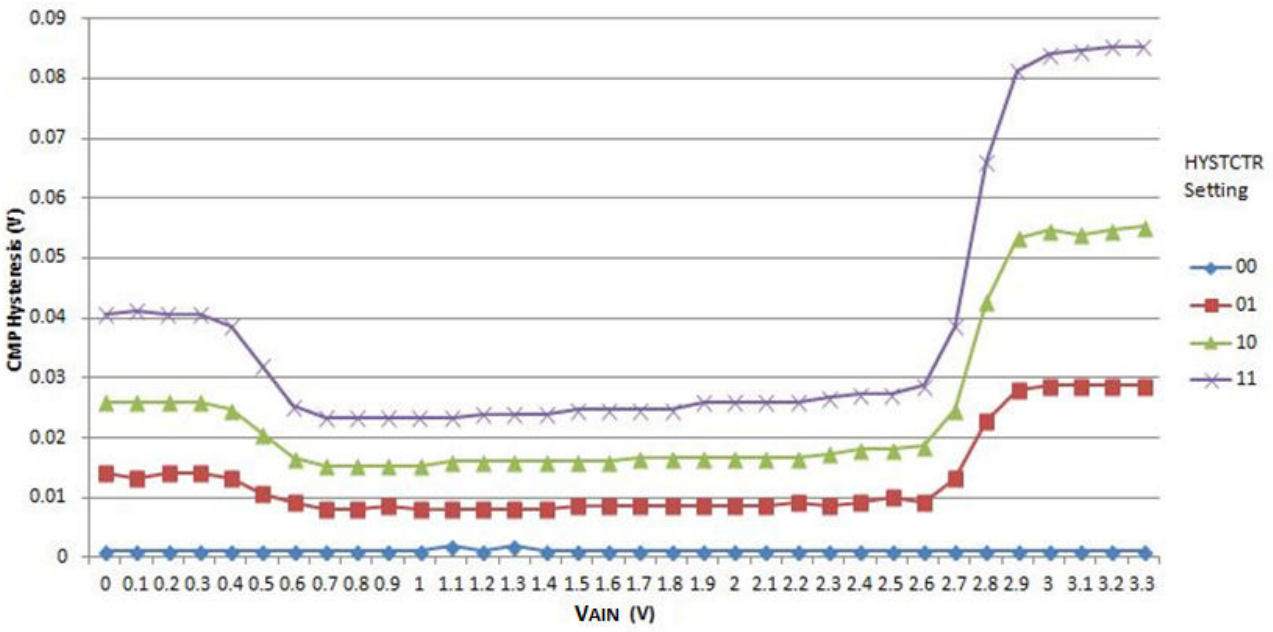


Figure 26. Typical hysteresis vs. V_{AIN} (VDDA = 3.3 V, PMODE = 0)

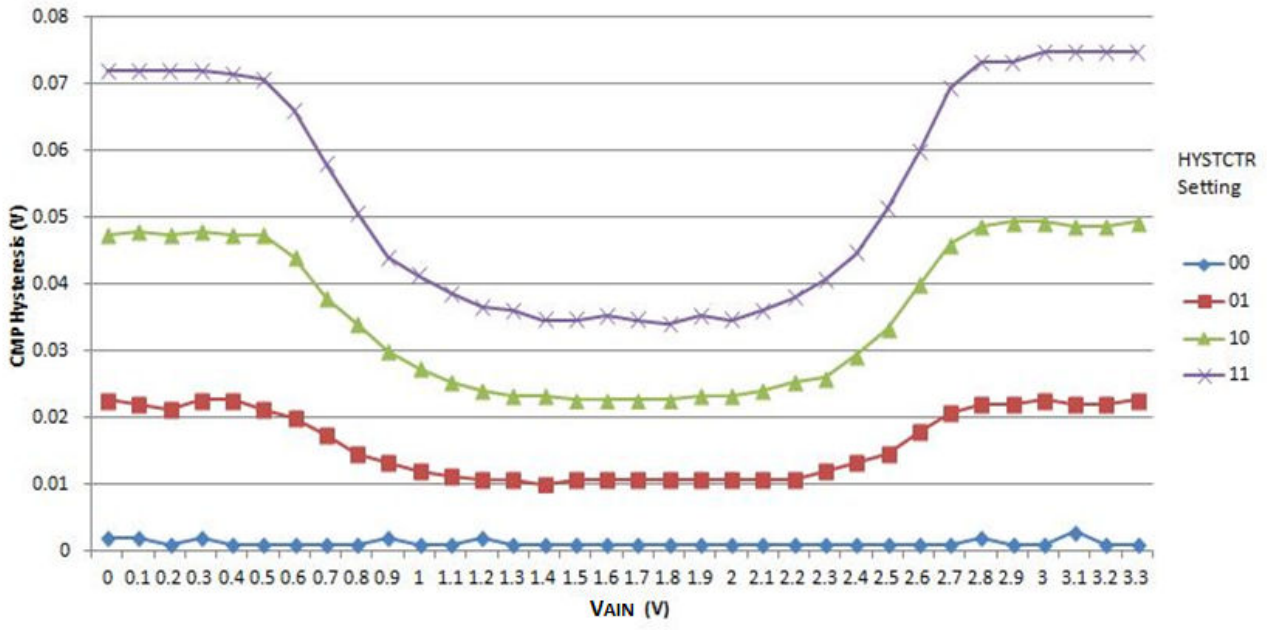


Figure 27. Typical hysteresis vs. V_{AIN} (VDDA = 3.3 V, PMODE = 1)

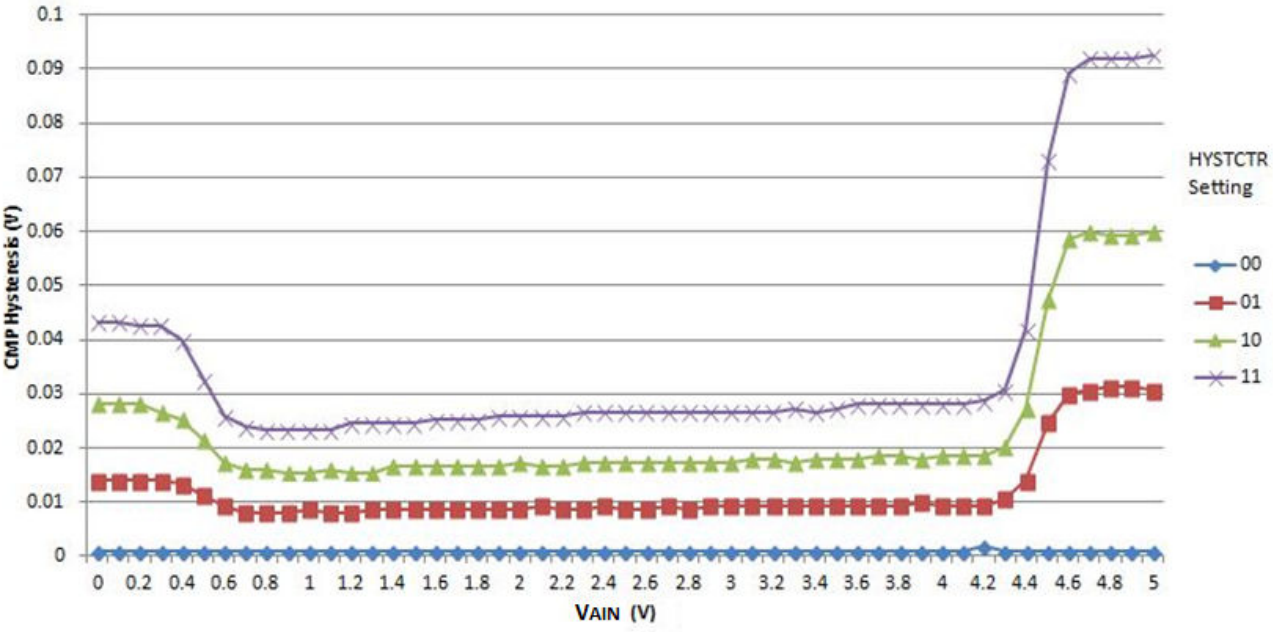


Figure 28. Typical hysteresis vs. V_{AIN} (VDDA = 5 V, PMODE = 0)

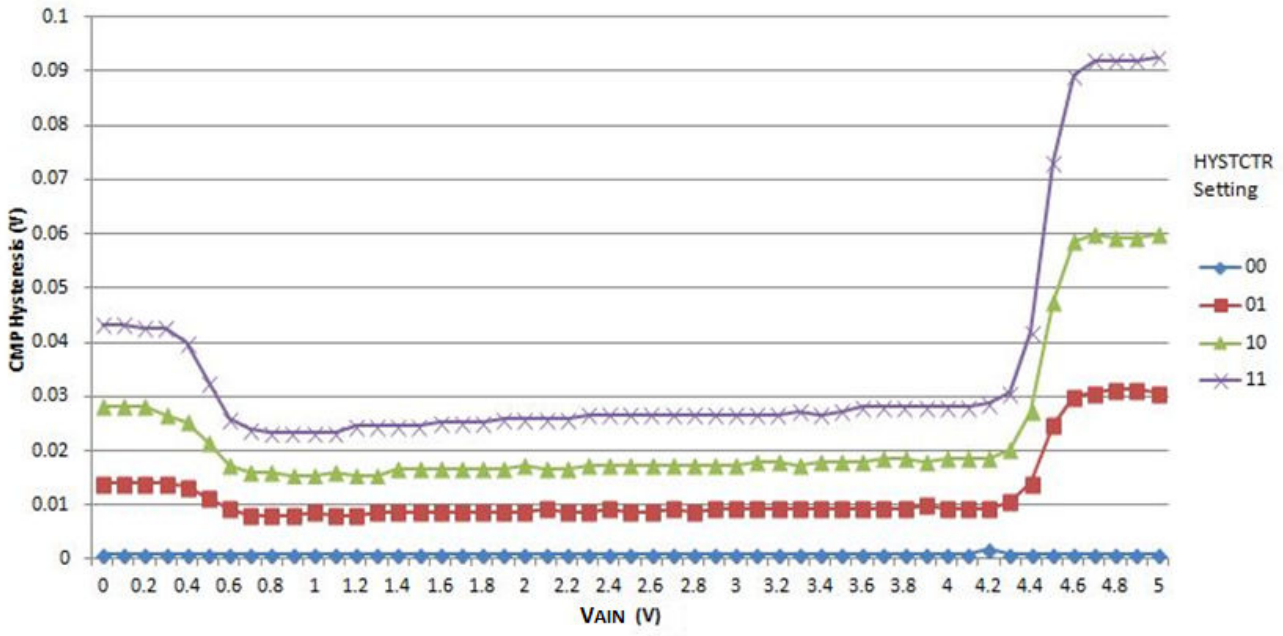


Figure 29. Typical hysteresis vs. V_{AIN} (VDDA = 5 V, PMODE = 1)

10.3.5 Communication modules

10.3.5.1 LPUART electrical specifications

Refer to General AC specifications for LPUART specifications.

Supported baud rate

Baud rate = Baud clock / ((OSR+1) * SBR).

For details, see LPUART chapter of the *Reference Manual*.

10.3.5.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

- All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds.
- All measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew setting (DSE = 1).

Table 75. LPSPI electrical specifications[1]

Num	Symbol	Description	Conditions	Run Mode[2]				VLPR Mode (S32M242)				VLPR Mode (S32M244)				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
	f_{periph} [3] [4]	Peripheral Frequency	Slave	-	40	-	40	-	4	-	4	-	1	-	1	MHz
			Master	-	40	-	40	-	4	-	4	-	1	-	1	
			Master Loopback[5]	-	40	-	48	-	4	-	4	-	1	-	1	
			Master Loopback(slow)[6]	-	48	-	48	-	4	-	4	-	1	-	1	
1	f_{op}	Frequency of operation	Slave	-	10	-	10	-	2	-	2	-	0.5	-	0.5	MHz
			Master	-	10	-	10	-	2	-	2	-	0.5	-	0.5	
			Master Loopback[5]	-	20	-	12	-	2	-	2	-	0.5	-	0.5	
			Master Loopback(slow)[6]	-	12	-	12	-	2	-	2	-	0.5	-	0.5	
2	t_{SPSCK}	SPSCK period	Slave	100	-	100	-	500	-	500	-	-	2000	-	2000	ns
			Master	100	-	100	-	500	-	500	-	-	2000	-	2000	
			Master Loopback[5]	50	-	83	-	500	-	500	-	-	2000	-	2000	
			Master Loopback(slow)[6]	83	-	83	-	500	-	500	-	-	2000	-	2000	
3	t_{Lead}[7]	Enable lead time (PCS to SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns

Table continues on the next page...

Table 75. LPSPI electrical specifications[1] (continued)

Num	Symbol	Description	Conditions	Run Mode[2]				VLPR Mode (S32M242)				VLPR Mode (S32M244)				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
			Master	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-50	-	(PCSSCK+1)*t_{periph}-50	-	(PCSSCK+1)*t_{periph}-115	-	(PCSSCK+1)*t_{periph}-115	-	
			Master Loopback[5]													
			Master Loopback(slow)[6]													
4	t_{Lag}[8]	Enable lag time (After SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns
			Master	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 50	-	(SCKPCS+1)*t_{periph}- 50	-	(PCSSCK+1)*t_{periph}-115	-	(PCSSCK+1)*t_{periph}-115	-	
			Master Loopback[5]													
			Master Loopback(slow)[6]													
5	t_{WSPSCK}[9]	Clock(SPSCK) high or low time (SPSCK duty cycle)	Slave	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-5	t_{SPSCK}/2+5	t_{SPSCK}/2-5	t_{SPSCK}/2+5	SPSCK/2-12	SPSCK/2+12	SPSCK/2-12	SPSCK/2+12	ns
			Master													
			Master Loopback[5]													
			Master Loopback(slow)[6]													
6	t_{SU}	Data setup time(inputs)	Slave	3	-	5	-	18	-	18	-	55	-	55	-	ns
			Master	29	-	38	-	72	-	78	-	145	-	145	-	

Table continues on the next page...

Table 75. LPSPI electrical specifications[1] (continued)

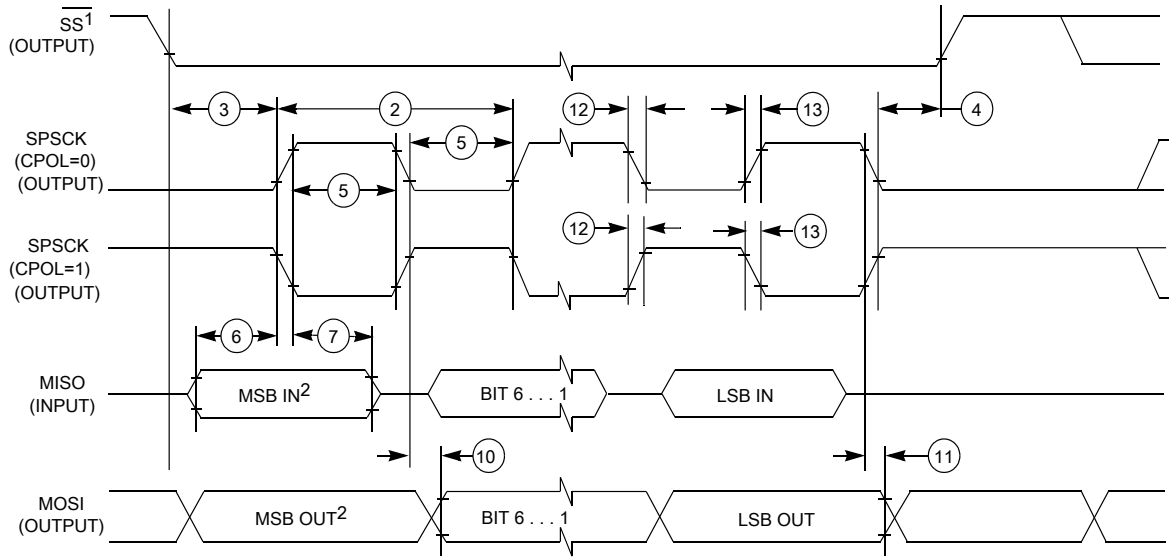
Num	Symbol	Description	Conditions	Run Mode[2]				VLPR Mode (S32M242)				VLPR Mode (S32M244)				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
			Master Loopback[5]	7	-	8	-	20	-	20	-	60	-	60	-	
			Master Loopback(slow)[6]	8	-	10	-	20	-	20	-	61	-	61	-	
7	t_{HI}	Data hold time(inputs)	Slave	3	-	3	-	14	-	14	-	27	-	27	-	ns
			Master	0	-	0	-	0	-	0	-	0	-	0	-	
			Master Loopback[5]	3	-	3	-	11	-	11	-	26	-	26	-	
			Master Loopback(slow)[6]	3	-	3	-	12	-	12	-	20	-	20	-	
8	t_a	Slave access time	Slave	-	50	-	50	-	100	-	100	-	180	-	180	ns
9	t_{dis}	Slave MISO (SOUT) disable time	Slave	-	50	-	50	-	100	-	100	-	180	-	180	ns
10	t_v	Data valid (after SPSCK edge)	Slave	-	30	-	39	-	92	-	96	-	190	-	190	ns
			Master	-	12	-	16	-	47	-	48	-	113	-	113	
			Master Loopback[5]	-	12	-	16	-	47	-	48	-	112	-	112	
			Master Loopback(slow)[6]	-	8	-	10	-	44	-	44	-	99	-	99	
11	t_{HO}	Data hold time(outputs)	Slave	4	-	4	-	4	-	4	-	4	-	4	-	ns
			Master	-15	-	-22	-	-22	-	-29	-	-30	-	-30	-	

Table continues on the next page...

Table 75. LPSPI electrical specifications[1] (continued)

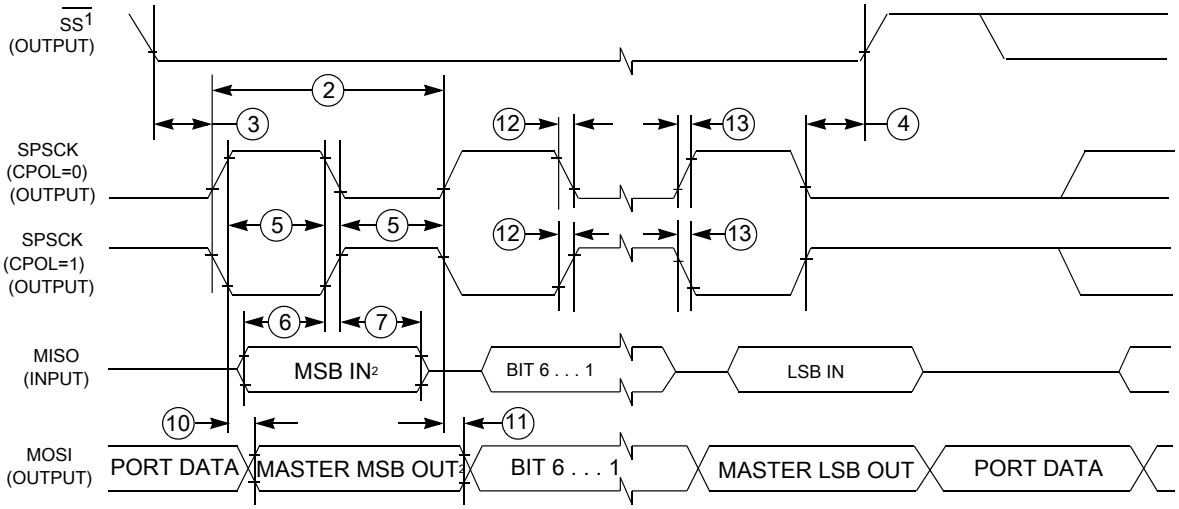
Num	Symbol	Description	Conditions	Run Mode[2]				VLPR Mode (S32M242)				VLPR Mode (S32M244)				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
			Master Loopback[5]	-10	-	-14	-	-14	-	-19	-	-19	-	-19	-	
			Master Loopback(slow)[6]	-15	-	-22	-	-21	-	-27	-	-30	-	-30	-	
12	$t_{RI/FI}$	Rise/Fall time input	Slave	-	1	-	1	-	1	-	1	-	1	-	1	ns
			Master	-		-		-		-		-		-		
			Master Loopback[5]	-		-		-		-		-		-		
			Master Loopback(slow)[6]	-		-		-		-		-		-		
13	$t_{RO/FO}$	Rise/Fall time output	Slave	-	25	-	25	-	25	-	25	-	25	-	25	ns
			Master	-		-		-		-		-		-		
			Master Loopback [5]	-		-		-		-		-		-		
			Master Loopback(slow) [6]	-		-		-		-		-		-		

1. Trace length should not exceed 11 inches for SCK pad when used in Master loopback mode.
2. While transitioning from HSRUN mode to RUN mode, LPSPI output clock should not be more than 14 MHz.
3. f_{periph} = LPSPI peripheral clock
4. $t_{periph} = 1/f_{periph}$
5. Master Loopback mode - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pads used are PTD15 and PTE0. Applicable only for LPSPI0.
6. Master Loopback (slow) - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pad used is PTB2. Applicable only for LPSPI0.
7. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where PCSSCK ranges from 0 to 255.
8. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where SCKPCS ranges from 0 to 255.
9. While selecting odd dividers, ensure Duty Cycle is meeting this parameter.



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

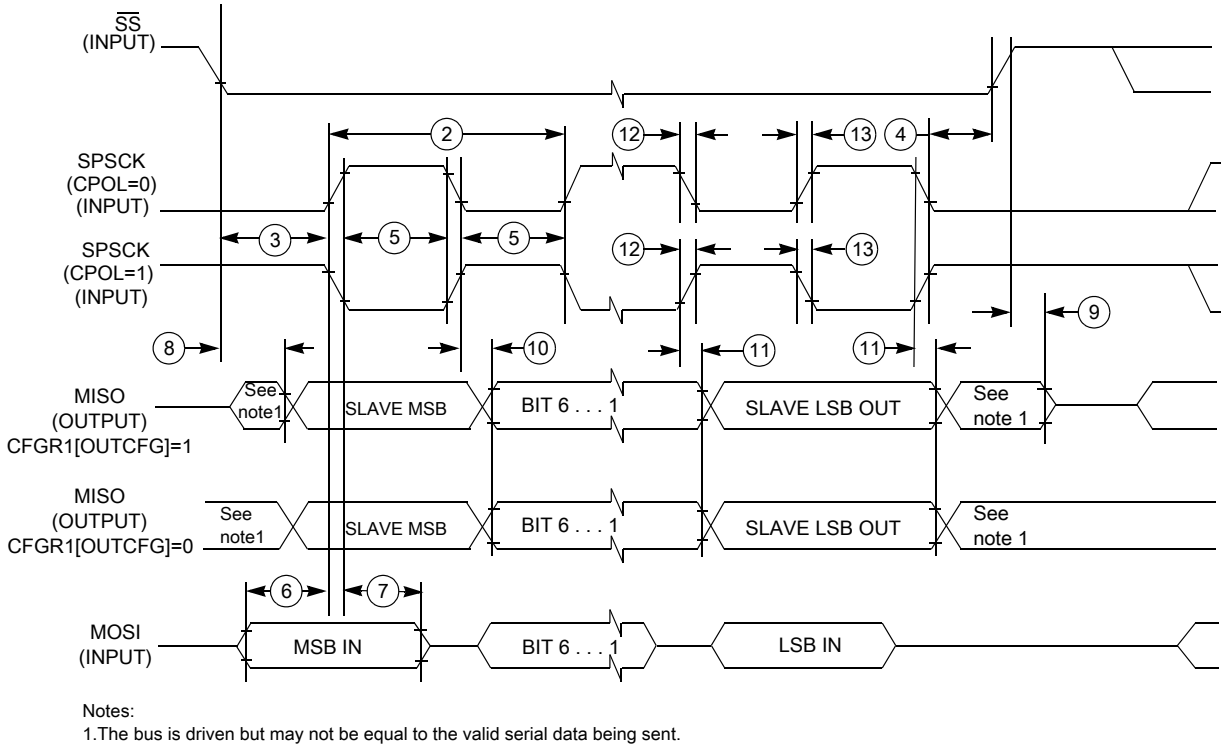
Figure 30. LPSPI master mode timing (CPHA = 0)



1.If configured as output

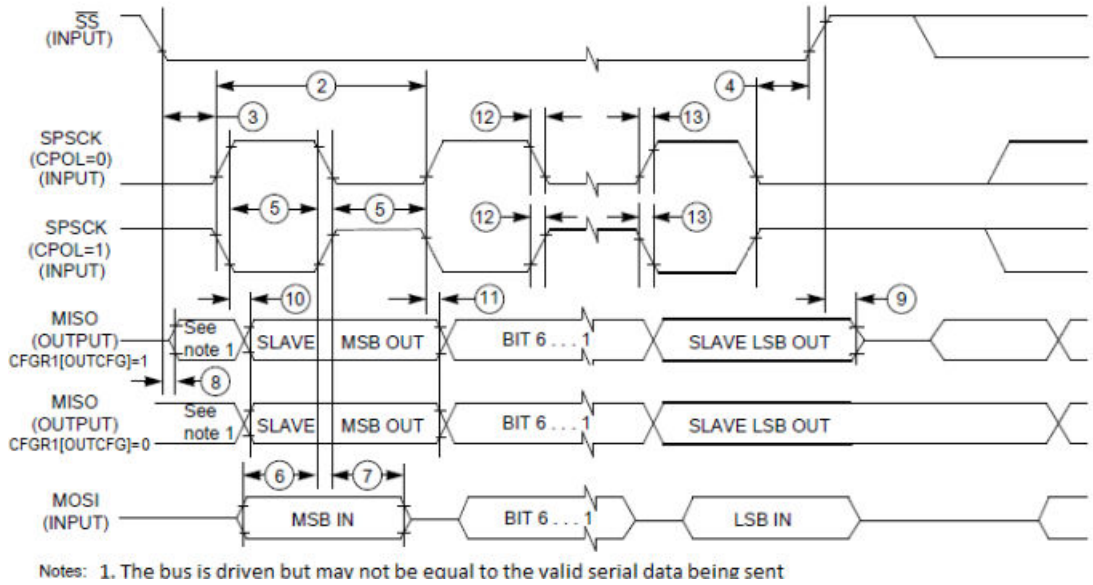
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 31. LPSPI master mode timing (CPHA = 1)



Notes:
1.The bus is driven but may not be equal to the valid serial data being sent.

Figure 32. LPSPI slave mode timing (CPHA = 0)



Notes: 1. The bus is driven but may not be equal to the valid serial data being sent

Figure 33. LPSPI slave mode timing (CPHA = 1)

10.3.5.3 LPI2C electrical specifications

See General AC specifications for LPI2C specifications.

For supported baud rate see section 'Chip-specific LPI2C information' of the *Reference Manual.*

10.3.5.4 FlexCAN electical specifications

For supported baud rate, see section 'Protocol timing' of the *Reference Manual*.

10.3.5.5 Clockout frequency

Maximum supported clock out frequency for this device is 20 MHz

10.3.6 Debug modules

10.3.6.1 SWD electrical specofications

Table 76. SWD electrical specifications

Symbol	Description	Run Mode				VLPR Mode (S32M242)				VLPR Mode (S32M244)				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
S1	SWD_CLK frequency of operation	-	25	-	25	-	10	-	10	-	1	-	1	MHz
S2	SWD_CLK cycle period	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	ns
S3	SWD_CLK clock pulse width	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2-5	S2/2+5	S2/2-5	S2/2+5	ns
S4	SWD_CLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	4	-	4	-	16	-	16	-	30	-	30	-	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	3	-	3	-	10	-	10	-	19	-	19	-	ns
S11	SWD_CLK high to SWD_DIO data valid	-	28	-	38	-	70	-	77	-	180	-	180	ns
S12	SWD_CLK high to SWD_DIO high-Z	-	28	-	38	-	70	-	77	-	180	-	180	ns
S13	SWD_CLK high to SWD_DIO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns

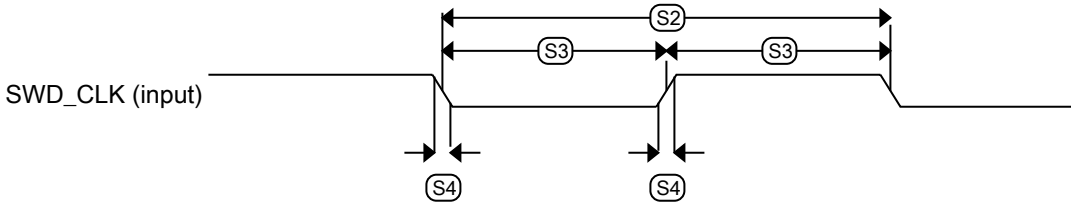


Figure 34. Serial wire clock input timing

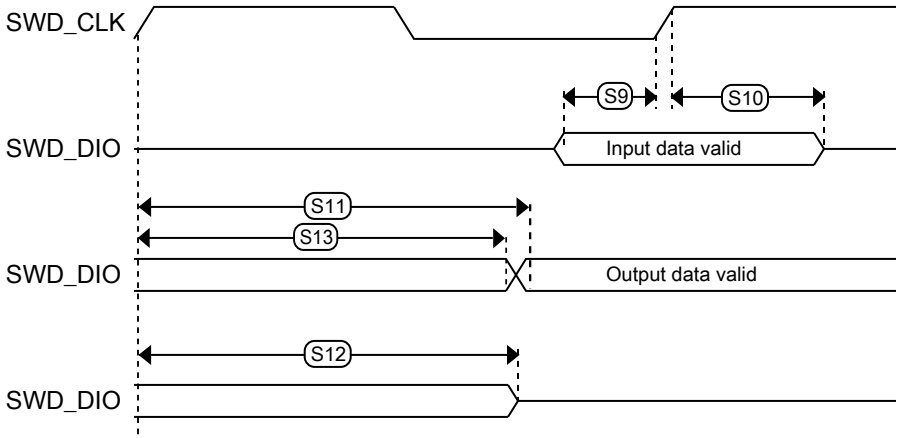


Figure 35. Serial wire data timing

10.3.6.2 JTAG electrical specifications

Table 77. JTAG electrical specifications

Symbol	Description	Run Mode				VLPR Mode (S32M242)				VLPR Mode (S32M244)				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		5.0 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min	Max	Min	Max	
JI	TCLK frequency of operation													MHz
	Boundary Scan	-	20	-	20	-	10	-	10	-	1	-	1	
	JTAG	-	20	-	20	-	10	-	10	-	1	-	1	
J2	TCLK cycle period	1/JI	-	1/JI	-	1/JI	-	1/JI	-	1/J1	-	1/J1	-	ns
J3	TCLK clock pulse width													ns
	Boundary Scan	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	
	JTAG													
J4	TCLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
J5	Boundary scan input data setup time to TCLK rise	5	-	5	-	15	-	15	-	23	-	23	-	ns
J6	Boundary scan input data hold time after TCLK rise	5	-	5	-	8	-	8	-	20	-	20	-	ns
J7	TCLK low to boundary scan output data valid	-	28	-	32	-	80	-	80	-	184	-	184	ns
J8	TCLK low to boundary scan output data invalid	0	-	0	-	0	-	0	-	0	-	0	-	
J9	TCLK low to boundary scan output high-Z	-	28	-	32	-	80	-	80	-	184	-	184	ns
J10	TMS, TDI input data setup time to TCLK rise	3	-	3	-	15	-	15	-	23	-	23	-	ns
J11	TMS, TDI input data hold time after TCLK rise	2	-	2	-	8	-	8	-	20	-	20	-	ns
J12	TCLK low to TDO data valid	-	28	-	32	-	80	-	80	-	184	-	184	ns
J13	TCLK low to TDO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns
J14	TCLK low to TDO high-Z	-	28	-	32	-	80	-	80	-	184	-	184	ns

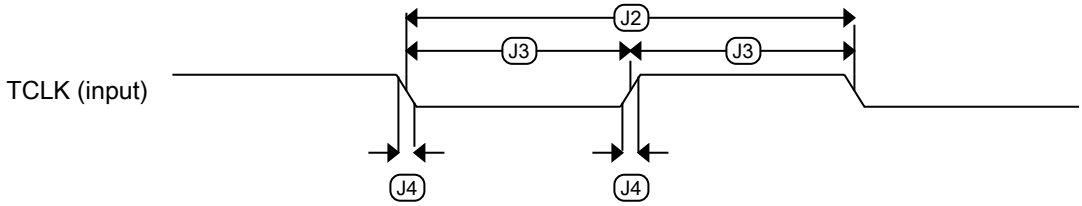


Figure 36. Test clock input timing

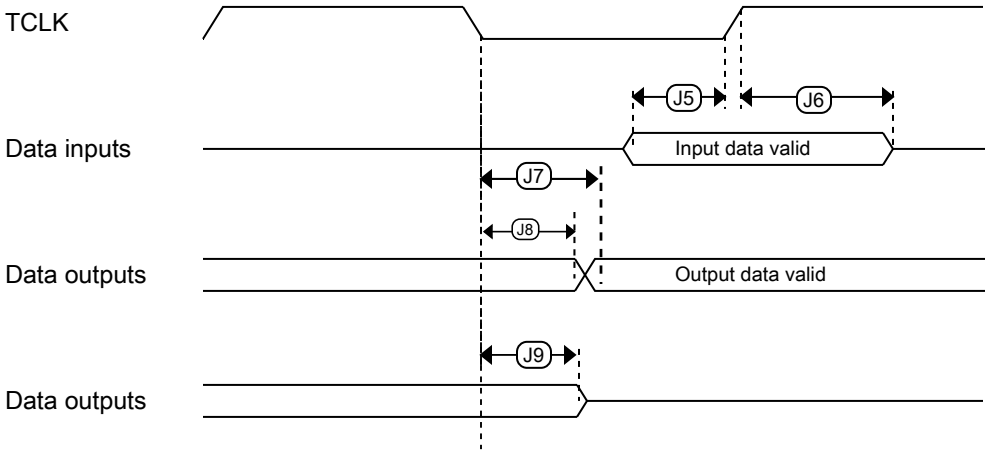


Figure 37. Boundary scan (JTAG) timing

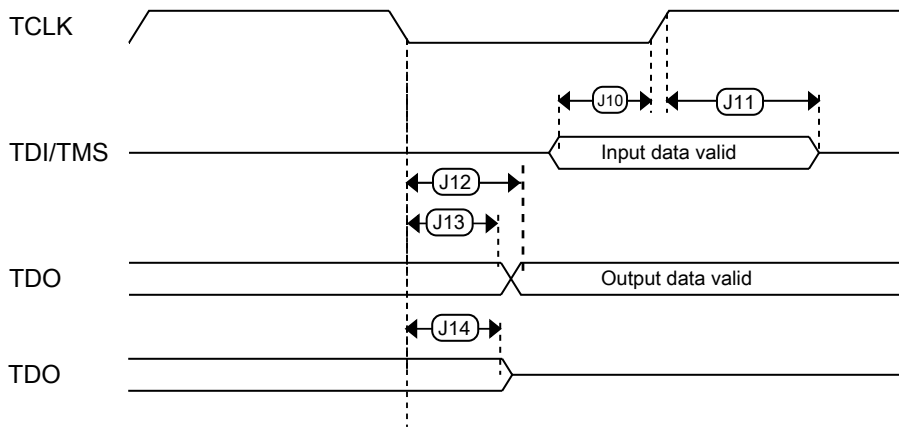


Figure 38. Test Access Port timing

10.4 Thermal attributes

10.4.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on a board with internal plane (2s2p) is usually appropriate if the board has low power dissipation and the components are well separated.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

- T_T = thermocouple temperature on top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the

package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

11 Thermal Characteristics

Table 78. Thermal characteristics

Rating	Board Type[1]	Symbol	S32M242 S32M241	S32M244 S32M243	S32M276 S32M274	Unit
Junction to Ambient Thermal Resistance[2]	JESD51-7, 2s2p	$R_{\theta JA}$	29	28.3	26.5	°C/W
Junction-to-Top of Package Thermal Characterization Parameter[2]	JESD51-7, 2s2p	Ψ_{JT}	8.1	8.2	6.5	°C/W

1. Thermal test board meets JEDEC specification for this package (JESD51-7).
2. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

12 Package

The S32M is offered in the following package types.

Table 79. Packaging

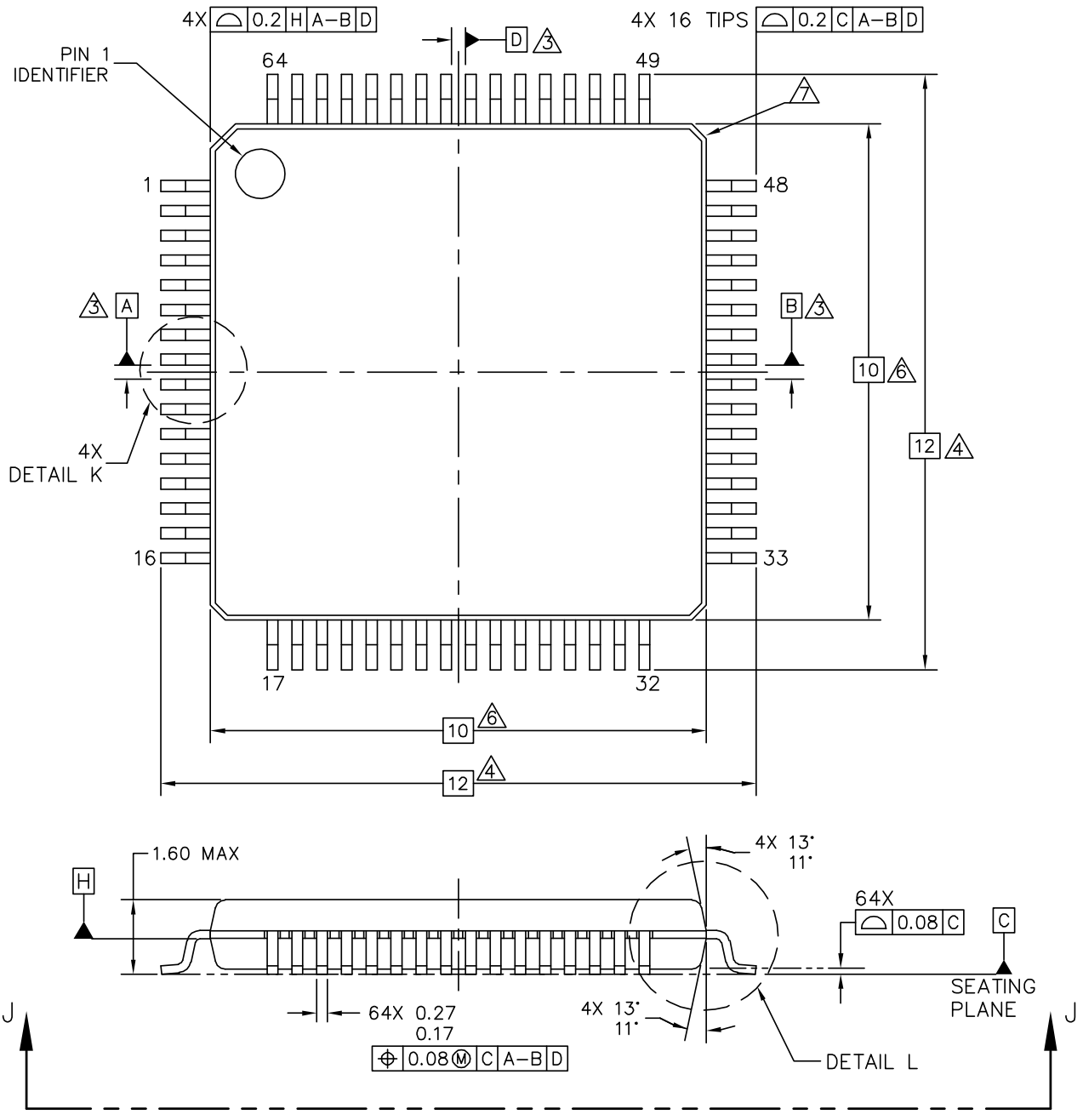
Package type	Document number
64LQFP_EP	98ASA10763D

NOTE

To find a package drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number or see below figures.

MECHANICAL OUTLINE

DO NOT SCALE THIS DRAWING

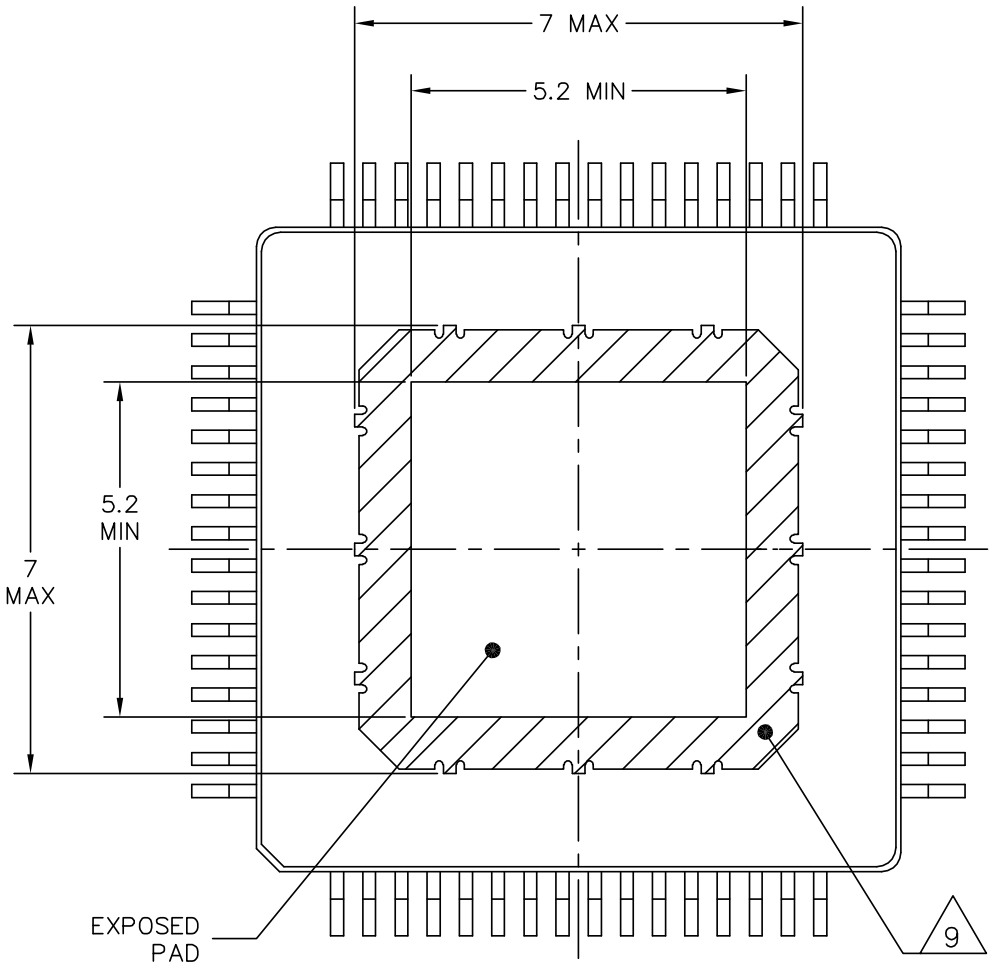


TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D REV: E
	STANDARD: JEDEC MS-026 BCD
	SOT1510-2 SHEET: 1 OF 8

Figure 39. Package outline 1 of 3

MECHANICAL OUTLINE

DO NOT SCALE THIS DRAWING



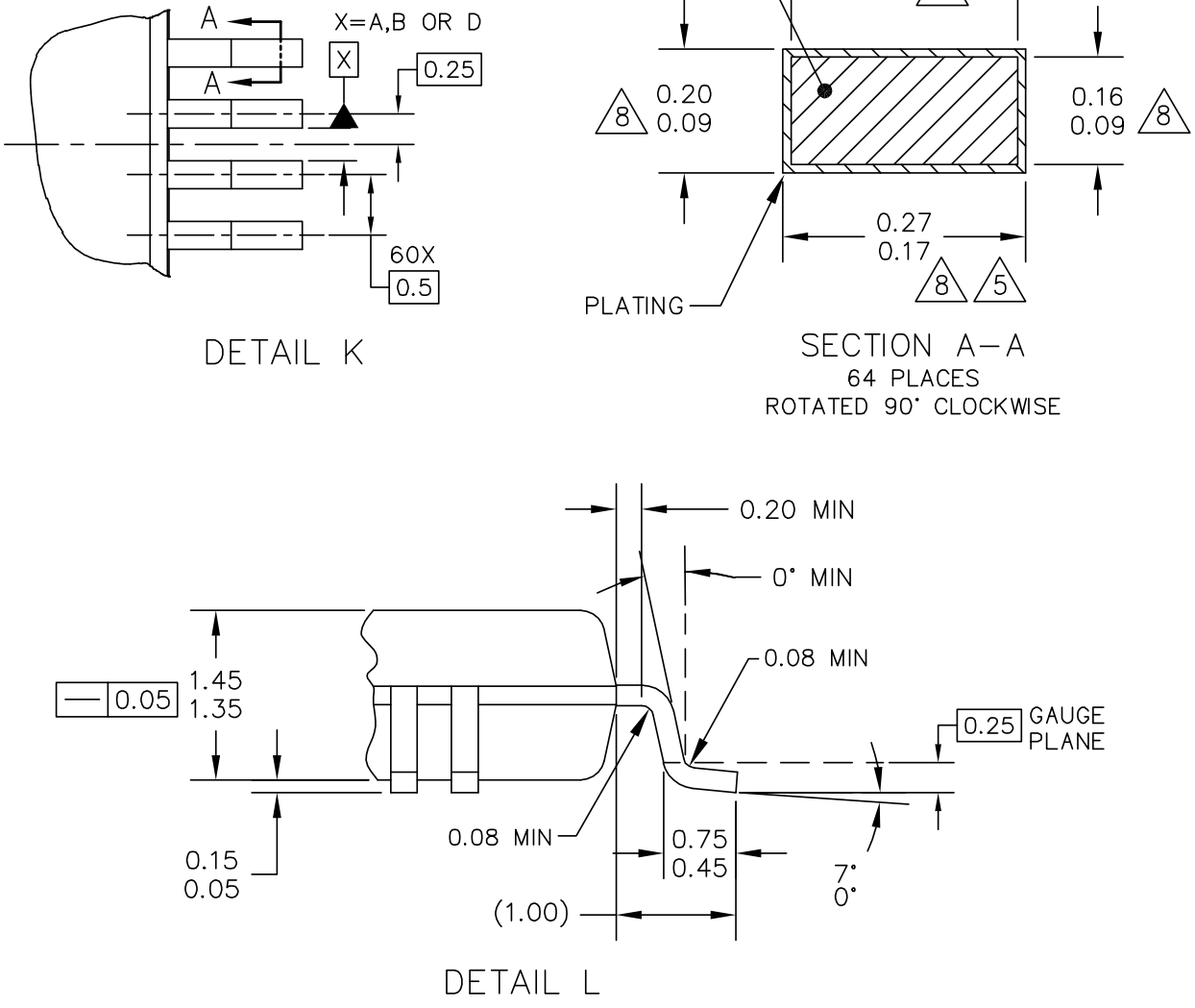
VIEW J–J

TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D REV: E
	STANDARD: JEDEC MS-026 BCD
	SOT1510-2 SHEET: 2

Figure 40. Package outline 2 of 3

MECHANICAL OUTLINE

DO NOT SCALE THIS DRAWING

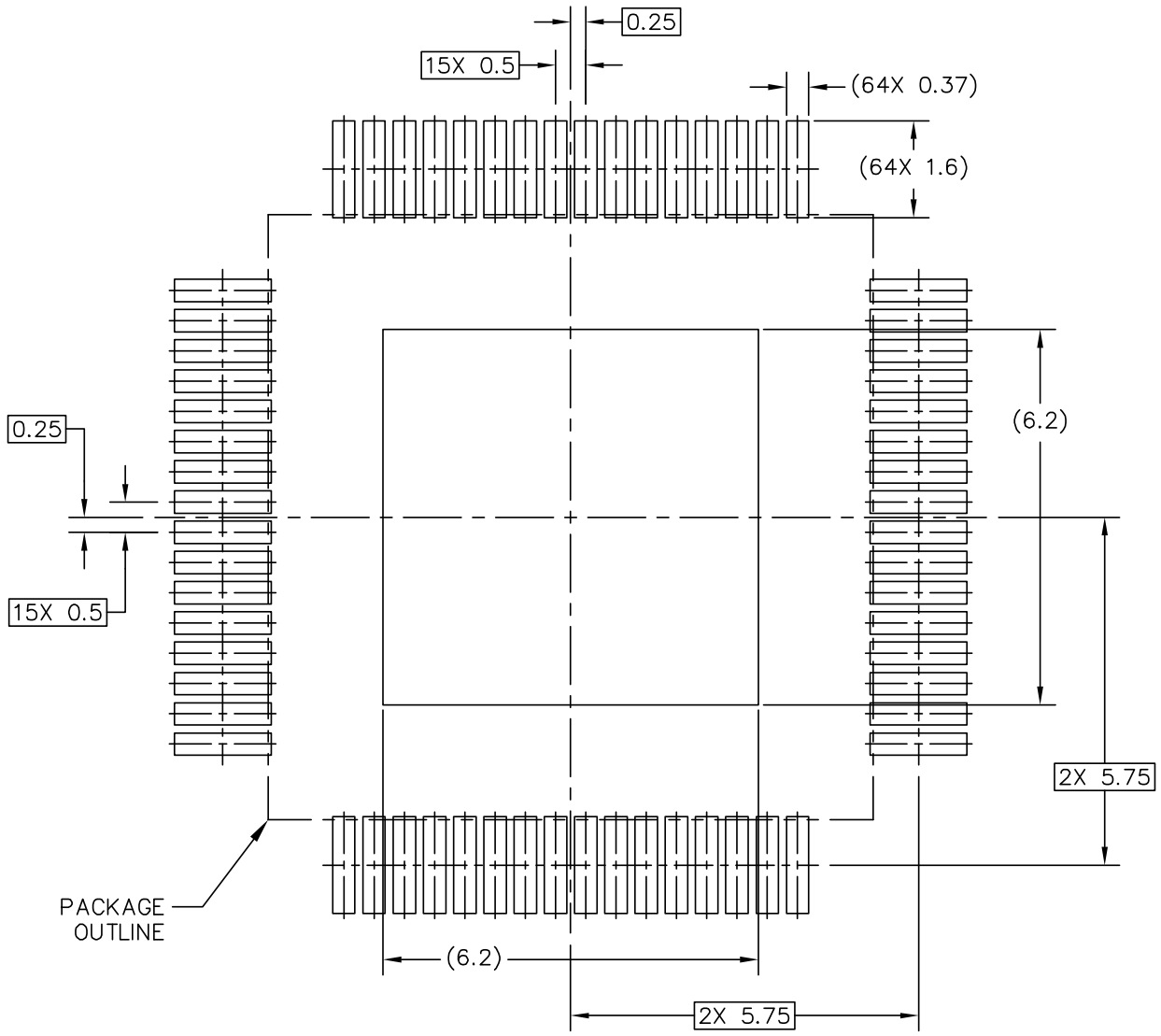


TITLE:	LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D REV: E
		STANDARD: JEDEC MS-026 BCD
		SOT1510-2 SHEET: 3

Figure 41. Package outline 3 of 3

MECHANICAL OUTLINE

DO NOT SCALE THIS DRAWING



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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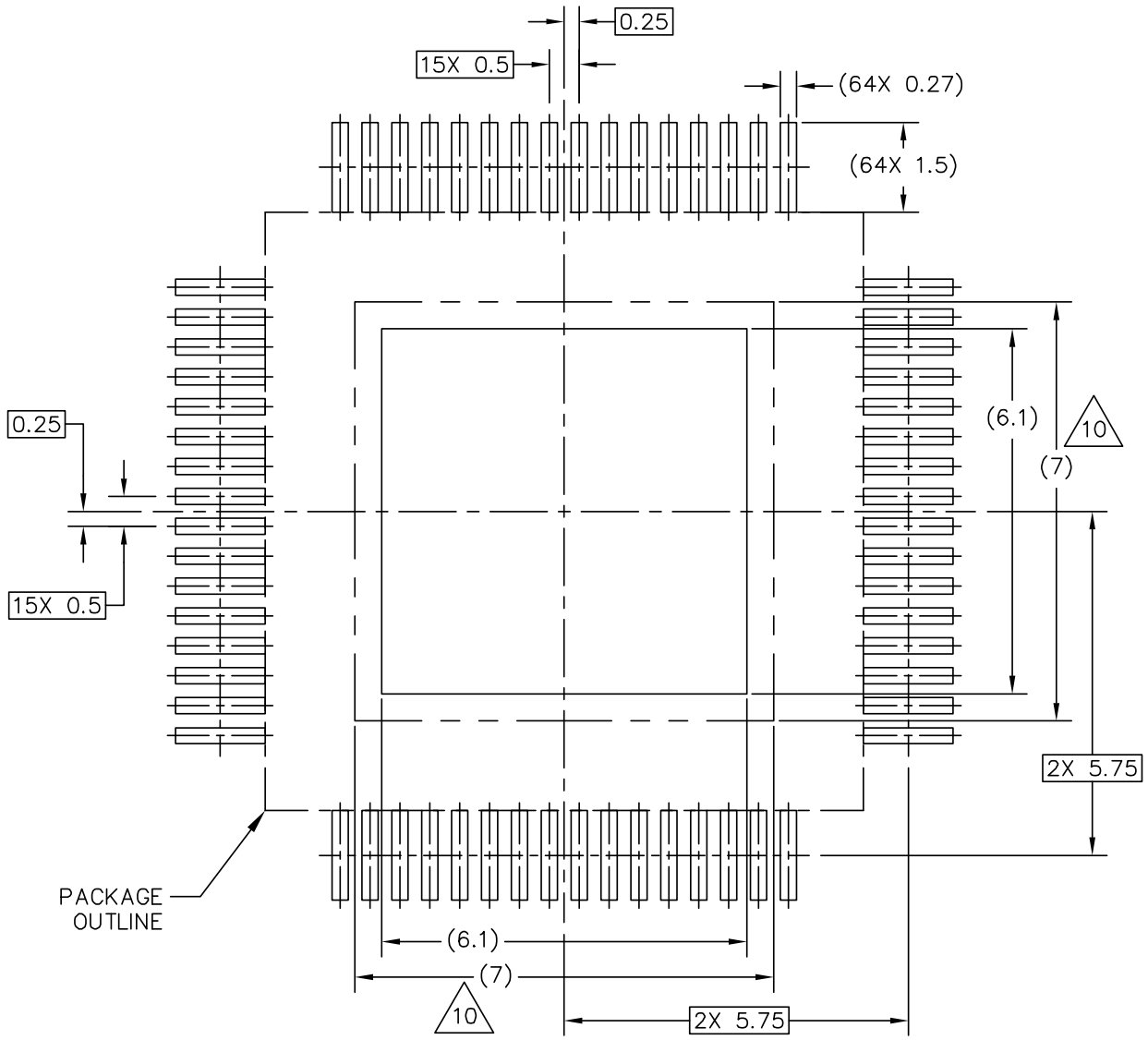
	STANDARD: JEDEC MS-026 BCD
	SOT1510-2 SHEET: 4

Figure 42. PCB design guidelines - solder mask opening pattern

MECHANICAL OUTLINE

DO NOT SCALE THIS DRAWING



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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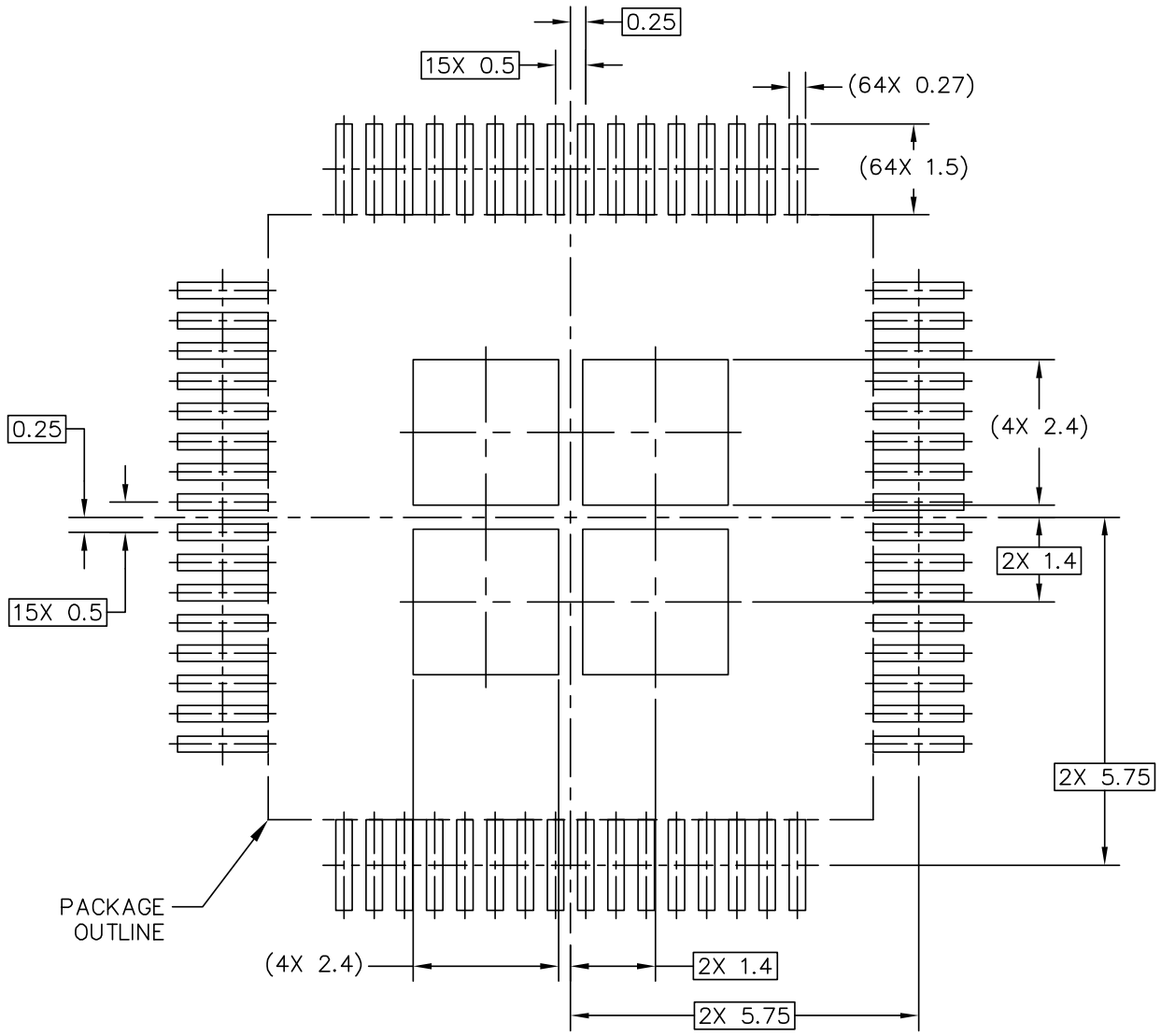
TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D REV: E
	STANDARD: JEDEC MS-026 BCD
	SOT1510-2 SHEET: 5

Figure 43. PCB design guidelines - I/O pads and solderable area

MECHANICAL OUTLINE

DO NOT SCALE THIS DRAWING



STENCIL THICKNESS 0.125 OR 0.150

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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TITLE:	LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D REV: E
		STANDARD: JEDEC MS-026 BCD
		SOT1510-2 SHEET: 6

Figure 44. PCB design guidelines - solder paste stencil

MECHANICAL OUTLINE

DO NOT SCALE THIS DRAWING

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.
9. HATCHED AREA REPRESENTS POSSIBLE MOLD FLASH ON EXPOSED PAD.
10. KEEP OUT ZONE REPRESENTS AREA ON PCB THAT MUST NOT HAVE ANY EXPOSED METAL (EG. TRACE/VIA) FOR PCB ROUTING DUE TO THE POSSIBILITY OF SHORTING TO TIE BAR/EXPOSED PAD.

TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D	REV: E
	STANDARD: JEDEC MS-026 BCD	
	SOT1510-2	SHEET: 7

Figure 45. Package drawing notes

13 Revision history

The following table lists the changes in this document.

Rev 3, Oct 2023
• Updated S32M27x block diagram. • Updated ordering information. • In section "Absolute maximum ratings", updated footnote "For S32M24x devices, VDD_AE10, VDD...". • In section "Thermal operating characteristics" deleted storage temperature range. • In section "PMC Electrical Specifications": — Limits and condition updated for V_VDD_5Vmode, VDD_REG_DYN, and VDDC. — Condition updated for V_VDD_3Vmode, IVDD_LD_FP, and IVDD_LD_LP. • In section "Voltage Monitors in Application Extension PMC" updated VDD_OV1 max to 5.55V and VDDC_UV max to 4.9V. • In section "Application Extension IO DC electrical specifications", updated max IO_VDDE_IOCD from 100 to 175 mA • In section "42 MHz RC Oscillator electrical specifications" updated fosc. • In section "CANPHY Electrical Specifications" added tbit(bus) and delta-trec parameters. • Updated "DPGA Electrical Specifications". • In section "Temperature Monitor Electrical Specifications" — added TTSENSE_* parameters for different temperature ranges and updated TOT_1. — updated TTSENS_acc_offset limit to +/-2 C and added clarification about different instances of temp monitor "There are two temperature sensors, one instance located in vicinity of...". • Added section "Supply Diagnosis". • In section "LPSPI" updated specification and diagrams to represent voltage measurment at 50% and updated symbol for "Data hold time (inputs)" from tHO to tHI. • In section "DPGA Electrical Specifications" clarified VIN in the footnote. • In section "GDU", clarified VIN and updated respective footnotes. • In comparator sections of both S32M24x and S32M27x, changed VIN level to corresponding parameter, VAIN. • In section LPUART section of S32M24x, reffered to LPUART chapter. • Added package drawings.

Rev 3 DraftA, May 2023
• In "Block diagram" added introduction to explain the diagram. • In feature comparison changed "Flash with ECC protection" to "Program flash memory" and "Data flash" to "Flash memory". • Updated Ordering information to remove TBDs. • In section "Absolute maximum ratings",

Table continues on the next page...

Rev 3 DraftA, May 2023
— changed the description of VHSx and VLSx from 1us to 100ns. — updated footnote attached to VHGx and VLGx. • In section "Application Extension IO DC electrical specifications" changed CJTAG to AMPOUT and updated IO_VDDE_IOCD from 100 to 175 mA. • In section "High Voltage Module (HVM)": — updated HVM_AIM limit from +/-4 to +/-5% for ratio 2, 7, 11, 16 as mentioned in the condition which is also updated (was 40°C <= Tj<=125°C) — updated HVM_AIM condition from 125°C < Tj to Ratio 1. — updated VM_LBI1H, VM_LBI2H and VM_LBI3H from 0.6 to 0.8V — updated VM_HBI1H and VM_HBI2H from 1 to 1.35V. — updated VM_HBI2A min from 24 to 23.5 V. • In section "CANPHY Electrical Specifications", tdom,TXD symbol updated to tCPTXDDT. • In section "GDU Electrical Specifications", is updated thouroghly. • In section "Temperature Monitor Electrical Specifications" mentioned it is AE on-die temperature sensor. • In section "SAR ADC" updated leading sentence and added footnote to TUE with condition "without adjacent pincurrent injection". • In section "SAR ADC" updated figure "SAR ADC Input Circuit" to update ADC supply from VREFH to VDD_HV_A. • In section "Low Power Comparator (LPCMP)": — updated description of tDDAC from "DAC Initializationand switchingsettling time" to "DAC Initialization time" — updated footnote attached to TDHSS. — changed ACMP0 to LPCMP0. • In section "Temperature Sensor" mentioned it is MCU on -die temperature sensor. • In section "Fast External Oscillator (FXOSC)", — added Oscillator Analog circuit supply current for ALC disabled and added specifications related to Input clock low/high level in bypass mode. — removed a note "To improve the FXOSC jitter & duty...". • In section "PLL" added sentence "Jitter values specified in this table are applicable for FXOSC reference clock input only" and updated footnote to cyclic jitter specification to mention "Accumulated jitter specification is not valid with SSCG". • Updated "Thermal attributes" section thoroughly.

Rev 2.1, Jan 2023
• Updated S32M27x block diagram.

Rev 2, Jan 2023
• Updated block diagrams and feature comparison. • Added "ordering information". • In section “Voltage and current operating requirements”, changed Vramp_fast from 32 to 100V/ms. • In section "ESD and Latch-up Protection Characteristics", added new footnote and added it to VHBM (CANH and CANL pins). Also attached footnote 3 to VHBM (LIN and HVI0 pins). • In table "IDD modes" removed VLPR mode column and PDB row and updated FlexTimer to PWM (FTM/eMIOS). • In section "PMC Electrical Specifications", for CVLS, CVDD and CVDDC added typical value as 2.2 or 4.7 uF and removed LIN specifications. • Updated section name from "High Voltage Input" to "High Voltage Module (HVM) electrical specifications". • In section "Application Extension IO DC electrical specifications", updated supply names and added specification "IO_RESET_NOT_FILTERED_PULSE". • In section "High Voltage Input", updated symbols HVM_AIM and deleted HVM_VTHT33. • In section "CANPHY Electrical Specifications", — deleted I(VSUP)_CANPHY_wakeup, "tdom,bus" and VO(diff)_dom with RL=50 to 60 ohm. — Updated min from 1.4 to 1.5 V and max from 3.3 to 3 V for VO(diff)_dom with condition RL=45 to 70 ohm. — Updated min from -50 to -500 mV for VO(diff)_rec (Normal mode). — For "|IO(sc)|", updated condition. • In "LINPHY Electrical Specifications" deleted ΔIVSUP_LIN_wup". • Updated symbols, conditions and footnotes in "GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)" and "GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)" sections. • In section "Fast External Oscillator (FXOSC)" added EXTAL_SWING_PP and VSB specifications.

Rev 1, Aug 2022
• Initial release.

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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