RW610FML

RW610FML

Rev. 1.0 — 2 November 2026 Data sheet

1 General description

RW610FML is a low-power, high-performance certified Wi-Fi and Bluetooth combo module supporting IEEE 802.11a/b/g/n/ac/ax and Bluetooth Low Energy (LE) 6.3 protocols.

RW610FML provides a comprehensive set of peripheral interfaces, including GPIO, SDIO, UART, SPI, PCM, I²C, I²S, PWM, ADC, DAC, USB, JTAG, SWD, LCD, DMIC, ACOMP, UTICK, USIM, WCI-2, and PTA, supported via pin multiplexing. These interfaces enable flexible system design and support a wide range of consumer applications.

2 Key features

RW610FML integrates processing, wireless connectivity, memory, peripheral interfaces, and antenna functionality in a compact surface-mount module.

- NXP RW610 inside
- 260 MHz Arm Cortex-M33
- Supports IEEE 802.11a/b/g/n/ac/ax specification: Dual-band 2.4 GHz and 5 GHz Wi-Fi 6 SISO with 20 MHz channels; up to MCS9 data rates
- Supports Bluetooth LE specification version 6.3
- Built-in 8 MB NOR flash
- FlexSPI external flash interface supports eXecute-In-Place (XIP) and on-the-fly firmware encryption/decryption and authentication
- Supports GPIOs, SDIO, UART, SPI, PCM, I²C, I²S, PWM, ADC, DAC, USB, JTAG, SWD, LCD, DMIC, ACOMP, UTICK, USIM, WCI-2, and PTA interfaces
- Onboard PCB antenna
- Normal operating temperature range: -40 °C to 85 °C[1]
- Storage temperature: -45 °C to +95 °C
- Dimensions: (25.5 ± 0.2) mm × (18 ± 0.2) mm × (3.16 ± 0.2) mm
- Weight: 1.51 g (approx.)
- MSL: 3
- Surface mount type

3 Applications

RW610FML is designed for a range of connected consumer, industrial, and infrastructure applications.

Target applications

- Smart appliances
- Smart home
- Gateways/Hubs
- Industrial automation

1 Products are designed for use in devices with a typical lifetime around 5 years.

- Electric charging stations
- Medical/healthcare

4 Ordering information

The part number and associated ordering information are shown in Table 1.

Table 1. Ordering information

Part number	Description
RW610FML/A2AIR	F: Dual-band w/BT ML: LGA A2: Chip revision A: Module revision I: Industrial grade R: Tape and reel

5 Block diagram

Figure 1 shows the block diagram of RW610FML and illustrates the major functional parts.

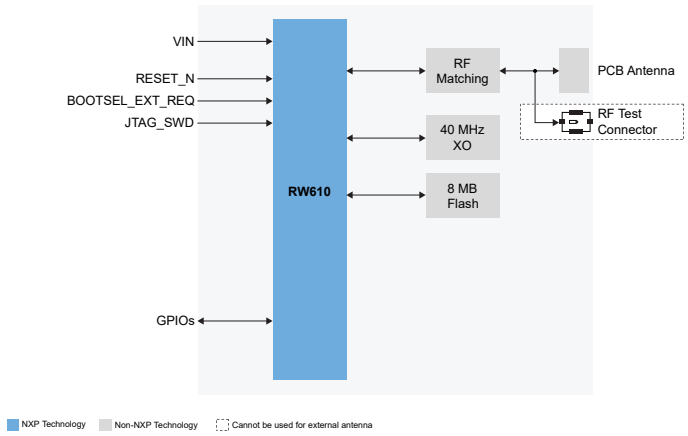


Figure 1. RW610FML block diagram

6 Pin information

This section provides an overview of the module pin architecture and signal allocation.

6.1 Pin assignment

Figure 2 shows the top view of RW610FML pin assignment.

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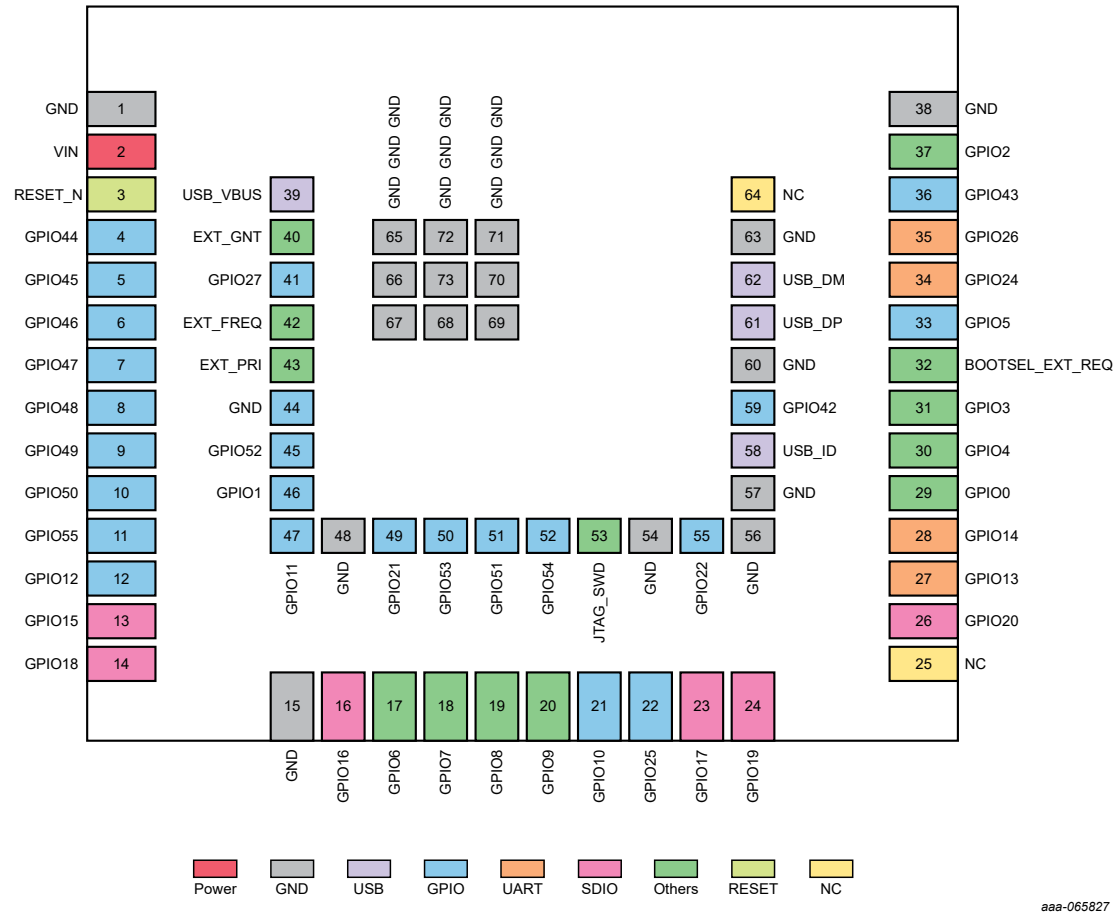


Figure 2. Top view of RW610FML pin assignment

6.2 Pin lists

Table 2 lists the pin description of RW610FML.

Table 2. Pin lists

Pin no	Pin name	Reset state	Pin type	Description
1	GND	-	PWR	Ground
2	VIN	-	PWR	Power supply for the RW610FML V = 3.14 V~3.6 V Provide sufficient current of at least 0.6 A
3	RESET_N	-	I	Full Power-down (input) (active low) 0 = Full Power-down mode 1 = Normal mode
4	GPIO44	Input	I/O	**GPIO mode**: General-purpose I/O 44
			A,O	**DAC_A**: DAC channel A
			A,I	**ADC0_2**: ADC0 channel 2
			A,I	**ACOMP2**: ACOMP channel 2
			O	**LCD SPI mode**: output signal to reset the device

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Table 2. Pin lists*...continued*

Pin no	Pin name	Reset state	Pin type	Description
			I/O	**Secure GPIO mode**: SPIO0[12]
5	GPIO45	Input	I/O	**GPIO mode**: General-purpose I/O
			I	**LCD SPI mode**: LCD tearing effect input signal used to synchronize MCU frame writing
			A,I	**ADC0_3**: ADC0 channel 3
			A,I	**ACOMP3**: ACOMP channel 3
			A,I	**EXT_VREF_ADC0_DAC**: ADC0 or DAC external voltage reference input
			I/O	**Secure GPIO mode**: SPIO0[13]
6	GPIO46	Input	I/O	**GPIO mode**: General-purpose I/O 46
			I/O	**LCD SPI mode**: LCD SPI interface data input/output
			A,I	**ADC0_4**: ADC0 channel 4
			A,I	**ACOMP4**: ACOMP channel 4
			I/O	**Secure GPIO mode**: SPIO0[14]
7	GPIO47	Input	I/O	**GPIO mode**: General-purpose I/O 47
			O	**LCD SPI mode**: LCD SPI interface data/command output
			A,I	**ADC0_5**: ADC0 channel 5
			A,I	**ACOMP5**: ACOMP channel 5
			I/O	**Secure GPIO mode**: SPIO0[15]
8	GPIO48	Input	I/O	**GPIO mode**: General-purpose I/O 48
			O	**LCD SPI mode**: LCD SPI interface clock
			A,I	**ADC0_6**: ADC0 channel 6
			A,I	**ADC1_6**: ADC1 channel 6
			A,I	**ACOMP6**: ACOMP channel 6
			I/O	**Secure GPIO mode**: SPIO0[16]
9	GPIO49	Input	I/O	**GPIO mode**: General-purpose I/O 49
			O	**LCD SPI mode**: LCD SPI interface chip select
			A,I	**ADC0_7**: ADC0 channel 7
			A,I	**ADC1_7**: ADC1 channel 7
			A,I	**ACOMP7**: ACOMP channel 7
			I/O	**Secure GPIO mode**: SPIO0[17]
10	GPIO50	Input	I/O	**GPIO mode**: General-purpose I/O 50
			I	**FREQME_GPIO_CLK**: Frequency measure pin clock input
			I	**ADC_DAC_TRIGGER0**: Bit 2 of ADC/DAC external trigger
			I/O	**Secure GPIO mode**: SPIO0[18]
11	GPIO55	Input	I/O	**GPIO mode**: General-purpose I/O 55
			O	**SCT0_OUT9**: SCTimer 0/PWM output 9

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Table 2. Pin lists*...continued*

Pin no	Pin name	Reset state	Pin type	Description
			I	**ADC_DAC_TRIGGER1**: Bit 3 of ADC/DAC external trigger
			I/O	**Secure GPIO mode**: SPIO0[18]
12	GPIO12	Input	I/O	**GPIO mode**: General-purpose I/O 12
				USB_DRV_VBUS: enables + 5 V voltage supply to USB OTG
				CT0_MAT2: CTIMER 0 match output 2
				CT_INP2: Pin input 2 to CTIMER
				SD_HOST_INT: SD host interrupt output signal
13	GPIO15	Input	I/O	**GPIO mode**: General-purpose I/O 15
			I	**SDIO mode**: SD_CLK SDIO clock input
			I	**UTICK_CAP0**: Micro-tick timer capture input 0
			O	**UCLK**: USIM clock
			I/O	**FC2_SCK_USART**: Flexcomm 2 USART clock
			I/O	**FC2_SCK_I2S**: Flexcomm 2 I^2S clock
			I/O	**FC2_SCK_SPI**: Flexcomm 2 SPI clock
14	GPIO18	Input	I/O	**GPIO mode**: General-purpose I/O 18
			I/O	**SDIO mode**: SDIO_DAT2 SDIO data input/output2
			I	**UTICK_CAP3**: Micro-tick timer capture input 3
			O	**UVS**: USIM mode selection
			O	**GPIO_INT_BMAT**: The output of the interrupt pattern matches the engine
15	GND	-	PWR	Ground
16	GPIO16	Input	I/O	**GPIO mode**: General-purpose I/O 16
			I/O	**SDIO mode**: (SD_D3) SDIO_DAT3 SDIO data input/output 3
			I	**UTICK_CAP1**: Micro-tick timer capture input 1
			O	**URST**: USIM reset signal
			I	**FC2_CTS_SDA_SSELN0_USART**: Flexcomm 2 USART clear-to-send
			I/O	**FC2_CTS_SDA_SSELN0_SPI**: Flexcomm 2 SPI chip select
			I/O	**FC2_CTS_SDA_SSELN0_I2C_COPY**: (I2C_SDA) Flexcomm 2 backup-I^2C data in/out
17	GPIO6	Input	I/O	**GPIO mode**: General-purpose I/O 6
			I	**JTAG_TCK**: JTAG test clock input signal
			I	**FC1_CTS_SDA_SSELN0_USART**: Flexcomm 1 USART clear-to-send
			I/O	**FC1_CTS_SDA_SSELN0_SPI**: Flexcomm1 SPI chip select
			I/O	**FC1_CTS_SDA_SSELN0_I2C_COPY**: (I2C_SDA) Flexcomm 1 backup-I2C data in/out
18	GPIO7	Input	I/O	**GPIO mode**: General-purpose I/O 7

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Table 2. Pin lists*...continued*

Pin no	Pin name	Reset state	Pin type	Description
			I	**JTAG_TMS**:JTAG test mode select input signal
			I	**FC1_SCK_USART**: Flexcomm 1 USART clock
			I/O	**FC1_SCK_I2S**: Flexcomm 1 I^2S clock
			I/O	**FC1_SCK_SPI:** Flexcomm 1 SPI clock
19	GPIO8	Input	I/O	**GPIO mode**: General-purpose I/O 8
			I	**JTAG_TDI**: JTAG test data input signal
			O	**FC1_TXD_SCL_MISO_WS_USART**: Flexcomm 1 USART transmitter
			I/O	**FC1_TXD_SCL_MISO_WS_I2C**: Flexcomm 1 I^2C clock
			I/O	**FC1_TXD_SCL_MISO_WS_I2S**: Flexcomm 1 I^2S word select
			I/O	**FC1_TXD_SCL_MISO_WS_SPI**: Flexcomm 1 SPI controller in/ target out
20	GPIO9	Input	I/O	**GPIO mode**: General-purpose I/O 9
			O	**JTAG_TDO**: JTAG test data output signal
			I	**FC1_RXD_SDA_MOSI_DATA_USART**: Flexcomm 1 USART receiver
			I/O	**FC1_RXD_SDA_MOSI_DATA_I2C**: Flexcomm 1 I^2C data in/ out
			I/O	**FC1_RXD_SDA_MOSI_DATA_I2S**: Flexcomm 1 I^2S receiver/ transmitter
			I/O	**FC1_RXD_SDA_MOSI_DATA_SPI**: Flexcomm 1 SPI controller out/target in
21	GPIO10	Input	I/O	**GPIO mode**: General-purpose I/O 10
			I	**JTAG_TRSTN**: JTAG test reset signal
			O	**FC1_RTS_SCL_SSELN1_USART**: Flexcomm 1 USART request-to-send
			I/O	**FC1_RTS_SCL_SSELN1_I2C_COPY**: (I2C_SCL) Flexcomm 1 backup-I2C clock
22	GPIO25	Input	I/O	**GPIO mode**: General-purpose I/O 25
			I	**AON_WAKEUP**: Always on out-of-band wake up input signal
			O	**CT1_MAT3**: 32-bit CTIMER 1 match output 3
			I	**CT_INP7**: Pin input 7 to CTIMER
			I/O	**FC3_SCK_USART**: Flexcomm 3 USART clock
			I/O	**FC3_SCK_I2S**: Flexcomm 3 I^2S clock
			I/O	**FC3_SCK_SPI**: Flexcomm 3 SPI clock
23	GPIO17	Input	I/O	**GPIO mode**: General-purpose I/O 17
			I/O	**SDIO mode**: SDIO_CMD SDIO command line
			I	**UTICK_CAP2**: Micro-tick timer capture input 2
			I/O	**UIO**: USIM transmit receive signal

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Table 2. Pin lists*...continued*

Pin no	Pin name	Reset state	Pin type	Description
			O	**FC2_RTS_SCL_SSELN1_USART**: Flexcomm 2 USART request-to-send
			I/O	**FC2_RTS_SCL_SSELN1_I2C_COPY** (I2C_SCL) Flexcomm 2 backup-I^{2}C clock
24	GPIO19	Input	I/O	**GPIO mode**: General-purpose I/O 19
			I/O	**SDIO mode**: SDIO_DAT0 SDIO data input/output 0
			O	**FC3_RTS_SCL_SSELN1_USART**: Flexcomm 3 USART request-to-send
			I/O	**FC3_RTS_SCL_SSELN1_I2C_COPY**: (I2C_SCL) Flexcomm 3 backup-I^{2}C clock
25	NC	-	-	-
26	GPIO20	Input	I/O	**GPIO mode**: General-purpose I/O 20
			I/O	**SDIO mode**: SDIO_DAT1 SDIO data input/output 1
			I	**FC3_CTS_SDA_SSELN0_USART**: Flexcomm 3 USART clear-to-send
			I/O	**FC3_CTS_SDA_SSELN0_SPI**: Flexcomm 3 SPI chip select
			I/O	**FC3_CTS_SDA_SSELN0_I2C_COPY**: (I2C_SDA) Flexcomm 3 backup-I^{2}C data in/out
27	GPIO13	Input	I/O	**GPIO mode**: General-purpose I/O 13
			I	**CT_INP3**: Pin input 3 to CTIMER
			O	**CT0_MAT3**: CTIMER 0 match output 3
			I	**SWCLK**: Serial wire clock input signal
			I	**FC2_RXD_SDA_MOSI_DATA_USART**: Flexcomm 2 USART receiver
			I/O	**FC2_RXD_SDA_MOSI_DATA_I2C**: Flexcomm 2 I^{2}C data in/out
			I/O	**FC2_RXD_SDA_MOSI_DATA_I2S**: Flexcomm 2 I^{2}S receiver/transmitter
			I/O	**FC2_RXD_SDA_MOSI_DATA_SPI**: Flexcomm 2 SPI controller out/target in
28	GPIO14	Input	I/O	**GPIO mode**: General-purpose I/O 14
			I	**CT_INP4**: Pin input 4 to CTIMER
			O	**CT1_MAT0**: CTIMER 1 match output 0
			I/O	**SWDIO**: Serial wire debug data input/output signal
			O	**FC2_TXD_SCL_MISO_WS_USART**: Flexcomm 2 USART transmitter
			I/O	**FC2_TXD_SCL_MISO_WS_I2C**: Flexcomm 2 I^{2}C clock
			I/O	**FC2_TXD_SCL_MISO_WS_I2S**: Flexcomm 2 I^{2}S word select
			I/O	**FC2_TXD_SCL_MISO_WS_SPI**: Flexcomm 2 SPI controller in/target out

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Table 2. Pin lists*...continued*

Pin no	Pin name	Reset state	Pin type	Description
29	GPIO0	Input	I/O	**GPIO mode**: General-purpose I/O 0
			I	**CT_INP0**: Pin input 0 to CTIMER
			O	**CT0_MAT0**: CTIMER 0 match output 0
			I	**FC0_CTS_SDA_SSELN0_USART**: Flexcomm 0 USART clear-to-send
			I/O	**FC0_CTS_SDA_SSELN0_SPI**: Flexcomm 0 SPI chip select
			I/O	**FC0_CTS_SDA_SSELN0_I2C_COPY**: (I2C_SDA) Flexcomm 0 backup-I2C data in/out
30	GPIO4	Input	I/O	**GPIO mode**: General-purpose I/O 4
			I	**Coexistence mode**: Ext_STATE/WCI-2_SIN
			O	**SCT0_OUT1**: SCTimer 0/PWM output 1
			I	**SCT0_PIN_INP1**: Input pin 1 to SCTimer 0/PWM
			I	**CLKIN_FRM_PD**: Clock from pad, which can replace the internal clock for debug purpose
			I/O	**FC0_SCK_USART**: Flexcomm 0 USART clock
			I/O	**FC0_SCK_I2S**: Flexcomm 0 I^2S clock
			I/O	**FC0_SCK_SPI**: Flexcomm 0 SPI clock
31	GPIO3	Input	I/O	**GPIO mode**: General-purpose I/O 3
			O	**SCT0_OUT0**: SCTimer 0/PWM output 0
			I	**SCT0_PIN_INP0**: Input pin 0 to SCTimer 0/PWM
			O	**FC0_TXD_SCL_MISO_WS_USART**: Flexcomm 0 USART transmitter
			I/O	**FC0_TXD_SCL_MISO_WS_I2C**: Flexcomm 0 I^2C clock
			I/O	**FC0_TXD_SCL_MISO_WS_I2S**: Flexcomm 0 I^2S word select
			I/O	**FC0_TXD_SCL_MISO_WS_SPI**: Flexcomm 0 SPI controller in/target out
32	BOOTSEL_EXT_REQ	-	I/O	Boot selection
				PTA coexistence interface: Request from external radio (mandatory)
33	GPIO5	Input	I/O	**GPIO mode**: General- purpose I/O 5
			I/O	**MCLK**: MCLK input or output for I^2S and/or digital microphone
			O	**FC0_RTS_SCL_SSELN1_USART**: Flexcomm 0 USART request-to-send
			I/O	**FC0_RTS_SCL_SSELN1_I2C_COPY**:(I2C_SCL) Flexcomm 0 backup-I2C clock
34	GPIO24	Input	I/O	**GPIO mode**: General-purpose I/O 24
			I	**AON_WAKEUP**: Always on out-of-band wakeup input signal
			O	**CT1_MAT2**: 32-bit CTIMER 1 match output 2
			I	**CT_INP6**: Pin input 6 to CTIMER

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Table 2. Pin lists*...continued*

Pin no	Pin name	Reset state	Pin type	Description
			I	**FC3_RXD_SDA_MOSI_DATA_USART**: Flexcomm 3 USART receiver
			I/O	**FC3_RXD_SDA_MOSI_DATA_I2C**: Flexcomm 3 I^2C data in/out
			I/O	**FC3_RXD_SDA_MOSI_DATA_I2S**: Flexcomm 3 I^2S receiver/transmitter
			I/O	**FC3_RXD_SDA_MOSI_DATA_SPI**: Flexcomm 3 SPI controller out/target in
35	GPIO26	Output	I/O	**GPIO mode**: General-purpose I/O 26
			I	**AON_CAPT**: Capture timer input signal
			O	**SCT0_OUT4**: SCTimer 0/PWM output 4
			I	**SCT0_PIN_INP4**: Pin input 4 to SCTimer 0/PWM
			O	**FC3_TXD_SCL_MISO_WS_USART**: Flexcomm 3 USART transmitter
			I/O	**FC3_TXD_SCL_MISO_WS_I2C**: Flexcomm 3 I^2C clock
			I/O	**FC3_TXD_SCL_MISO_WS_I2S**: Flexcomm 3 I^2S word select
			I/O	**FC3_TXD_SCL_MISO_WS_SPI**: Flexcomm 3 SPI controller in/target out
36	GPIO43	Input	I/O	**GPIO mode**: General-purpose I/O 43
			A,I	**ADC0_1**: ADC0 channel 1
			A,I	**ACOMP1**: ACOMP channel 1
			A,O	**DAC_B**: DAC channel B
			I/O	**Secure GPIO mode**: SPIO0[11]
37	GPIO2	Input	I/O	**GPIO mode**: General-purpose I/O 2
			I	**FC0_RXD_SDA_MOSI_DATA_USART**: Flexcomm0 USART receiver
			I/O	**FC0_RXD_SDA_MOSI_DATA_I2C**: Flexcomm 0 I^2C data in/out
			I/O	**FC0_RXD_SDA_MOSI_DATA_I2S**: Flexcomm 0 I^2S receiver/transmitter
			I/O	**FC0_RXD_SDA_MOSI_DATA_SPI**: Flexcomm 0 SPI controller out/target in
38	GND	-	PWR	Ground
39	USB_VBUS	-	A, I/O	VBUS selection, 5 V analog power supply
40	EXT_GNT	Input	I/O	**PTA coexistence interface:** External radio grant output signal (mandatory)
41	GPIO27	Input	I/O	**GPIO mode**: General-purpose I/O 27
			O	**AON_OUT**: Always-on GPIO output signal
			O	**SCT0_OUT5**: SCTimer 0/PWM output 5
			I	**SCT0_PIN_INP5**: Pin input 5 to SCTimer 0/PWM

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Table 2. Pin lists*...continued*

Pin no	Pin name	Reset state	Pin type	Description
42	EXT_FREQ	Input	O	**WCI-2 coexistence interface**: Output signal to external radio
			I	**PTA coexistence interface**: External radio frequency input signal (optional)
43	EXT_PRI	Input	I	**PTA coexistence interface**: External radio input priority signal (optional)
44	GND	-	PWR	Ground
45	GPIO52	Input	I/O	**GPIO mode**: General- purpose I/O 52
			I	**PDM_DATA23**: PDM data input for DMIC channels 2 and 3
			O	**CT3_MAT0**: CTIMER 3 match output 0
			I	**CT_INP12**: Pin input 12 to CTIMER
			O	**ACOMP0_EDGE_PULSE**: Analog comparator 0 edge pulse
			I/O	**Secure GPIO mode**: SPIO0[20]
46	GPIO1	Input	I/O	**GPIO mode**: General-purpose I/O 1
			I	**CT_INP1**: Pin input 1 to CTIMER
			O	**CT0_MAT1**: CTIMER 0 match output 1
47	GPIO11	Input	I/O	**GPIO mode**: General-purpose I/O 11
			O	**SCT0_OUT8**: SCTimer 0/PWM output 8
48	GND	-	PWR	Ground
49	GPIO21	Input	I/O	**GPIO mode**: General-purpose I/O 21
			O	**CT1_MAT1**: CTIMER 1 match output 1
			I	**CT_INP5**: Pin input 5 to CTIMER
50	GPIO53	Input	I/O	**GPIO mode**: General-purpose I/O 53
			O	**PDM_CLK01**: PDM clock output for DMIC channels 0 and 1
			O	**CT3_MAT1**: CTIMER 3 match output 1
			I	**CT_INP13**: Pin input 13 to CTIMER
			O	**ACOMP1_GPIO_OUT**: Analog comparator 1 level output
			I/O	**Secure GPIO mode**: SPIO0[21]
51	GPIO51	Input	I/O	**GPIO mode**: General-purpose I/O 51
			I	**PDM_DATA01**: PDM data input for DMIC channels 0 and 1
			O	**CT2_MAT3**: CTIMER 2 match output 3
			I	**CT_INP11**: Pin input 11 to CTIMER
			O	**ACOMP0_GPIO_OUT**: Analog comparator 0 level output
			I/O	**Secure GPIO mode**: SPIO0[19]
52	GPIO54	Input	I/O	**GPIO mode**: General-purpose I/O 54
			O	**ACOMP1_EDGE_PULSE**: Analog comparator 1 edge pulse
			O	**PDM_CLK23**: PDM clock output for DMIC channels 2 and 3
			O	**CT3_MAT2**: CTIMER 3 match output 2

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Table 2. Pin lists*...continued*

Pin no	Pin name	Reset state	Pin type	Description
			I	**CT_INP14**: Pin input 14 to CTIMER
			I/O	**Secure GPIO mode**: SPIO0[22]
53	JTAG_SWD	Input	I/O	Configuration pin
54	GND	-	PWR	Ground
55	GPIO22	Input	I/O	**GPIO mode**: General-purpose I/O 22
			A,I	**AON_XTAL32K_IN**: Always-on 32K crystal input signal
			I	**SLP_CLK_32K**: External sleep clock input signal
			I	**SCT0_PIN_INP2**: Pin input 2 to SCTimer 0/PWM
			I	**ENET_RX_DATA0:** ipp_ind_mac0_rxdata0 (I)
56	GND	-	PWR	Ground
57	GND	-	PWR	Ground
58	USB_ID	Input	A, I	USB OTG ID pin
59	GPIO42	Input	I/O	**GPIO mode**: General-purpose I/O 42
			A,I	**ADC0_0**: ADC0 channel 0
			A,I	**ACOMP0**: ACOMP channel 0
			I/O	**Secure GPIO mode**: SPIO0[10]
60	GND	-	PWR	Ground
61	USB_DP	Tristate	A, I/O	USB bus data+
62	USB_DM	Tristate	A, I/O	USB bus data-
63	GND	-	PWR	Ground
64	NC	-	-	-
65	GND	-	PWR	Ground
66	GND	-	PWR	Ground
67	GND	-	PWR	Ground
68	GND	-	PWR	Ground
69	GND	-	PWR	Ground
70	GND	-	PWR	Ground
71	GND	-	PWR	Ground
72	GND	-	PWR	Ground
73	GND	-	PWR	Ground

7 Application interfaces

This section describes the application-facing interfaces and configuration options supported by the module.

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7.1 Boot mode

RW610FML boots from the internal flash memory by default. Pull the BOOTSEL_EXT_REQ pin low and reset the module. RW610FML enters the ISP boot mode, allowing the internal flash to be reprogrammed via UART, I²C, SPI, or USB interfaces.

Table 3. Boot configuration options

Pin name	Configuration function
BOOTSEL_EXT_REQ	1= Boot from FlexSPI Flash (default) 0= ISP boot (UART/I^{2}C/SPI/USB)

7.2 JTAG/SWD configuration

RW610FML supports JTAG or SWD debug interfaces. The JTAG_SWD pin is used as a configuration input to select the active debug interface. Table 4 shows the debug interface configuration options.

Table 4. Debug interface configuration

Pin name	Configuration function
JTAG_SWD	1= JTAG 0= SWD

To configure the selection bit to logic 0, connect a pulldown resistor of 51 kΩ or less from the JTAG_SWD pin to GND. To configure the selection bit to logic 1, no external circuitry is required; the pin is internally pulled up by default.

7.3 GPIO multiplexing

The RW610FML GPIO pins support multiple alternate functions, as shown in Table 5.

Table 5. Pin multiplexing of the GPIOs

Pin no	Pin name	Alternate 0	Alternate 1	Alternate 2	Alternate 3	Alternate 4	Alternate 5	Alternate 6	Alternate 7
29	GPIO0	GPIO[0]	UART0_ CTS	-	-	SPI0_CS	-	-	-
46	GPIO1	GPIO[1]	-	-	-	-	-	-	-
37	GPIO2	GPIO[2]	UART0_ RXD	I2C0_SDA	I2S0_SDA	SPI0_MOSI	PCM_ DOUT/DIN	-	-
31	GPIO3	GPIO[3]	UART0_ TXD	I2C0_SCL	I2S0_WS	SPI0_MISO	PCM_ SYNC	PWM0	-
30	GPIO4	GPIO[4]	UART0_ SCK	EXT_ STATE	I2S0_SCK	SPI0_SCK	PCM_CLK	PWM1	WCI-2_ SIN
33	GPIO5	GPIO[5]	UART0_ RTS	-	-	-	MCLK	-	-
17	GPIO6	GPIO[6]	UART1_ CTS	-	-	SPI1_CS	-	-	-
18	GPIO7	GPIO[7]	UART1_ SCK	-	I2S1_SCK	SPI1_SCK	PCM_CLK	-	-
19	GPIO8	GPIO[8]	UART1_ TXD	I2C1_SCL	I2S1_WS	SPI1_MISO	PCM_ SYNC	-	-

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Table 5. Pin multiplexing of the GPIOs*...continued*

Pin no	Pin name	Alternate 0	Alternate 1	Alternate 2	Alternate 3	Alternate 4	Alternate 5	Alternate 6	Alternate 7
20	GPIO9	GPIO[9]	UART1_ RXD	I2C1_SDA	I2S1_SDA	SPI1_MOSI	PCM_ DOUT/DIN	-	-
21	GPIO10	GPIO[10]	UART1_ RTS	JTAG_ TRST	-	-	-	-	-
47	GPIO11	GPIO[11]	-	-	-	-	-	PWM8	-
12	GPIO12	GPIO[12]	-	-	-	-	-	-	-
27	GPIO13	GPIO[13]	UART2_ RXD	I2C2_SDA	I2S2_SDA	SPI2_MOSI	PCM_ DOUT/DIN	SWCLK	-
28	GPIO14	GPIO[14]	UART2_ TXD	I2C2_SCL	I2S2_WS	SPI2_MISO	PCM_ SYNC	SWDIO	-
13	GPIO15	GPIO[15]	UART2_ SCK	-	I2S2_SCK	SPI2_SCK	PCM_CLK	UCLK	UTICK_ CAP0
16	GPIO16	GPIO[16]	UART2_ CTS	I2C2_ COPY_SDA	-	SPI2_CS	-	URST	UTICK_ CAP1
23	GPIO17	GPIO[17]	UART2_ RTS	I2C2_ COPY_SCL	-	-	-	UIO	UTICK_ CAP2
14	GPIO18	GPIO[18]	-	-	-	-	-	-	UTICK_ CAP3
24	GPIO19	GPIO[19]	UART3_ RTS	I2C3_ COPY_SCL			-		
26	GPIO20	GPIO[20]	UART3_ CTS	I2C3_ COPY_SDA	-	SPI3_CS	-	-	-
49	GPIO21	GPIO[21]	-	-	-	-	-	-	-
55	GPIO22	GPIO[22]	SLP_CLK_ 32K	-	-	-	-	-	-
34	GPIO24	GPIO[24]	UART3_ RXD	-	I2S3_SDA	SPI3_MOSI	PCM_ DOUT/DIN	-	-
22	GPIO25	GPIO[25]	UART3_ SCK	-	I2S3_SCK	SPI3_SCK	PCM_CLK	-	-
35	GPIO26	GPIO[26]	UART3_ TXD	-	I2S3_WS	SPI3_MISO	PCM_ SYNC	PWM4	-
41	GPIO27	GPIO[27]	-	-	-	-	-	PWM5	-
59	GPIO42	GPIO[42]	-	-	ADC0_0	ACOMP0	-	-	-
36	GPIO43	GPIO[43]	-	DAC_B	ADC0_1	ACOMP1	-	-	-
4	GPIO44	GPIO[44]	LCD_ RESETN	DAC_A	ADC0_2	ACOMP2	-	-	-
5	GPIO45	GPIO[45]	LCD_TE	EXT_ VREF_DAC	ADC0_3	ACOMP3	-	-	-
6	GPIO46	GPIO[46]	LCD_SPI_ DATA	-	ADC0_4	ACOMP4	-	-	-
7	GPIO47	GPIO[47]	LCD_SPI_ DC	-	ADC0_5	ACOMP5	-	-	-

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Table 5. Pin multiplexing of the GPIOs*...continued*

Pin no	Pin name	Alternate 0	Alternate 1	Alternate 2	Alternate 3	Alternate 4	Alternate 5	Alternate 6	Alternate 7
8	GPIO48	GPIO[48]	LCD_SPI_SCK	-	ADC0_6	ACOMP6	ADC1_6	-	-
9	GPIO49	GPIO[49]	LCD_SPI_SS	-	ADC0_7	ACOMP7	ADC1_7	-	-
10	GPIO50	GPIO[50]	-	DAC_TRIGGER0	-	-	-	-	-
51	GPIO51	GPIO[51]	PDM_DATA01	-	-	ACOMP0_GPIO_OUT	-	-	-
45	GPIO52	GPIO[52]	PDM_DATA23	-	-	ACOMP0_EDGE_PULSE	-	-	-
50	GPIO53	GPIO[53]	PDM_CLK01	-	-	ACOMP1_GPIO_OUT	-	-	-
52	GPIO54	GPIO[54]	PDM_CLK23	-	-	ACOMP1_EDGE_PULSE	-	-	-
11	GPIO55	GPIO[55]	-	DAC_TRIGGER1	-	-	-	PWM9	-

Note: *For more details, refer to the RW610 data sheet.*

7.4 Interface definition

The following subsections define the electrical interfaces available for system integration and peripheral connectivity.

7.4.1 SDIO interface

RW610FML has one SDIO device interface, which complies with the SDIO 3.0 specification. The interface supports Peripheral mode with maximum clock rate of up to 208 MHz, 1-bit (by default), and 4-bit data bus modes.

Table 6. SDIO interface

Pin no	Pin definition	I/O	Description
24	SDIO_DATA0	I/O	SDIO data input/output 0
26	SDIO_DATA1	I/O	SDIO data input/output 1
14	SDIO_DATA2	I/O	SDIO data input/output 2
16	SDIO_DATA3	I/O	SDIO data input/output 3
13	SDIO_CLK	I	SDIO clock input
23	SDIO_CMD	I/O	SDIO command line

To ensure reliable communication performance, the following design guidelines must be considered when designing the SDIO interface:

- To suppress bus jitter and ensure signal integrity, external pull-up resistors with resistance values ranging from 10 kΩ to 100 kΩ (recommended value: 10 kΩ) must be reserved on SDIO_CMD, SDIO_DATA[0:3], and SDIO_CLK signal lines. These pull-up resistors must be connected to RW610FML VIN supply.

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- SDIO signal traces must preferably be routed on inner PCB layers; surrounded by ground on the same layer, and continuous ground planes on the adjacent upper and lower layers. The characteristic impedance of SDIO signal traces must be 50 Ω ± 10 %. The SDIO_CLK signal trace must be routed separately and surrounded by ground to minimize coupling and noise.
- SDIO signal traces must be routed away from power supply traces, crystal oscillators, magnetic components, and RF signals. SDIO signal traces must also be routed away from analog signals and noise sources, such as system clocks and DC-DC converters.
- The SDIO_CLK, SDIO_DATA[0:3], and SDIO_CMD signal traces must be matched in length, with a trace-to-trace spacing of less than 2.54 mm. Whenever possible, route these signals on the same PCB layer, keeping them parallel. Ensure that sufficient ground vias are placed near the SDIO traces and connected to a solid ground plane.
- The total trace length inside RW610FML is 16.16 mm. Based on the SDIO transmission mode, the recommended external PCB trace length is as follows:
  - SDR104 mode: The total trace length must be less than 50 mm.
  - Other modes (such as DDR50 and SDR50): The total trace length must be less than 150 mm.
  - The clearance between adjacent traces must be at least twice the trace width. The total load capacitance of the SDIO bus must be less than 15 pF.

7.4.2 UART interface

RW610FML provides up to four UART interfaces.

Table 7. UART interfaces

Pin no	Pin definition	I/O	Description
31	UART0_TXD	O	UART0 transmit output signal (Flexcomm 0)
37	UART0_RXD	I	UART0 receive input signal (Flexcomm 0)
19	UART1_TXD	O	UART1 transmit output signal (Flexcomm 1)
20	UART1_RXD	I	UART1 receive input signal (Flexcomm 1)
28	UART2_TXD	O	UART2 transmit output signal (Flexcomm 2)
27	UART2_RXD	I	UART2 receive input signal (Flexcomm 2)
35	UART3_TXD	O	UART3 transmit output signal (Flexcomm 3)
34	UART3_RXD	I	UART3 receive input signal (Flexcomm 3)

7.4.3 SPI interface

RW610FML provides up to four SPI interfaces. Each SPI interface can operate as either a controller or a peripheral, with a maximum clock frequency of up to 30 MHz.

Table 8. SPI interface

Pin no	Pin definition	I/O	Description
29	FC0_SPI_CS	I/O	SPI chip select (Flexcomm 0)
30	FC0_SPI_SCK	I/O	SPI clock (Flexcomm 0)
31	FC0_SPI_MISO	I/O	SPI controller-in peripheral-out (Flexcomm 0)
37	FC0_SPI_MOSI	I/O	SPI controller-out peripheral-in (Flexcomm 0)
17	FC1_SPI_CS	I/O	SPI chip select (Flexcomm 1)
18	FC1_SPI_SCK	I/O	SPI clock (Flexcomm 1)

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Table 8. SPI interface...*continued*

Pin no	Pin definition	I/O	Description
19	FC1_SPI_MISO	I/O	SPI controller-in peripheral-out (Flexcomm 1)
20	FC1_SPI_MOSI	I/O	SPI controller-out peripheral-in (Flexcomm 1)
16	FC2_SPI_CS	I/O	SPI chip select (Flexcomm 2)
13	FC2_SPI_SCK	I/O	SPI clock (Flexcomm 2)
27	FC2_SPI_MISO	I/O	SPI controller-in peripheral-out (Flexcomm 2)
28	FC2_SPI_MOSI	I/O	SPI controller-out peripheral-in (Flexcomm 2)
26	FC3_SPI_CS	I/O	SPI chip select (Flexcomm 3)
22	FC3_SPI_SCK	I/O	SPI clock (Flexcomm 3)
34	FC3_SPI_MISO	I/O	SPI controller-in peripheral-out (Flexcomm 3)
35	FC3_SPI_MOSI	I/O	SPI controller-out peripheral-in (Flexcomm 3)

7.4.4 PCM interface

The PCM function is implemented through two I^2S plus MCLK combinations:

- One I^2S is set to PCM_DOUT
- The other I^2S is set to the peripheral PCM_DIN

The timing specification follows the I^2S bus interface specification.

Table 9. PCM interface

Pin no	Pin name	I/O	Description
18	GPIO7	I/O	PCM clock
19	GPIO8	I/O	PCM data frame sync
20	GPIO9	I/O	PCM data output/input
30	GPIO4	I/O	PCM clock
31	GPIO3	I/O	PCM data frame sync
37	GPIO2	I/O	PCM data output/input
13	GPIO15	I/O	PCM clock
28	GPIO14	I/O	PCM data frame sync
27	GPIO13	I/O	PCM data output/input
22	GPIO25	I/O	PCM clock
35	GPIO26	I/O	PCM data frame sync
34	GPIO24	I/O	PCM data output/input
33	GPIO5	I/O	Controller clock output for codec

Figure 3 shows an example connection to a bidirectional PCM codec where the module's PCM_SYNC serves as a central.

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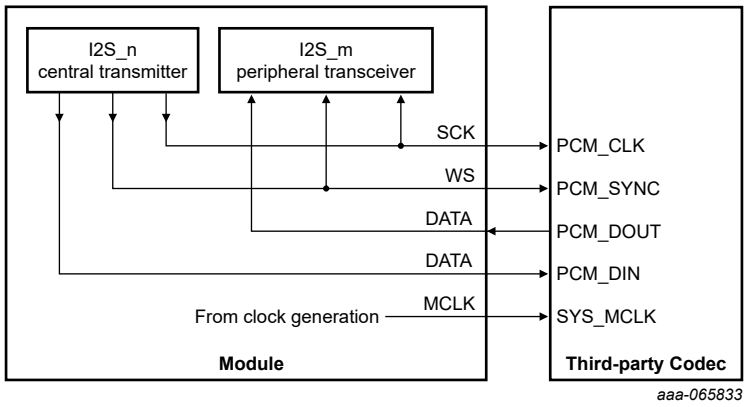


Figure 3. PCM_SYNC serving as central

Figure 4 shows the example connection to a bidirectional PCM codec where the module's PCM_SYNC serves as a peripheral.

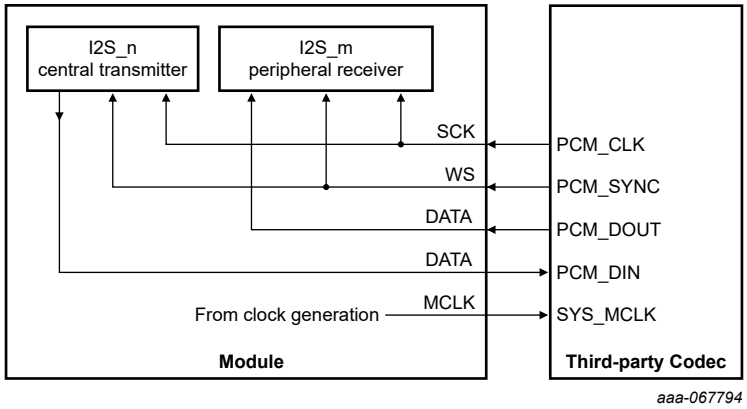


Figure 4. PCM_SYNC serving as peripheral

7.4.5 I²C interface

RW610FML provides up to four I²C interfaces that support both controller and peripheral modes.

Table 10. I²C interface

Pin no	Pin definition	I/O	Description
31	FC0_I2C_CLK	I/O	I2C0 serial clock (Flexcomm 0)
37	FC0_I2C_SDA	I/O	I2C0 serial data (Flexcomm 0)
29	FC0_I2C_SDA_COPY	I/O	Backup-I2C0 serial data (Flexcomm 0)
33	FC0_I2C_CLK_COPY	I/O	Backup-I2C0 serial clock (Flexcomm 0)
19	FC1_I2C_CLK	I/O	I2C1 serial clock (Flexcomm 1)
20	FC1_I2C_SDA	I/O	I2C1 serial data (Flexcomm 1)
17	FC1_I2C_SDA_COPY	I/O	Backup-I2C1 serial data (Flexcomm 1)
21	FC1_I2C_CLK_COPY	I/O	Backup-I2C1 serial clock (Flexcomm 1)
28	FC2_I2C_CLK	I/O	I2C2 serial clock (Flexcomm 2)
27	FC2_I2C_SDA	I/O	I2C2 serial data (Flexcomm 2)

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Table 10. I²C interface...*continued*

Pin no	Pin definition	I/O	Description
23	FC2_I2C_CLK_COPY	I/O	Backup-I2C2 serial clock (Flexcomm 2)
16	FC2_I2C_SDA_COPY	I/O	Backup-I2C2 serial data (Flexcomm 2)
35	FC3_I2C_CLK	I/O	I2C3 serial clock (Flexcomm 3)
34	FC3_I2C_SDA	I/O	I2C3 serial data (Flexcomm 3)
24	FC3_I2C_CLK_COPY	I/O	Backup-I2C3 serial clock (Flexcomm 3)
26	FC3_I2C_SDA_COPY	I/O	Backup-I2C3 serial data (Flexcomm 3)

7.4.6 I²S interface

RW610FML provides up to four I²S interfaces, which support both controller and peripheral modes with sampling rates from 8 kHz to 384 kHz.

Table 11. I²S interface

Pin no	Pin definition	I/O	Description
30	FC0_I2S_SCK	I/O	I2S0 clock (Flexcomm 0)
31	FC0_I2S_WS	I/O	I2S0 word select (Flexcomm 0)
37	FC0_I2S_SDA	I/O	I2S0 receiver/transmitter (Flexcomm 0)
18	FC1_I2S_SCK	I/O	I2S1 clock (Flexcomm 1)
19	FC1_I2S_WS	I/O	I2S1 word select (Flexcomm 1)
20	FC1_I2S_SDA	I/O	I2S1 receiver/transmitter (Flexcomm 1)
13	FC2_I2S_SCK	I/O	I2S2 clock (Flexcomm 2)
28	FC2_I2S_WS	I/O	I2S2 word select (Flexcomm 2)
27	FC2_I2S_SDA	I/O	I2S2 receiver/transmitter (Flexcomm 2)
22	FC3_I2S_SCK	I/O	I2S3 clock (Flexcomm 3)
35	FC3_I2S_WS	I/O	I2S3 word select (Flexcomm 3)
34	FC3_I2S_SDA	I/O	I2S3 receiver/transmitter (Flexcomm 3)

7.4.7 PWM interface

RW610FML provides up to six PWM channels.

Table 12. PWM interface

Pin no	Pin definition	I/O	Description
31	SCT0_OUT0	O	PWM0
30	SCT0_OUT1	O	PWM1
35	SCT0_OUT4	O	PWM4
41	SCT0_OUT5	O	PWM5
47	SCT0_OUT8	O	PWM8
11	SCT0_OUT9	O	PWM9

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7.4.8 ADC channel

RW610FML provides up to eight 16-bit ADC channels with an internal reference voltage of 1.2 V.

Table 13. ADC channel

Pin no	Pin definition	I/O	Description
59	ADC0_0	A, I	ADC0 channel 0
36	ADC0_1	A, I	ADC0 channel 1
4	ADC0_2	A, I	ADC0 channel 2
5	ADC0_3	A, I	ADC0 channel 3
6	ADC0_4	A, I	ADC0 channel 4
7	ADC0_5	A, I	ADC0 channel 5
8	ADC0_6/ADC1_6	A, I	ADC0 Channel 6/ADC1 Channel 6
9	ADC0_7/ADC1_7	A, I	ADC0 Channel 7/ADC1 Channel 7

7.4.9 DAC

RW610FML integrates a 10-bit DAC peripheral with two output channels. Each channel can be configured for single-ended output, or both channels can be combined to generate a differential output signal.

Table 14. DAC

Pin no	Pin definition	I/O	Description
36	DAC_B	A, O	DAC channel B
4	DAC_A	A, O	DAC channel A
5	EXT_VREF_ADC0_DAC	A, I	DAC external voltage reference input
10	ADC_DAC_TRIGGER0	I	Bit 2 of DAC external trigger
11	ADC_DAC_TRIGGER1	I	Bit 3 of DAC external trigger

7.4.10 USB interface

RW610FML provides one integrated Universal Serial Bus (USB) interface that operates as a host or device and complies with the USB 2.0 specification. It supports high-speed (480 Mbit/s) mode and is backward-compatible with full-speed (12 Mbit/s) mode.

Table 15. USB interface

Pin no	Pin definition	I/O	Description
61	USB_DP	A, I/O	USB 2.0 differential data (+)
62	USB_DM	A, I/O	USB 2.0 differential data (-)
39	USB_VBUS	A, I/O	VBUS selection
58	USB_ID	A, I	USB ID detect

Figure 5 shows the USB interface connection.

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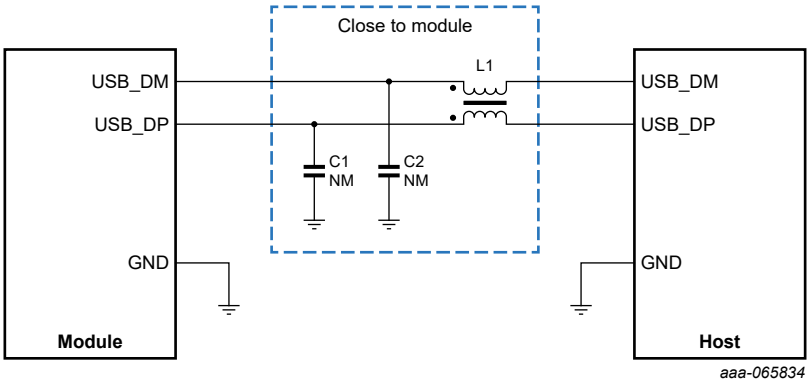


Figure 5. USB interface connection

When designing the USB interface, follow the guidelines below to ensure compliance with the USB 2.0 specification:

- Route USB signal traces (USB_DP and USB_DM) as differential pairs with ground reference on the same layer, and continuous ground planes on the adjacent upper and lower layers. The differential characteristic impedance of the USB 2.0 interface must be 90 Ω ± 10 %.
- Do not route USB signal traces through crystals, oscillators, magnetic components, sensitive circuits, and signals, such as RF circuits and analog signals. Also, do not route USB signal traces near noise sources including system clocks and DC-DC converters.
- If no internal pull-down resistors are integrated on the host side, place external 15 kΩ pull-down resistors on USB_DP and USB_DM. Connect both resistors to the ground and locate the resistors close to the host.

7.4.11 JTAG interface

RW610FML provides a JTAG interface for downloading and debugging. Keep JTAG_SWD at a high level. The downloading and debugging interface is JTAG. JTAG_SWD is active high by default.

Table 16. JTAG interface

Pin no	Pin definition	I/O	Description
17	JTAG_TCK	I	JTAG test clock input signal
18	JTAG_TMS	I	JTAG test mode select input signal
19	JTAG_TDI	I	JTAG test data input signal
20	JTAG_TDO	O	JTAG test data output signal
21	JTAG_TRST	I	JTAG test reset signal

7.4.12 SWD interface

RW610FML provides a 2-line Serial Wire Debug interface (SWD). Keep JTAG_SWD at a low level. The downloading and debugging interface is SWD.

Table 17. SWD interface

Pin no	Pin definition	I/O	Description
27	SWCLK	I	Serial wire clock input
28	SWDIO	I/O	Serial wire debug data input/output

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7.4.13 LCD interface

RW610FML provides one LCD SPI interface.

Table 18. LCD interface

Pin no	Pin definition	I/O	Description
4	LCD_RESETN	O	LCD output signal to reset the device
5	LCD_TE	I	LCD tearing effect
6	LCD_SPI_DATA	I/O	LCD SPI data
7	LCD_SPI_DC	O	LCD SPI data/command select
8	LCD_SPI_SCK	O	LCD SPI clock
9	LCD_SPI_SS	O	LCD SPI chip select

7.4.14 DMIC interface

The RW610FML provides Pulse Density Modulation (PDM) data input for left and/or right audio channels, supported over one or two PDM data buses.

Table 19. DMIC interface

Pin no	Pin definition	I/O	Description
51	PDM_DATA01	I	PDM data input for DMIC channels 0 and 1
45	PDM_DATA23	I	PDM data input for DMIC channels 2 and 3
50	PDM_CLK01	O	PDM clock output for DMIC channels 0 and 1
52	PDM_CLK23	I/O	PDM clock output for DMIC channels 2 and 3

7.4.15 ACOMP interface

RW610FML provides two identical analog comparators for multiplexing:

- ACOMP0
- ACOMP1

The comparators are designed to have true rail-to-rail inputs and operate over the full voltage range of VIN. The comparator output state (high-level/low-level) is latched and can be used as interrupts.

Table 20. ACOMP interface

Pin no	Pin definition	I/O	Description
59	ACOMP0	A, I	ACOMP channel 0
36	ACOMP1	A, I	ACOMP channel 1
4	ACOMP2	A, I	ACOMP channel 2
5	ACOMP3	A, I	ACOMP channel 3
6	ACOMP4	A, I	ACOMP channel 4
7	ACOMP5	A, I	ACOMP channel 5
8	ACOMP6	A, I	ACOMP channel 6
9	ACOMP7	A, I	ACOMP channel 7
51	ACOMP0_GPIO_OUT	O	Analog comparator 0 level output

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Table 20. ACOMP interface...*continued*

Pin no	Pin definition	I/O	Description
45	ACOMP0_EDGE_PULSE	O	Analog comparator 0 edge pulse
50	ACOMP1_GPIO_OUT	O	Analog comparator 1 level output
52	ACOMP1_EDGE_PULSE	O	Analog comparator 1 edge pulse

7.4.16 UTICK

RW610FML provides one UTICK timer with four capture inputs.

Table 21. UTICK interface

Pin no	Pin definition	I/O	Description
13	UTICK_CAP0	I	Micro-tick timer capture input 0
16	UTICK_CAP1	I	Micro-tick timer capture input 1
23	UTICK_CAP2	I	Micro-tick timer capture input 2
14	UTICK_CAP3	I	Micro-tick timer capture input 3

7.4.17 SIM interface

RW610FML provides one (U)SIM interface.

Table 22. USIM interface

Pin no	Pin definition	I/O	Description
13	UCLK	O	(U)SIM clock
16	URST	O	(U)SIM reset
23	UIO	I/O	(U)SIM transmit receive

7.4.18 WCI-2 coexistence interface

RW610FML provides one WCI-2 coexistence interface.

Table 23. WCI-2 coexistence interface

Pin no	Pin definition	I/O	Description
30	WCI-2_SIN	I	External radio coexistence input
42	WCI-2_SOUT	O	External radio coexistence output

7.4.19 PTA coexistence interface

RW610FML provides one PTA coexistence interface.

Table 24. PTA coexistence interface

Pin no	Pin definition	I/O	Description
30	EXT_STATE	I	External radio state input (optional)
42	EXT_FREQ	I	External radio coexistence input (optional)
40	EXT_GNT	O	External radio coexistence output (mandatory)

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Table 24. PTA coexistence interface*...continued*

Pin no	Pin definition	I/O	Description
32	BOOTSEL_EXT_REQ	I	External radio coexistence request (mandatory)
43	EXT_PRI	I	External radio input priority (optional)

8 RF characteristics

This section summarizes the Radio-frequency (RF) performance characteristics and wireless communication capabilities of the module.

8.1 Wi-Fi radio specification

Unless otherwise stated, all specifications are at 25 °C, nominal voltage, and at RF connector.

Table 25. Wi-Fi receiver performance 2.4 GHz

Parameter	Condition	Typ	Unit
Receiver sensitivity 802.11b	1 Mbit/s	-96	dBm
Receiver sensitivity 802.11b	11 Mbit/s	-87	dBm
Receiver sensitivity 802.11g	6 Mbit/s	-90	dBm
Receiver sensitivity 802.11g	54 Mbit/s	-73	dBm
Receiver sensitivity 802.11n	MCS0 BPSK	-90	dBm
Receiver sensitivity 802.11n	MCS7 64QAM	-71	dBm
Receiver sensitivity 802.11ax	MCS0 BPSK	-90	dBm
Receiver sensitivity 802.11ax	MCS9 256QAM	-66	dBm

Table 26. Wi-Fi receiver performance 5 GHz

Parameter	Condition	Typ	Unit
Receiver sensitivity 802.11a	6 Mbit/s	-90	dBm
Receiver sensitivity 802.11a	54 Mbit/s	-73	dBm
Receiver sensitivity 802.11n	MCS0 BPSK	-90	dBm
Receiver sensitivity 802.11n	MCS7 64QAM	-71	dBm
Receiver sensitivity 802.11ac	MCS0 BPSK	-90	dBm
Receiver sensitivity 802.11ac	MCS8 256QAM	-67	dBm
Receiver sensitivity 802.11ax	MCS0 BPSK	-88	dBm
Receiver sensitivity 802.11ax	MCS9 256QAM	-65	dBm

Table 27. Wi-Fi transmit performance 2.4 GHz

Parameter	Condition	Typ	Unit
Maximum output power 802.11b	1 Mbit/s	19	dBm
Maximum output power 802.11b	11 Mbit/s	19	dBm

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Table 27. Wi-Fi transmit performance 2.4 GHz*...continued*

Parameter	Condition	Typ	Unit
Maximum output power 802.11g	6 Mbit/s	18	dBm
Maximum output power 802.11g	54 Mbit/s	17	dBm
Maximum output power 802.11n	MCS0 BPSK	18	dBm
Maximum output power 802.11n	MCS7 64QAM	16	dBm
Maximum output power 802.11ax	MCS0 BPSK	18	dBm
Maximum output power 802.11ax	MCS9 256QAM	15	dBm

Table 28. Wi-Fi transmit performance 5 GHz

Parameter	Condition	Typ	Unit
Maximum output power 802.11a	6 Mbit/s	18	dBm
Maximum output power 802.11a	54 Mbit/s	16	dBm
Maximum output power 802.11n	MCS0 BPSK	18	dBm
Maximum output power 802.11n	MCS7 64QAM	15.5	dBm
Maximum output power 802.11ac	MCS0 BPSK	18	dBm
Maximum output power 802.11ac	MCS8 256QAM	14.5	dBm
Maximum output power 802.11ax	MCS0 BPSK	18	dBm
Maximum output power 802.11ax	MCS9 256QAM	13.5	dBm

8.2 Bluetooth LE radio specification

This section provides the receiver and transmitter performance specifications for the Bluetooth LE radio.

Table 29. Bluetooth LE receiver performance

Parameter	Condition	Typ	Unit
Receiver sensitivity	Bluetooth LE 1 Mbit/s	-97	dBm
Receiver sensitivity	Bluetooth LE 2 Mbit/s	-95	dBm
Receiver sensitivity	Bluetooth LR 500 kbit/s	-98	dBm
Receiver sensitivity	Bluetooth LR 125 kbit/s	-104	dBm

Table 30. Bluetooth LE transmit performance

Parameter	Condition	Typ	Unit
Bluetooth LE maximum transmit power	-	8	dBm

8.3 Antenna

RW610FML is provided with the onboard PCB antenna.

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8.3.1 PCB antenna

This section provides the electrical and RF performance parameters of the onboard PCB antenna.

Table 31. PCB antenna parameters

Parameter	2.4 GHz band	5 GHz band
Frequency	2400 MHz - 2500 MHz	5150 MHz - 5850 MHz
Input impedance	50 Ω	50 Ω
VSWR	< 5	< 3.5
Maximum gain	2.4 dBi	3.1 dBi
Average efficiency	45 %	50 %

Figure 6 and Figure 7 show the radiation patterns for RW610FML with the onboard PCB antenna.

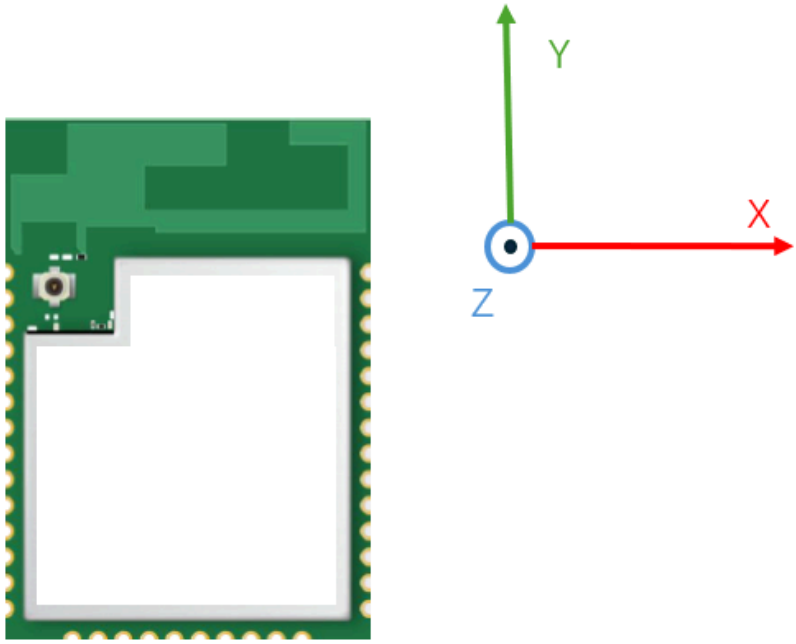


Figure 6. Radiation pattern

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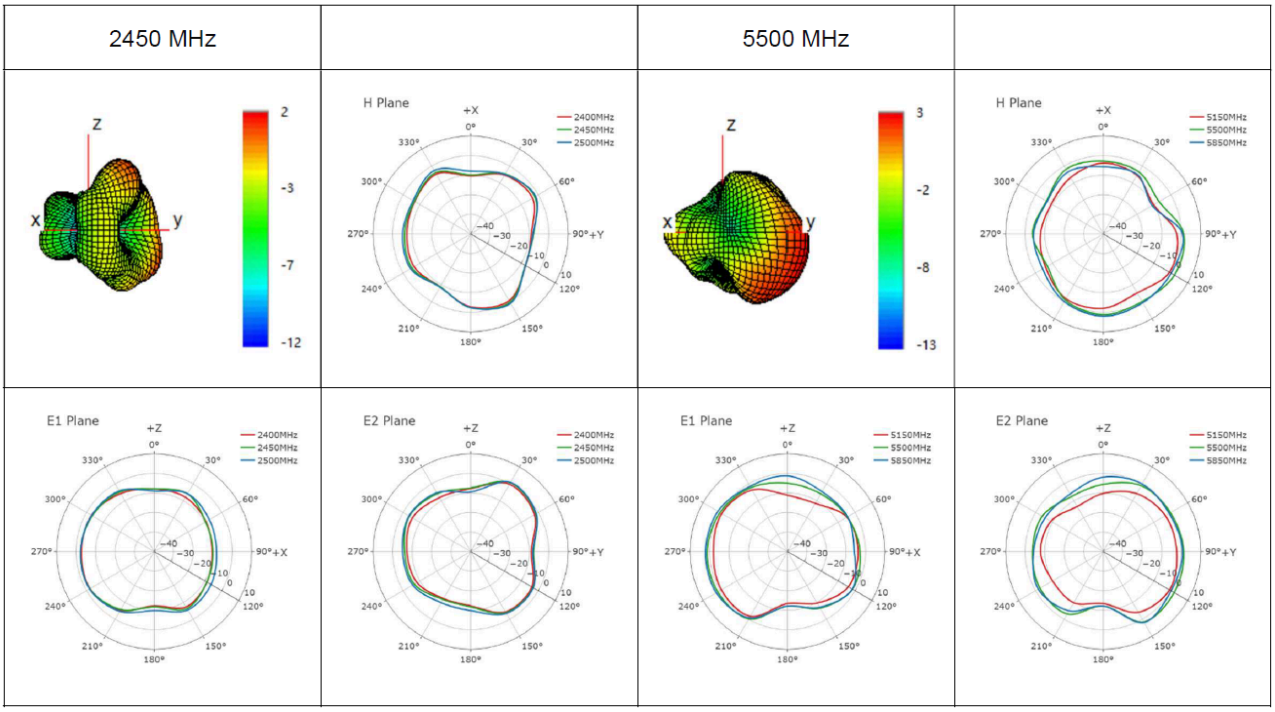


Figure 7. Radiation pattern

To ensure optimal RF performance and system reliability when using a PCB antenna, the following placement and layout guidelines must be observed:

- RW610FML must be placed at the edge of the host PCB.
- The PCB antenna must extend at least 6.3 mm beyond the edge of the host PCB.
- Maintain a minimum clearance of 16 mm between the PCB antenna and any power connectors, Ethernet ports, USB connectors, or other large components on the host PCB.
- When using a plastic enclosure, ensure a minimum clearance of 10 mm between the PCB antenna and the enclosure.
- When using a metal enclosure, use an external antenna instead of a PCB antenna.

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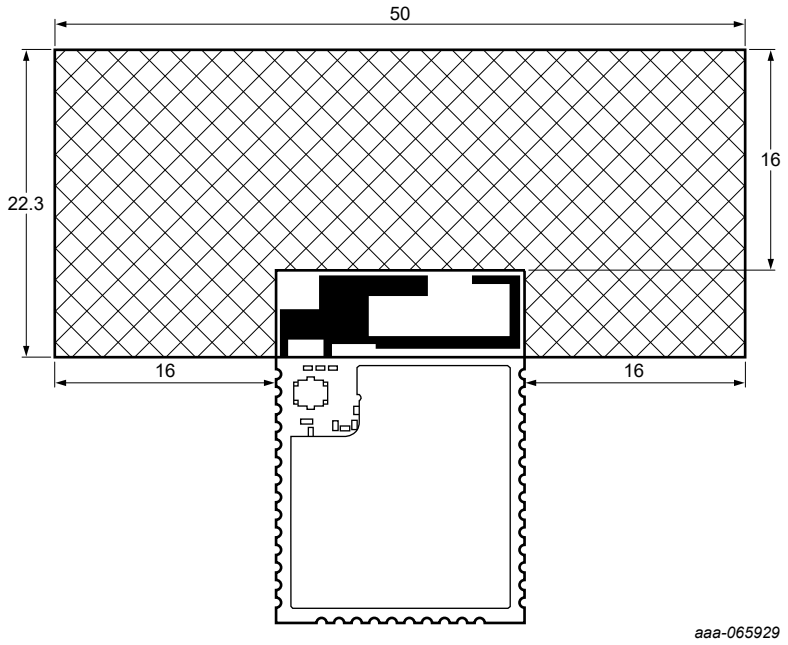


Figure 8. PCB antenna layout guidelines

9 Electrical specifications

This section provides the operating conditions, digital pad ratings, and power consumption characteristics of RW610FML.

9.1 Operating condition

CAUTION: *The absolute maximum ratings table defines the limitations for electrical and thermal stresses.*

These limits prevent permanent damage to the device. Exposure to conditions at or beyond these ratings is not guaranteed and can damage the device.

Table 32. Operating condition

Parameter	Min	Typ	Max	Unit
Operating temperature	-40	-	+85	°C
VIN	3.14	3.3	3.6	V
USB_VUSB	4.4	-	5.25	V

Table 33. Digital pad rating -3.3 V operation

Parameter	Min	Typ	Max	Unit
I/O pad supply voltage	2.97	3.3	3.63	V
Input high voltage	0.7 x VIN	-	VIN	V
Input low voltage	0	-	0.3 x VIN	V
Output high voltage	0.9 x VIN	-	VIN	V
Output low voltage	0	-	0.1 x VIN	V

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10 Mechanical information

This section describes the mechanical dimensions of RW610FML. All dimensions are measured in millimeters (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

10.1 Footprint information

Figure 9 shows the pin assignment of bottom view.

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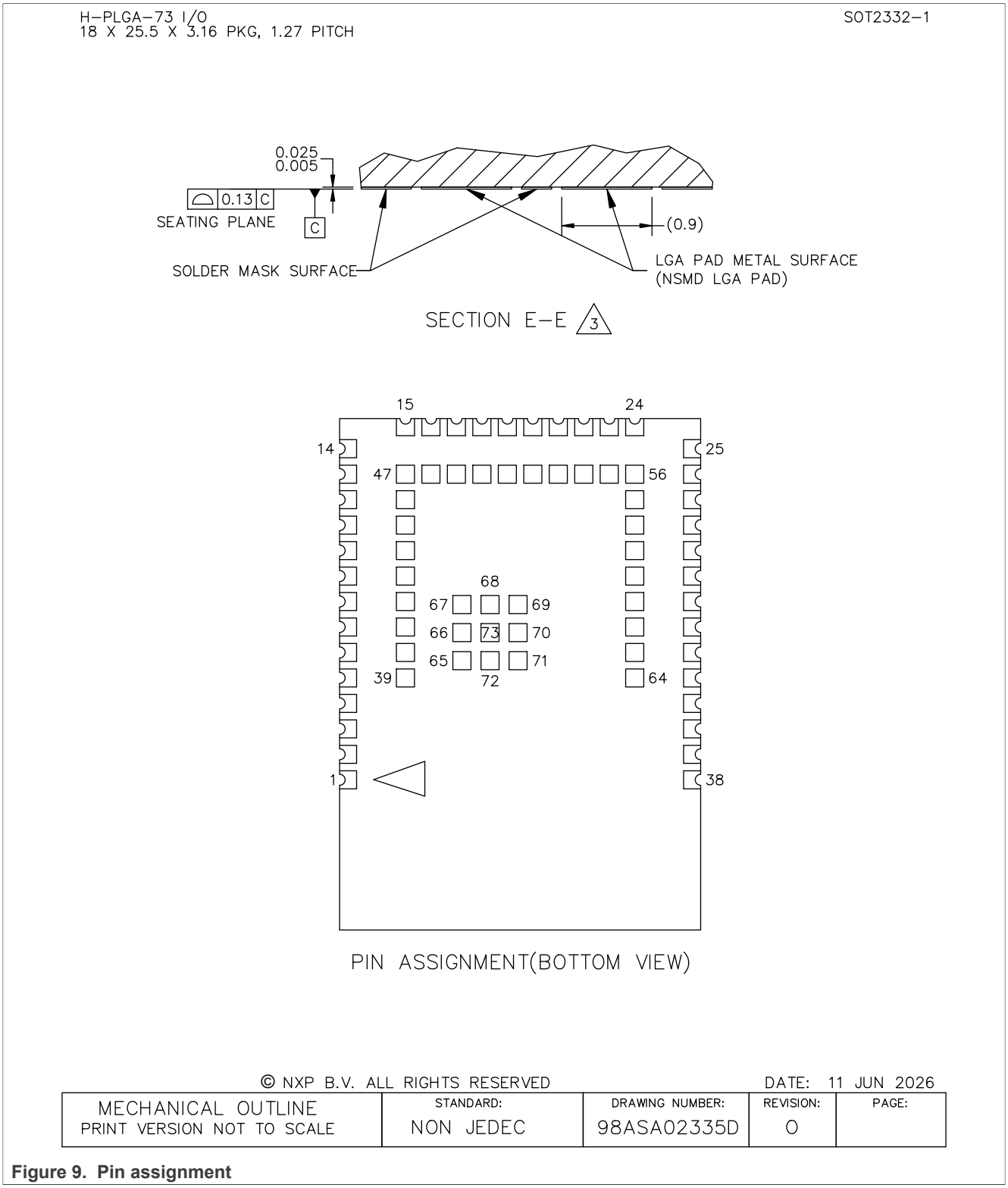


Figure 9. Pin assignment

10.2 Mechanical dimensions

Figure 10 shows mechanical dimensions of RW610FML.

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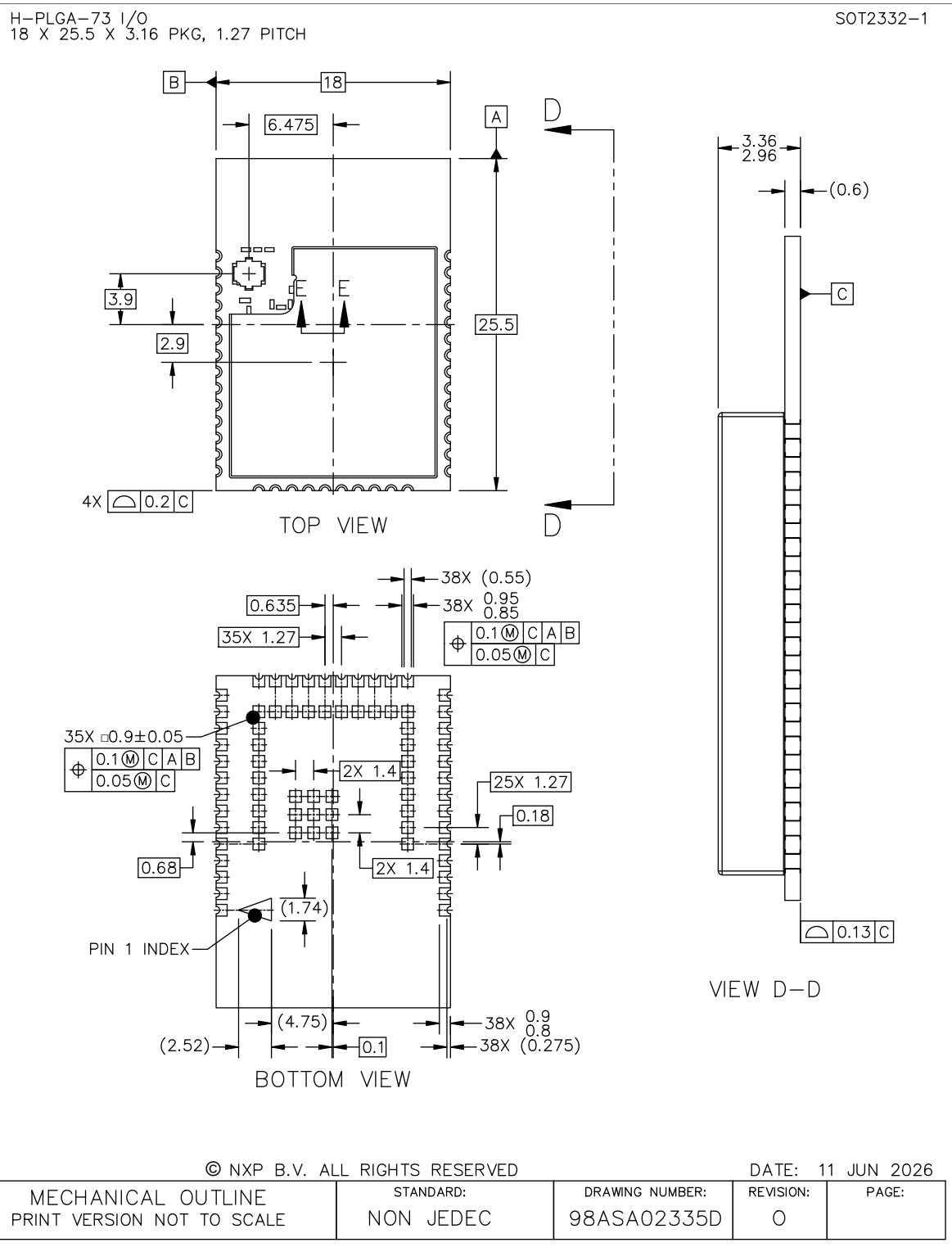


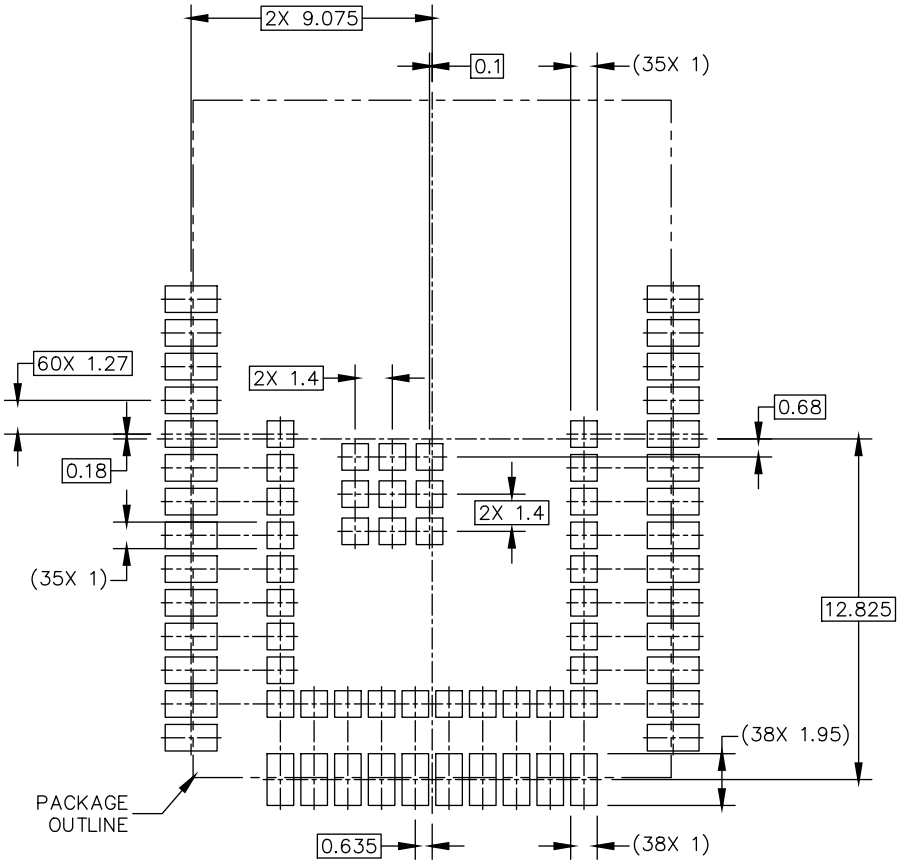
Figure 10. Mechanical dimensions

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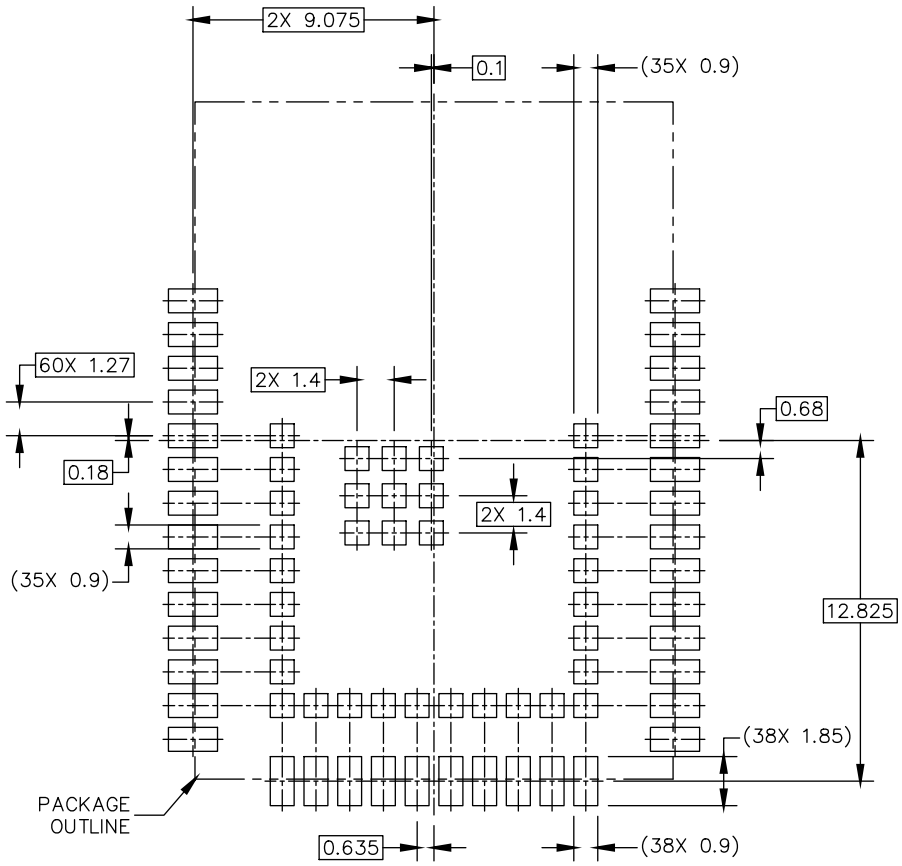
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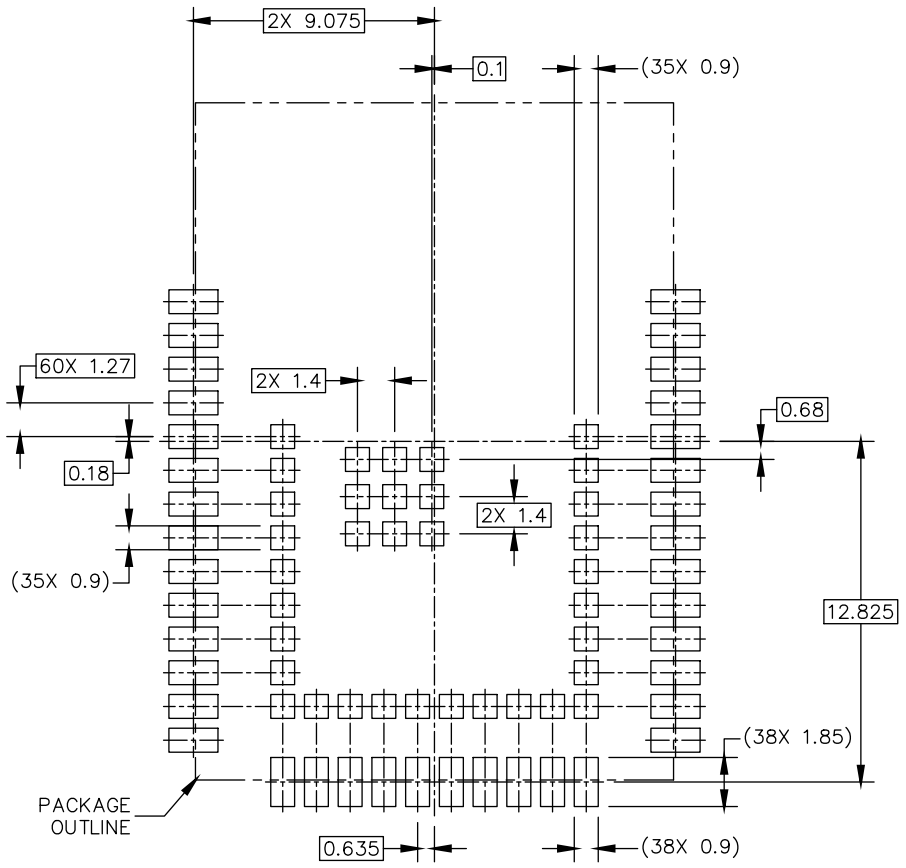
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RECOMMENDED STENCIL THICKNESS 0.125 OR 0.15

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 11. Mechanical dimensions

10.3 Package markings

Figure 12 shows the package markings for RW610FML.

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Figure 12. Package markings

11 Certifications and qualifications

The RW610FML module is certified for use in the countries/regions shown in the list below:

- Europe: CE
- America: FCC
- Canada: IC
- Australia/New Zealand: RCM
- Japan: Giteki

12 Handling and storage of information

This section outlines recommended handling practices and storage requirements to maintain product reliability and performance.

12.1 Handling information

Static electricity can occur naturally and damage RW610FML. Proper electrostatic discharge (ESD) protection measures and handling procedures must be implemented to ensure module reliability.

The following precautions are recommended during development, production, assembly, and testing:

- Wear appropriate anti-static protection, such as ESD gloves or wrist straps.
- Implement ESD protection components (such as TVS diodes) on ESD-sensitive interfaces and signal nodes in the system design.
- Handle RW610FML only in ESD-controlled environments.

12.2 Storage conditions

RW610FML is supplied in vacuum-sealed packaging and is classified with a Moisture Sensitivity Level (MSL) of 3. Recommended storage and handling requirements are described below:

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Storage conditions

- Recommended storage condition:
  - Temperature: 23 ± 5 °C
  - Relative humidity: 35 % to 60 %
- Shelf life (vacuum-sealed packaging):
  - 12 months when stored under the recommended storage conditions.
- Floor life: 168 hours in an environment with:
  - Temperature: 23 ± 5 °C
  - Relative humidity: ≤ 60 %
- Once the vacuum-sealed packaging is removed, RW610FML must undergo reflow-soldering, or other high-temperature processes within 168 hours.
- If this time is exceeded, RW610FML must be stored in a low-humidity environment (RH < 10 %), such as a dry cabinet, before further processing.

Pre-baking requirements

To prevent issues such as blistering, cracking, or internal PCB layer separation, RW610FML must be pre-baked under any of the following conditions:

- RW610FML is not stored under the recommended storage conditions.
- The specified floor life requirement is violated.
- The vacuum-sealed packaging is damaged or has been opened for more than 24 hours.
- RW610FML is to be reworked or repaired.

Pre-baking conditions

If pre-baking is required, the following conditions must be applied:

- Bake RW610FML at 120 ± 5 °C for 24 hours.
- After baking, RW610FML must be soldered to the PCB within 24 hours.
- If soldering cannot be completed within this timeframe, RW610FML must be stored in a dry environment, such as a dry cabinet.

13 Manufacturing and soldering

Push the squeegee to apply the solder paste on the surface of the stencil. As a result, the paste fills the stencil openings and penetrates to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.125 mm to 0.15 mm.

The recommended peak reflow temperature must be 235 °C to 246 °C, with 246 °C as the absolute maximum reflow temperature. To avoid damage to RW610FML caused by repeated heating, mount the RW610FML only after reflow soldering for the other side of the PCB has been completed. Figure 13 shows the recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters.

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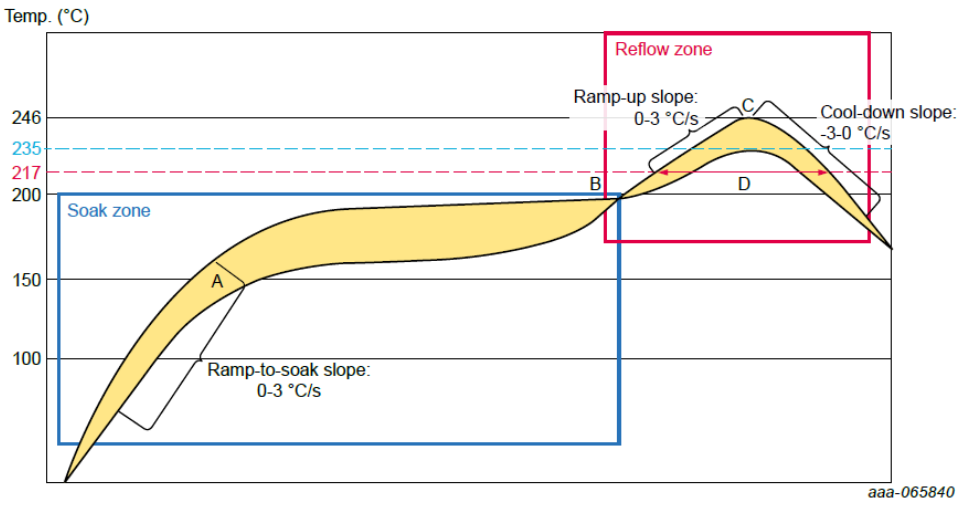


Figure 13. Reflow soldering thermal profile

14 Acronyms

Table 34 lists the acronyms used in this document.

Table 34. Acronyms

Term	Description
ACOMP	Analog Comparator
ADC	Analog-to-Digital Converter
AP	Access Point
Bluetooth LE	Bluetooth Low Energy
BPSK	Binary Phase-Shift Keying
CCK	Complementary Code Keying
CDM	Charged Device Model
CE	Conformité Européenne
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
DMIC	Digital Microphone
DQPSK	Differential Quadrature Reference Phase-Shift Keying
EVM	Error Vector Magnitude
FCC	Federal Communications Commission
GFSK	Gaussian Frequency Shift Keying
GND	Ground
GPIO	General-Purpose Input/Output
HBM	Human Body Model
HT	High Throughput

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Table 34. Acronyms...*continued*

Term	Description
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IC	Innovation, Science and Economic Development Canada (ISED) Certification
I^2S	Inter-IC Sound
IEEE	Institute of Electrical and Electronics Engineers
ISP	In-System Programming
JTAG	Joint Test Action Group
Kbit/s	Kilobits Per Second
LCC	Leadless Chip Carrier (package)
LCD	Liquid Crystal Display
LGA	Land Grid Array
Mbit/s	Million Bits Per Second
MCS	Modulation and Coding Scheme
MCU	Microcontroller Unit
NOR	Not OR
OTA	Over The Air
PCB	Printed-circuit board
PCM	Pulse Code Modulation
PDM	Pulse-density Modulation
PTA	Packet Traffic Arbitration
PWM	Pulse Width Modulation
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature phase-shift keying
RC	Resistor Capacitor
RH	Relative Humidity
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
SAE	Simultaneous Authentication of Equals
SD	Secure Digital
SDIO	Secure Digital Input/Output
SMD	Surface Mount Device
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
STA	Station
TBD	To Be Determined

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Table 34. Acronyms...*continued*

Term	Description
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
UTICK	Micro-tick Timer
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Normal Voltage Value
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCI	Wireless Coexistence Interface
Wi-Fi	Wireless Fidelity
WPA	Wi-Fi Protected Access
XIP	Execute in Place

15 References

The following reference provides more technical information about the RW610 device:

[1] *Wireless MCU with Integrated Wi-Fi 6 and Bluetooth Low Energy* (document RW610)

16 Revision history

Table 35 summarizes the revisions to this document.

Table 35. Revision history

Document ID	Release date	Description
RW610FML v.1.0	2 November 2026	Product datasheet • Initial release

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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