MFS5600AMBAFES – NXP Standard

Configuration report for FS5600-B OTP program ID: AF rev A

Rev. 1.1 - 11/14/2022 **Report**

1 General description

The FS5600 integrates a battery connected DC-DC controller with external FETs and a battery connected DC-DC converter with internal FETs. In addition, it offers functional safety features such as independent voltage monitors, windowed watchdog timer, I/O monitoring via ERRMON and FCCU and build-in-self-test.

Note: Electrical characteristics are maintained in the FS5600 data sheet

2 Features and benefits

- 2 x High-Voltage Buck Converters:
  - Buck Controller - External FETs - 900 mA gate drive current
  - Buck Regulator - Internal FETs - 3 A+ load capability
  - ±1.5 % Output Accuracy
  - 250 KHz to 3 MHz switching frequency
- High-efficiency PFM mode
- Safety Features:
  - Available in Enhanced ASIL B, ASIL B, and QM variations
  - 2 internal and up to 4 high-accuracy external voltage monitors
  - Windowed Watchdog Timer
  - ERRMON and FCCU monitoring
  - 2 x PGOOD and 1 x FS0B outputs
  - ABIST and LBIST for latest failure check
- GPIOs for seamless operation with PF PMICs
- Rated from –40 °C to 150 °C TJ
- 32-Ld 5 mm x 5 mm QFN
- AEC-Q100 Grade-1 Qualified

3 Applications

- Infotainment / Cluster / Driver Awareness
- Telematics
- V2X
- Radar
- Vision
- ADAS
- Sensor fusion

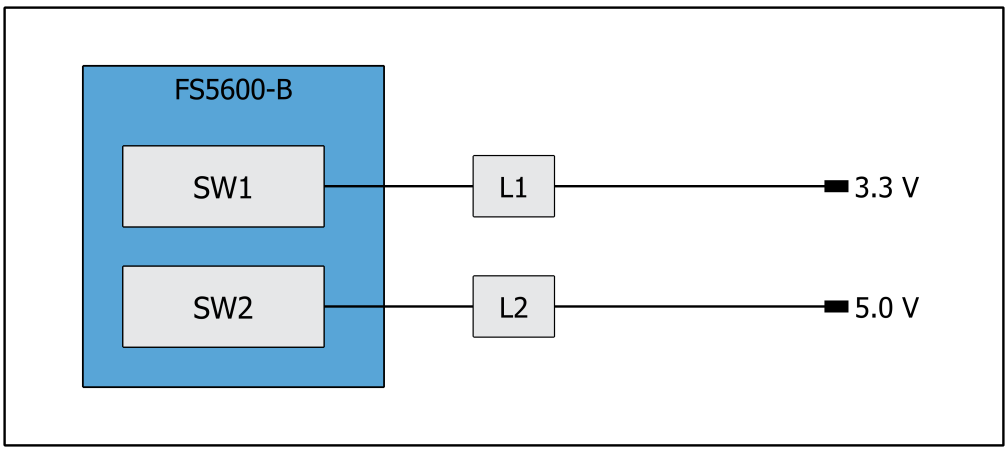
4 Ordering information

Table 1. Ordering information

Type number[1]	Package		
	Name	Description	Version
MFS5600AMBAFES	HVQFN32	HVQFN32 plastic thermally enhanced low profile quad flat package. 32 terminals; 0.5mm pitch; 5 mm x 5 mm x 0.85 mm body	SOT617-24(SC)

[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Hardware configuration diagram



6 OTP configuration

See FS5600 datasheet for parametric details. The OTP configuration summary for AF sequence ID is provided in Tables below.

Table 2. PGOOD and GPIO Control

Functional block	Feature	OTP selection
PGOOD1 CTRL	SW1 Under Voltage PGOOD1	SW1 asserts PGOOD1
	SW1 Over Voltage PGOOD1	SW1 asserts PGOOD1
	SW2 Under Voltage PGOOD1	SW2 will not assert PGOOD1
	SW2 Over Voltage PGOOD1	SW2 will not assert PGOOD1
	VMON1 Under Voltage PGOOD1	VMON1 will not assert PGOOD1
	VMON1 Over Voltage PGOOD1	VMON1 will not assert PGOOD1
	VMON2 Under Voltage PGOOD1	VMON2 will not assert PGOOD1
	VMON2 Over Voltage PGOOD1	VMON2 will not assert PGOOD1
	VMON3 Under Voltage PGOOD1	VMON3 will not assert PGOOD1
	VMON3 Over Voltage PGOOD1	VMON3 will not assert PGOOD1
	VMON4 Under Voltage PGOOD1	VMON4 will not assert PGOOD1
	VMON4 Over Voltage PGOOD1	VMON4 will not assert PGOOD1
	WD PGOOD1	WD does not Impact PGOOD
	FCCU Error PGOOD1	FCCU does not Impact PGOOD
PGOOD2 CTRL	SW1 Under Voltage PGOOD2	SW1 will not assert PGOOD2
	SW1 Over Voltage PGOOD2	SW1 will not assert PGOOD2
	SW2 Under Voltage PGOOD2	SW2 asserts PGOOD2
	SW2 Over Voltage PGOOD2	SW2 asserts PGOOD2
	VMON1 Under Voltage PGOOD2	VMON1 will not assert PGOOD2
	VMON1 Over Voltage PGOOD2	VMON1 will not assert PGOOD2

	VMON2 Under Voltage PGOOD2	VMON2 will not assert PGOOD2
	VMON2 Over Voltage PGOOD2	VMON2 will not assert PGOOD2
	VMON3 Under Voltage PGOOD2	VMON3 will not assert PGOOD2
	VMON3 Over Voltage PGOOD2	VMON3 will not assert PGOOD2
	VMON4 Under Voltage PGOOD2	VMON4 will not assert PGOOD2
	VMON4 Over Voltage PGOOD1	VMON4 will not assert PGOOD2
	WD PGOOD2	WD does not Impacts PGOOD
	FCCU Error PGOOD2	FCCU does not Impact PGOOD
PGOOD and GPIO Timing	Delay Duration Of PGOOD1	No Delay
	Delay Duration Of PGOOD2	No Delay
	Delay Duration Of GPIO1	Low
	Delay Duration Of GPIO2	Low
	Delay Duration Of GPIO3	Low
GPIO Configuration	GPIO1 Configuration	Output is high Z
	GPIO2 Configuration	GPO (output)
	GPIO3 Configuration	GPO (output)

Table 3. Regulators

Functional block	Feature	OTP selection
SW1 Enable and Mode	SW1 Mode	PWM
	SW1 Voltage	3.3 V
SW2 Enable and Mode	SW2 Mode	PWM
	SW2 Voltage	5.0 V
SW1 Loop design	SW1 Clock Select	CLK2
	SW1 Transconductance	28 us

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	SW1 Slope	90 mV/us
	SW1 Resistor Compensation	150 KOhm
SW2 Loop design	SW2 Clock Select	CLK2
	SW2 Slope Compensation	82 mV/us
SW1 Misc	SW1 Soft Start Ramp Slew Rate	675 us
	Peak Current Limit	6.5 A
	SW1 PFM On-time	630 ns
	SW1 Minimum On-time	80 ns
	SW1 Pull Down	Pull Down Enabled
SW2 Misc	SW2 Soft Start Ramp Slew Rate	5 mV/us
	SW2 ILIM Selection	150 mV
	SW2 PFM On-time	300 ns
	SW2 Minimum On-time	25 ns
	SW2 Pulldown Resistor	Pull Down Enabled
	SW2 High Slew Rate	2.8 Ohm PullUp/1.7 Ohm PullDn
	SW2 Low Slew Rate	1 Ohm PullUp/PullDn
SW1 and SW2 OFF Delay	SW1 Turn Off Delay	Off after EN1 goes low
	SW2 Turn Off Delay	Off after EN2 goes low
Clock Management	Clock1 Divide Ratio	CLK1 = CLK_FREQ / 8
	Clock2 Divide Ratio	CLK1 = CLK_FREQ / 48
	Input Frequency Range At SYNCIN Pin	2000 KHz and 3000 KHz
	Clock Frequency (MHz)	22 MHz
	Frequency Spread Spectrum	Enabled
	Modulation Frequency	22 KHz

Table 4. Functional Safety

Functional block	Feature	OTP selection
Normal and Deep Fail Safe Entry	Normal State	Enabled
	Deep Fail Safe State	0
	PGOOD1 Safe State	Low
	PGOOD2 Safe State	Low
	ERRMON1 Safe State	Low
	ERRMON2 Safe State	Low
VMON Threshold Selection	VMON1 UV Detection Threshold	95.5 %
	VMON1 OV Detection Threshold	104.5 %
	VMON2 UV Detection Threshold	95.5 %
	VMON2 OV Detection Threshold	104.5 %
	VMON3 UV Detection Threshold	95.5 %
	VMON3 OV Detection Threshold	104.5 %
	VMON4 UV Detection Threshold	95.5 %
	VMON4 OV Detection Threshold	104.5 %
ABIST and LBIST	ABIST Enable	ABIST Enabled
Watchdog Timer	Watchdog Operation	Watchdog Disabled
	Watchdog Selection	Simple WD
	Watchdog Fail Impact	Stay in NORMAL STATE
ERRMON1	ERRMON1 Fault Polarity	Low
	ERRMON1 Acknowledge Timer	1 ms
ERRMON2	ERRMON2 Fault Polarity	Low
	ERRMON2 Acknowledge Timer	1 ms

VMON Debounce Selection	VMON1 UV Debounce Timing	5 us
	VMON1 OV Debounce Timing	30 us
	VMON2 UV Debounce Timing	5 us
	VMON2 OV Debounce Timing	30 us
	VMON3 UV Debounce Timing	5 us
	VMON3 OV Debounce Timing	30 us
	VMON4 UV Debounce Timing	5 us
	VMON4 OV Debounce Timing	30 us
Fault Counter Config	SW1 Fault Error Counter	Disable
	SW2 Fault Error Counter	Disable
	VMON1 Fault Error Counter	Disable
	VMON2 Fault Error Counter	Disable
	VMON3 Fault Error Counter	Disable
	VMON4 Fault Error Counter	Disable
	ERRMON1 Fault Error Counter	Disable
	ERRMON2 Fault Error Counter	Disable
	FCCU Fault Error Counter	Disable

Table 5. Miscellaneous

Functional block	Feature	OTP selection
MODE/SYNCIN Selection	Mode Select For SYNCINB	MODE
	MODE Debounce	Falling Edge - 40 us and Rising Edge - 10 us
I2C Configuration	I2C CRC Enable	CRC Disabled
	Device Address	0x18
Miscellanous	Ultra Low Power Operation Enable	Reduction in quiescent current

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