PN7220/PN7221

NFC controller with NCI interface supporting EMV and NFC Forum applications

Rev. 4.1 — 5 November 2026 Product short data sheet

1 General description

This document describes the functionality and electrical specification of the PN7220 and PN7221 high-power NFC controller family with NCI interface.

The product PN7221 supports all features of the PN7220 plus "Enhanced Contactless Polling" (ECP) by Apple. Note that the ECP feature is available after formal authorization only. In the following document, PN7220 refers to both PN7220 and PN7221 unless stated otherwise.

As an NCI 2.2 compliant NFC controller with high RF output (2 W) and high receiver sensitivity, the NXP PN7220 is a robust solution for payment terminals and all readers that must generate a strong RF field in a difficult environment. Offering full compliance with EMVCo 3.1 L1 analog and digital, the PN7220 simplifies designs while ensuring interoperability with a broad range of smartcards and mobile phones.

In addition to the reader/writer functionality, the device supports the host card emulation of ISO14443-A cards up to 848 kbit/s and three TDA8035 which offers the possibility for an ISO 7816 contact interface connection.

The PN7221 is based on the PN7220 and supports all features of PN7220 plus "Enhanced Contactless Polling" (ECP) by Apple - this description is not part of this document. Note that the ECP feature is available after formal authorization only.

Two host connection options are available for this product:

1. Connection to one single host - this is typically one host running an Android operating system
2. Connection to two hosts - in this case one host is typically a security CPU connected by the SPI interface to meet PCI compliance requirements for an EMVCo payment subsystem, and the second host connected by an I^2C interface which is typically used to run an Android operating system for all non-EMVCo payment related applications.

The PN7220 communicates with a connected host through a physical interface using the NCI 2.2 protocol.

The PN7220 supports two types of configurable polling loops: one NFC Forum polling loop, and one EMVCo compliant polling loop. Switching between the polling loops is done based on a hardware input (GPIO) triggered by a connected host - in case of a switching of the polling loop all data from an ongoing transaction is cleared from the internal buffers, the NCI software stack is being reset and an RF reset is being executed. This helps to ensure data integrity for the performed transaction and allows to connect the right logical software endpoints to each of the polling loops.

To speed-up the switching between NFC Forum polling and EMVCo polling and ease the RF configuration of each polling loop, two independent sets of RF configuration data can be stored in EEPROM. This allows to optimize each polling loop to meet individual RF requirements.

The PN7220 product family supports highly innovative and unique features which do not require any host controller interaction. These features include dynamic power control (DPC), adaptive waveshape control (AWC), and fully automatic EMD error handling.

Additional documents supporting a design-in of the PN7220/PN7221 are available on nxp.com.

In this document, the term "MIFARE card" refers to a contactless card with an embedded MIFARE IC.

For more information, refer to the PN7220 product page ref.[1] and full data sheet ref.[2] on nxp.com.

This data sheet requires additional documents for functional chip description and design-in.

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2 Features and benefits

2.1 RF functionality

2.1.1 ISO/IEC 14443-A

- Reader/writer mode supporting ISO/IEC 14443-A R/W up to 848 kbit/s

2.1.2 ISO/IEC 14443-B

- Reader/writer mode supporting ISO/IEC 14443-B up to 848 kbit/s

2.1.3 FeliCa

- Reader/writer mode supporting FeliCa 212 kbit/s and 424 kbit/s (without crypto)

2.1.4 Tag type reading

- Supports reading of all NFC tag types (type 2, type 3, type 4A and type 4B, type 5)

2.1.5 MIFARE card reading

- Reader/writer communication mode for the MIFARE card family including MIFARE Classic Crypto supporting MIFARE Classic en-/decryption is integrated in hardware

2.1.6 ISO/IEC 15693

- Reader/writer mode supporting ISO/IEC 15693 (ICODE)
  - RX: "Manchester" encoding with 424 kHz single-subcarrier (SSC) and 6.6 kBd
  - RX: "Manchester" encoding with 424 kHz single-subcarrier (SSC) and 26 kBd

2.1.7 NFC Forum compliancy

- NFC Forum version 13 compliance for R/W – analog and digital

2.1.8 EMVCo contactless compliancy

- Contactless EMVCo 3.1 compliance for R/W – digital
- Contactless EMVCo 3.1 compliance for R/W analog can be achieved, but depends on connected antenna geometry and size, matching network and RF settings.

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2.1.9 Host interface

The devices PN7220 and PN7221 support one host interface using a single interface connection based on an I^2C interface host interface (host interface 1) with data rates up to 3.4 Mbit/s.

In addition, the device supports two host interfaces using one interface connection based on an I^2C interface (host interface 2) up to 3.4 Mbit/s and one SPI interface (host interface 1) up to 15 Mbit/s.

The logical interface layer of the host interfaces is based on the NCI 2.2 interface specification, enhanced by NXP proprietary commands.

2.2 Transmitter

- Transmitter with high RF output power of 2.0 W
- Dynamic power control 2.0 (DPC) (dynamic power control without processing load on host MCU)
- Adaptive waveshape control (AWC)

2.3 Receiver

- Robust receiver: Automatic configuration, advanced insensitivity against TFT display noise for higher RF performance

2.4 Integrated polling loop

- RF polling loop according to NFC Forum
- RF Polling loop according to EMVCo 3.1, integrated EMVCo L1 software stack

2.5 Integrated DC-DC

The PN7220 implements an integrated DC-DC which can be used to supply the transmitter. Since the supply voltage of the transmitter LDO can be up to 6.0 Volts, this simplifies the design of the power supply.

A single supply concept for the RF system, for example, with single 3.3 V supply, is possible and allows making use of the maximum RF output power by providing a maximum transmitter supply voltage.

The integrated DC-DC is used by the dynamic power control (DPC) to reduce the maximum power dissipation of the chip.

The usage of the DC-DC is optional.

For applications making use of the low-power card detection, the DC-DC is available.

2.6 RF debugging support

- RF debugging without external probing of test signals possible by sampling debug data into chip-internal memory based on pre-defined trigger conditions – ideal debugging solution for PCI-compliant POS terminals
- One digital and one analog debug signal is provided by the chip for connection of an oscilloscope.

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2.7 ISO 7816 contact interface

The product supports the connection of up to three TDA8035 ICs which is the default EEPROM configuration of the device.

The device features an integrated EMVCo L1 contact card activation, and is compliant with contactless EMVCo specification 3.x.

The contact interface can be used for a single or dual host configuration.

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3 Applications

- Payment terminals following the COTS security requirements with full EMVCo 3.1 analog and digital compliancy
- Multi-application terminals
- Ticket validators for the controlling staff in public transport
- E-vehicle charging stations
- Vending machines

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4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(VBAT)}$	supply voltage on pin VBAT (analog and digital supply)	VBAT ≥ VDDIO	2.4	-	5.5	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO (supply for host interface and GPIOs)	1.8 V supply	1.62	-	1.98	V
		3.3 V supply	2.4	-	3.6	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA (input of the transmitter power amplifier)	PN7220 - supply with VDDPA from internal VDDPALDO with DC-DC	1.5	-	5.7	V
I_{pd}	power down current	$VDD_{(VDDPA)}$ = $VDD_{(VDDIO)}$ =$VDD_{(VDD)}$ 3.0 V; hard power down state; pin VEN set LOW, T_{amb} = 25 °C, External supply by VDDIO	-	40	105	µA
I_{stb}	standby current	T_{amb} = 25 °C	-	45	110	µA
$IDD_{(VDDPA)}$	supply current on pin VDDPA	supplied via VUP_TX (TX_LDO active)	-	-	350	mA
		supplied without DC-DC and TXLDO active	-	-	400	mA
$P_{(PA)}$	transmitter output power	supplied via VUP_TX (TX_LDO active)	-	-	2.0	W
		supplied without DC-DC and TXLDO active	-	-	2.3	W
T_{amb}	ambient operating temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB TX $current_{max}$ = 350 mA @ $VDDPA_{max}$ = 5.7 V	-40	-	+85	°C
		in still air with exposed pins soldered on a 4 layer JEDEC PCB TX $current_{max}$ = 120 mA @ $VDDPA_{max}$ = 3.6 V	-40	-	+105	°C
T_{stg}	storage temperature	no supply voltage applied	-55	-	+150	°C
T_{j_max}	maximum junction temperature	-	-	-	+125	°C

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5 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN7220EV/C100K	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs The ending "K" in the product name is indicating the packing "multiple tray"; 12NC (order number) ending - 557 Version for connection to 1 host microcontroller Initialized with firmware version 1.00	SOT1307-2
PN7220EV/C100Y	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518 Version for connection to 1 host microcontroller Initialized with firmware version 1.00	SOT1307-2
PN7221EV/C100K	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs The ending "K" in the product name is indicating the packing "multiple tray"; 12NC (order number) ending - 557 Version for connection to 1 host microcontroller and ECP - Initialized with firmware version 1.00	SOT1307-2
PN7221EV/C100Y	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518 Version for connection to 1 host microcontroller and ECP - Initialized with firmware version 1.00	SOT1307-2
PN7220EV/C101K	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs The ending "K" in the product name is indicating the packing "multiple tray"; 12NC (order number) ending - 557 Version for connection to 1 or 2 host microcontroller Initialized with firmware version 2.02	SOT1307-2
PN7220EV/C101Y	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518 Version for connection to 1 or 2 host microcontroller Initialized with firmware version 2.02	SOT1307-2

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Table 2. Ordering information...*continued*

Type number	Package		
	Name	Description	Version
PN7221EV/C101K	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs The ending "K" in the product name is indicating the packing "multiple tray"; 12NC (order number) ending - 557 Version for connection to 1 or 2 host microcontroller and ECP - Initialized with firmware version 2.02	SOT1307-2
PN7221EV/C101Y	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518 Version for connection to 1 or 2 host microcontroller and ECP - Initialized with firmware version 2.02	SOT1307-2

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6 Block diagram

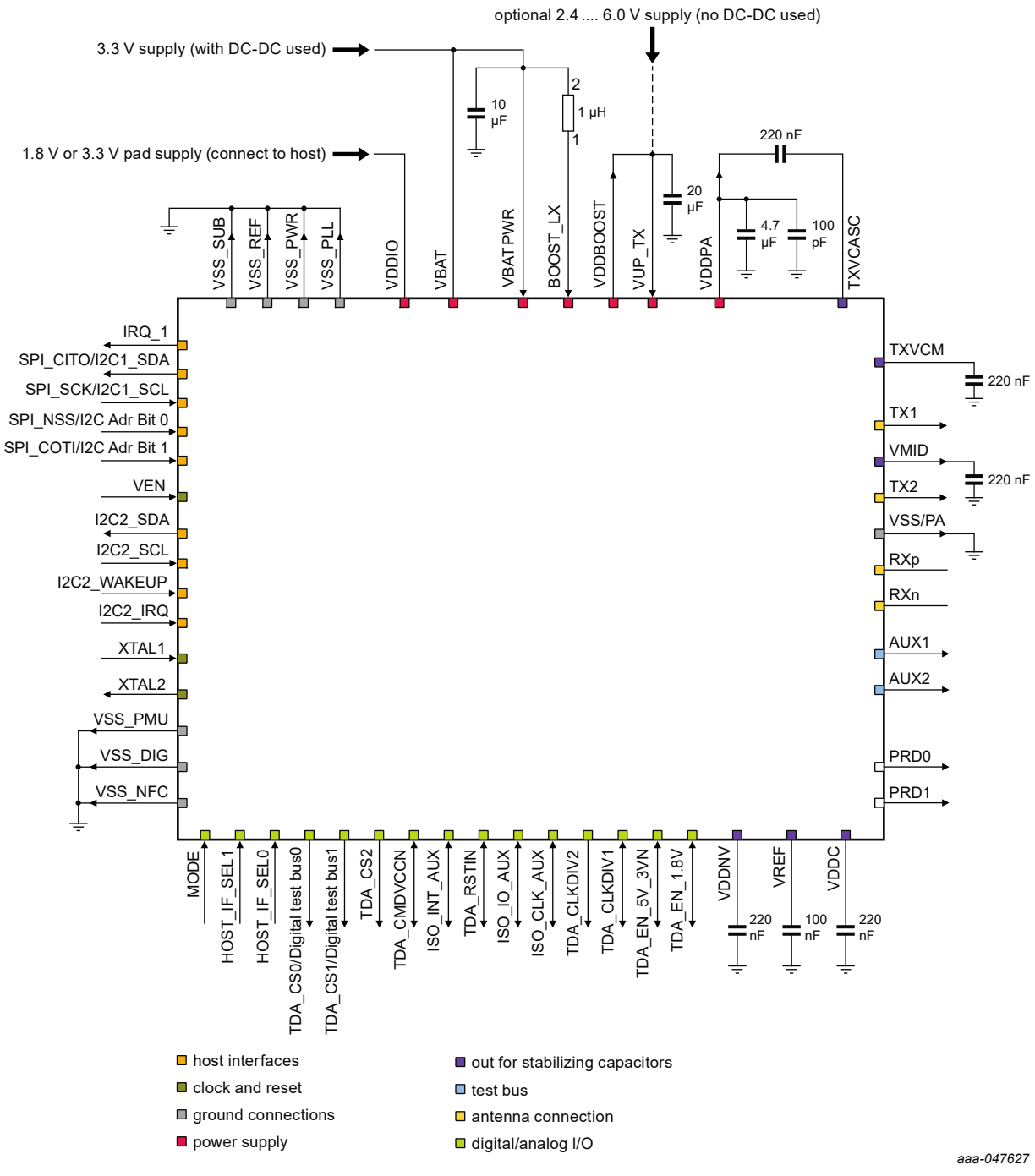


Figure 1. System connections [1]

[1] The replacement of "MOSI/MISO" to "COTI/CITO" in this document follows the recommendation of the NXP - I^2C standards organization.

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The PN7220 is connected to an application processor / host CPU based on an NCI interface.

The device offers high compatibility to existing solutions which offer an NCI interface (Host IF_1). The physical interface used for the connection is a I^2C interface.

Host IF_1 allows I^2C data rates up to 3.4 Mbit/s.

I^2C address:

The PN7220 host interface 1 supports the 7-bit addressing mode. The first five bits are fixed and set to decimal 40, the last two bits are configurable using ADDR0 and ADDR1 pins. This provides maximum flexibility even in cases where the I^2C bus is shared with other devices on top of the PN7220.

Default mode after boot:

The system is always booting in mode (EMVCo polling or NFC Forum polling) defined by the level on the pin MODE/GPIO2.

Switching between NFC Forum and EMVCo polling:

Switching to a EMVCo polling loop is done based on a physical signal "MODE/GPIO2" controlled by the application processor / host CPU. All previous data from earlier communications are erased, and the NCI software stack is being reset. The system enters then the new EMVCo polling mode. Switching back to NFC Forum mode again clears all previous data from earlier communication and resets the NCI software stack.

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7 Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(VUP_TX)}$	supply voltage on pin VUP_TX	-	-0.3	6.3	V
$V_{DD(VBAT)}$	supply voltage on pin VBAT	-	-0.3	5.8	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO	on pin VDDIO, power supply for host interface and GPIOs	-0.3	3.8	V
$V_{DD(GPIO_x)}$	input voltage on pin used as GPIO	-	-0.3	3.8	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA	maximum limiting values for $I_{DD(VDDPA)}$ and $T_{j(max)}$ not violated	-	6.0	V
$V_{i(RXP)}$	input voltage on pin RXP	-	-0.3	2	V
$V_{i(RXN)}$	input voltage on pin RXN	-	-0.3	2	V
V_{ESD}	electrostatic discharge voltage	human body model (HBM)[1]	-2000	2000	V
		charge device model (CDM)[2]	-500	500	V
$T_{j(max)}$	junction temperature	-	-	125	°C
T_{stg}	storage temperature	no supply voltage applied	-55	150	°C

[1] According to ANSI/ESDA/JEDEC JS-001
[2] According to ANSI/ESDA/JEDEC JS-002

Stress above one or more of the limiting values may cause permanent damage to the device or limit the lifetime.

Product might not behave according to specification.

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8 References

[1] Webpage – PN7220: High-Performance, One-Chip NFC Controller for EMVCo 3.2 and NFC Forum Operation (link)

[2] Data sheet – PN7220/PN7221 NFC controller with NCI interface supporting EMV and NFC Forum applications (link)

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9 Revision history

Table 4. Revision history

Document ID	Release date	Description
PN7220_PN7221_SDS v.4.1	5 November 2026	Released alongside data sheet update.

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Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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